SEMICONDUCTOR PACKAGE HAVING INCREASED SOLDER JOINT STRENGTH

TECHNICAL FIELD OF THE INVENTION

The present invention relates to semiconductor packages, and more particularly, but not by way of limitation, to semiconductor packages with increased solder joint strength for mounting the semiconductor package to external surfaces.

HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski, and incorporated by reference. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, consumer demand increases. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

Such conventional semiconductor packages are not without certain problems. Specifically, in a typical semiconductor package the bottom surface of the externally exposed leads is flat. The flat bottom surface of these externally exposed leads results in a weakening of the solder joint strength between the semiconductor package and an external surface, such as that of a motherboard. When the semiconductor package is mounted onto a motherboard or other surface by soldering, the flat bottom surface of the leads may lack enough friction to readily maintain a sufficient solder joint strength. As a result, the semiconductor package may undesirably detach from the motherboard at one or more critical locations. This is extremely undesirable and is a distinct disadvantageous aspect of prior art designs. The present invention addresses such problems by providing semiconductor packages with increased solder joint strength.

BRIEF SUMMARY OF THE INVENTION

The present invention relates to semiconductor packages. More particularly, one aspect of the present invention comprises a semiconductor chip having an upper surface and a bottom surface in conjunction with the following features of the invention. A plurality of input bond pads and output bond pads on the upper surface of the semiconductor chip and along the perimeter of the semiconductor chip are electrically connected to the semiconductor chip. A chip paddle is provided which has a top surface, a side surface and a bottom surface. The chip paddle, being bonded to the bottom surface of the semiconductor chip by an adhesive, also has corners, a perimeter and a half-etched section at the lower edge along its perimeter. A leadframe is also provided with a plurality of tie bars. Each of the tie bars has a side surface and a bottom surface. The plurality of tie bars are connected to the corners of the chip paddle. The plurality of the tie bars externally extend from the chip paddle and have a half-etched section. A plurality of dam bars are provided on the leadframe help limit flow of encapsulation material on the leadframe. A plurality of leads, referred to alternately as internal or external, connect to the leadframe. Each of the leads has a side surface and a bottom surface. The leads are radially formed at regular intervals along and spaced apart from the perimeter to the chip paddle and extend towards the chip paddle. Each of the leads has a step shaped half-etched section facing the chip paddle. A plurality of conductive wires, comprised of a suitable conductor, are electrically connected to and between the plurality of leads and the semiconductor chip. Encapsulating or encapsulant material encapsulates the semiconductor chip, conductive wires, chip paddle, and the leads to form a package body. The flow of the encapsulation material is limited by the dam bars formed on the leadframe. The dam bars also serve to stabilize the leads on the leadframe. After encapsulation, the chip paddle, leads, and tie bars are externally exposed at respective side and bottom surfaces.

The above described assembly further includes, in accordance with the present invention, at least one depression formed on the externally exposed bottom surface of the leads to improve the solder joint strength with a motherboard. Alternately and additionally, at least one depression may be formed on the externally exposed bottom surface of the leads. Likewise, at least one depression may be formed on the externally exposed bottom surface of at least one tie bar to increase the solder joint strength. The

presence of the depressions in the respective locations of the semiconductor package serves to provide an additional area which may fuse with the solder, thereby strengthening the solder joint strength between the semiconductor package and the motherboard.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

FIGURE 1 is a side elevational, cross-section view of a one embodiment of the semiconductor package of the present invention, wherein depressions are formed on the externally exposed bottom surface of the leads;

FIGURE 2 is a bottom plan view of the semiconductor package of FIGURE 1;

FIGURE 3 is a side elevational, cross section view of the semiconductor package of FIGURES 1 and 2 after the semiconductor package has been connected to a motherboard;

FIGURE 4 is a bottom plan view of an alternate embodiment of the semiconductor package of the present invention, wherein depressions are formed on the externally exposed bottom surface of the tie bars;

FIGURE 5 is a bottom plan view of an alternate embodiment of the semiconductor package of the present invention, wherein depressions are formed on the externally exposed bottom surface of the chip paddle; and

FIGURE 6 is a top plan view of a leadframe used to make the semiconductor package of FIGURE 1.

DETAILED DESCRIPTION OF THE INVENTION

Referring first to FIG. 1 there is shown a cross sectional view of one embodiment of a semiconductor package 10 constructed in accordance with the principles of the present invention. The semiconductor package 10 includes a corner 12 (FIG. 2) and bottom surface 15. The semiconductor package 10 includes a semiconductor chip 20 having an upper surface 30, and a bottom surface 50. A plurality of input bond pads 60 and output bond pads 70, collectively referred to as bond pads, are disposed on the upper

surface 30 of the semiconductor chip 20. A chip paddle 80 having a top surface 90 and a bottom surface 110 (FIG. 2) is secured to the bottom surface 50 of the semiconductor chip 20 via an adhesive 120. The chip paddle 80 has corners 130, a perimeter 140 (FIG. 2) and may include a half-etched section 150. The half-etched section 150 is located at a lower edge of the chip paddle 80.

Referring now to FIGS. 1, 2 and 6 in combination, a leadframe 170 is shown having a plurality of tie bars 180, a side surface and a bottom surface. The tie bars 180 are connected to the corners 130 of the chip paddle 80 and include a bottom surface 185. The tie bars 180 externally extend from the chip paddle 80. The leadframe 170 further has a half-etched section 210 and a plurality of dam bars 220.

A plurality of finger-like leads 230 are connected to the leadframe 170 and have an upper surface 235, a side surface 240 and a bottom surface 250. Upper surface 235 may, but does not have to be electroplated with gold or silver. The leads 230 are radially formed at regular intervals along the perimeter 140 and spaced apart from the perimeter 140 of the chip paddle 80. The leads 230 extend towards the chip paddle 80, such that each of the plurality of leads 230 has a half-etched section 260 facing the chip paddle 80.

To enclose the semiconductor package 10, encapsulation material 280 encapsulates the semiconductor chip 20, conductive wires 270, chip paddle 80, and leads 230. Encapsulation material 280 may be thermoplastics or thermoset resins, with the thermoset resins including silicones, phenolics, and epoxies. The dam bars 220 limit the flow of the encapsulation material 280 on the leadframe 170 and provide stability to the leads 230 on the leadframe 170. During encapsulation, the chip paddle 80, leads 230, and tie bars 180 may be externally exposed at the respective side and bottom surfaces. The respective half-etched sections 150, 210, and 260 of the chip paddle 80, tie bars 180, and leads 230 are provided to increase the bonding strength of the encapsulation material 280 in the semiconductor package 10. It is contemplated that the respective half-etched sections 150, 210, and 260 may be eliminated without departing from the scope and spirit of this invention.

In a first embodiment of the present invention, at least one depression 310 is formed on the bottom surface 250 of the leads 230, which are externally exposed on the bottom surface 15 of the semiconductor package 10. The depressions 310 may have various configurations in cross-section, and as such may include but are not limited to

rectangular, hemispherical, square, triangular, circular, and omega shapes. The depressions 310 provide additional area on the bottom surface 15 of the semiconductor package 10 for solder 320 to be applied when the semiconductor package 10 is secured to a motherboard 330, best seen in FIG. 3. When the semiconductor package 10 is secured to the motherboard 330, the variety of cross-sectional configurations of the depression 310 support the increased solder joint strength between the motherboard 330 and the semiconductor package 10. As shown in FIGS. 1-3, a plurality of depressions 310 is preferred to maximize the solder joint strength between the semiconductor package 10 and the motherboard 330. As seen in FIG. 3, the solder 320 expands into the depression 310 and thereby provides increase interlocking location for the solder 320 to expand when the semiconductor package 10 is secured to the motherboard 330.

The depressions 310 may be formed by a chemical etching process, wherein the depressions 310 are contoured when a typical full etching process is conducted to form a general pattern of the leadframe 170, including the chip paddle 80, tie bars 180, leads 230, and dam bars 220. Alternatively, the depressions 310 may be formed after the typical full etching process for the leadframe 170, wherein the area in which the depressions 310 are to be formed is coated with a photoresist (not shown) while the remaining area of the surface is uncoated. During this alternate process, an etchant (not shown) is sprayed directly over the uncoated area to form the depressions 310. Alternatively, the depressions 310 may be formed by mechanical stamping, wherein a punch is applied to the position at which the depressions 310 are to be formed.

In an alternate embodiment shown in FIG. 4, at least one depression 310 is formed on the bottom surface 185 of the tie bars 180. In still another embodiment of the present invention shown in FIG. 5, at least one depression 310 may be formed on the bottom surface 110 of the chip paddle 80. The solder 320 (FIG. 3) on the bottom surface 110 of the chip paddle 80 further increases the heat radiation performance of the semiconductor chip 20. The depressions 310 formed on the tie bars 180 and chip paddle 80 may be created by any of the methods described above.

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

Attorney Docket No.	Title of Application	First Named Inventor
09/687,485	Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly	Young Suk Chung
09/687,876	Near Chip Size Semiconductor Package	Sean Timothy Crowley
09/687,495	Semiconductor Package	Sean Timothy Crowley
09/687,531	Stackable Semiconductor Package and Method for Manufacturing Same	Sean Timothy Crowley
09/687,530	Stackable Semiconductor Package and Method for Manufacturing Same	Jun Young Yang
09/687,126	Method of and Apparatus for Manufacturing Semiconductor Packages	Hyung Ju Lee
09/687,493	Semiconductor Package Having Improved Adhesiveness and Ground Bonding	Sung Sik Jang
09/687,541	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung

It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. While the print coating supply system for a plurality of coating substances shown is described as being preferred, it will be obvious to a person of ordinary skill in the art that various changes and modifications may be made therein without departing from the spirit and the scope of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners and a perimeter;

a leadframe having a plurality of tie bars having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, each of said plurality of leads having a side surface, a generally planar bottom surface and a half-etched section facing said chip paddle, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip;

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of leads in spaced relation to said side surface thereof.

2. The semiconductor package of claim 1, wherein at least one depression is formed on said bottom surface of said chip paddle.

3. The semiconductor package of claim 1, wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars.

4. The semiconductor package of claim 1, wherein said chip paddle has a half-etched section at a lower edge of said chip paddle along said chip paddle perimeter.

5. The semiconductor package of claim 1, wherein said bond pads are electrically connected to said semiconductor chip.

6. The semiconductor package of claim 1, wherein each of said plurality of leads has a half-etched section facing said chip paddle; leadframe with space for receiving semiconductor chip; semiconductor chip secured to said space;

7. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a generally planar bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners and a perimeter;

a leadframe having a plurality of tie bars having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, each of said plurality of leads having a side surface, a bottom surface and a half-etched section facing said chip paddle, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of said chip paddle in spaced relation to said side surface thereof.

8. The semiconductor package of claim 7, wherein at least one of said plurality of leads has at least one depression formed on said bottom surface of the respective said plurality of leads.

9. The semiconductor package of claim 7, wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars.

10. The semiconductor package of claim 7, wherein said chip paddle has a half-etched section at a lower edge of said chip paddle along said chip paddle perimeter.

11. The semiconductor package of claim 7, wherein said bond pads are electrically connected to said semiconductor chip.

12. The semiconductor package of claim 7, wherein each of said plurality of leads has a half-etched section facing said chip paddle.

13. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners and a perimeter;

a leadframe having a plurality of tie bars having a side surface and a generally planar bottom surface, each of said plurality of tie bars being connected to said corners of

said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, each of said plurality of leads having a side surface, a bottom surface and a half-etched section facing said chip paddle, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip;

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars in spaced relation to said surface thereof.

14. The semiconductor package of claim 13, wherein at least one depression is formed on said bottom surface of said chip paddle.

15. The semiconductor package of claim 13, wherein at least one of said plurality of leads has at least one depression formed on said bottom surface of the respective said plurality of leads.

16. The semiconductor package of claim 13, wherein said chip paddle has a half-etched section at a lower edge of said chip paddle along said chip paddle perimeter.

17. The semiconductor package of claim 13, wherein said bond pads are electrically connected to said semiconductor chip.

18. The semiconductor package of claim 13, wherein each of said plurality of leads has a half-etched section facing said chip paddle.

19. A semiconductor package comprising:

a leadframe having a plurality of tie bars having a side surface and a generally planar bottom surface, a chip paddle having a top surface, a side surface and a bottom surface, corners and a perimeter, said chip paddle having a space adapted to receive a semiconductor chip, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, each of said plurality of leads having a side surface, a bottom surface and a half-etched section facing said chip paddle, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars in spaced relation to said bottom surface thereof.

20. The semiconductor package of claim 19, further comprising:

a semiconductor chip having an upper surface and a bottom surface, said semiconductor chip being secured to said space on said leadframe by an adhesive;

a plurality of bond pads on said upper surface of said semiconductor chip;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe.

21. The semiconductor package of claim 20, wherein at least one depression is formed on said bottom surface of said chip paddle.

22. The semiconductor package of claim 20, wherein at least one of said plurality of leads has at least one depression formed on said bottom surface of the respective said plurality of leads.

23. The semiconductor package of claim 20, wherein said chip paddle has a half-etched section at a lower edge of said chip paddle along said chip paddle perimeter.

24. The semiconductor package of claim 20, wherein said bond pads are electrically connected to said semiconductor chip.

25. The semiconductor package of claim 20, wherein each of said plurality of leads has a half-etched section facing said chip paddle.

26. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a generally planar bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners and a perimeter;

a leadframe having a plurality of tie bars having a side surface and a generally planar bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, each of said plurality of leads having a side surface, a generally planar bottom surface and a half-etched section facing said chip paddle, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip;

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces;

wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars in spaced relation to said side surface thereof;

wherein at least one depression is formed on said bottom surface of said chip paddle in spaced relation to said side surface thereof; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of leads in spaced relation to said side surface thereof.

27. The semiconductor package of claim 26, wherein said chip paddle has a half-etched section at a lower edge of said chip paddle along said chip paddle perimeter.

28. The semiconductor package of claim 26, wherein said bond pads are electrically connected to said semiconductor chip.

29. The semiconductor package of claim 26, wherein each of said plurality of leads has a half-etched section facing said chip paddle.

30. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners, a perimeter and a half-etched section at a lower edge of said chip paddle along said perimeter;

a leadframe having a plurality of tie bars having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, said plurality of leads having a side surface and a generally planar bottom surface, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip;

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of leads in spaced relation to said side surface thereof.

31. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a generally planar bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners, a perimeter and a half-etched section at a lower edge of said chip paddle along said perimeter;

a leadframe having a plurality of tie bars having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, said plurality of leads having a side surface and a bottom surface, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of said chip paddle in spaced relation to said side surface thereof.

32. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an

adhesive, said chip paddle having corners, a perimeter and a half-etched section at a lower edge of said chip paddle along said perimeter;

a leadframe having a plurality of tie bars having a side surface and a generally planar bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, said plurality of leads having a side surface and a bottom surface, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip;

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars in spaced relation to said side surface thereof.

33. A semiconductor package comprising:

a leadframe having a plurality of tie bars having a side surface and a generally planar bottom surface, a chip paddle having a top surface, a side surface, a bottom surface, corners, a perimeter and a half-etched section at a lower edge of said chip paddle along said perimeter, said chip paddle having a space adapted to receive a semiconductor chip, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, said plurality of leads having a side surface and a bottom surface, said plurality of leads being radially

formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars in spaced relation to said bottom surface thereof.

34. A semiconductor package comprising:

a semiconductor chip having an upper surface and a bottom surface;

a plurality of bond pads on said upper surface of said semiconductor chip;

a chip paddle having a top surface, a side surface and a generally planar bottom surface, said chip paddle secured to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners, a perimeter and a half-etched section at a lower edge of said chip paddle along said perimeter;

a leadframe having a plurality of tie bars having a side surface and a generally planar bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe, each of said plurality of leads having a side surface and a generally planar bottom surface, said plurality of leads being radially formed at regular intervals along and spaced apart from said perimeter of said chip paddle and extending towards said chip paddle;

a plurality of conductive wires electrically connected to said plurality of leads and said semiconductor chip;

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of leads to form a package body, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe;

wherein said chip paddle, said plurality of leads and said plurality of tie bars are externally exposed at respective side and bottom surfaces;

wherein at least one depression is formed on said bottom surface of at least one of said plurality of tie bars in spaced relation to said side surface thereof;

wherein at least one depression is formed on said bottom surface of said chip paddle in spaced relation to said side surface thereof; and

wherein at least one depression is formed on said bottom surface of at least one of said plurality of leads in spaced relation to said side surface thereof.

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ABSTRACT OF THE DISCLOSURE

A packaged semiconductor having increased solder joint strength. The packaged semiconductor includes a semiconductor chip and a plurality of bond pads on the semiconductor chip. A leadframe includes a chip paddle, a plurality of tie bars connected to corners of the chip paddle and a plurality of dam bars. A plurality of leads connect to the leadframe, and are radially formed at regular intervals along and spaced apart from the chip paddle, and extend towards the chip paddle. A plurality of conductive wires electrically connect the leads and the semiconductor chip. Encapsulation material encapsulates the semiconductor chip, wires, chip paddle, and leads to form a package body, wherein dam bars formed on the leadframe limit flow of the encapsulation material. The chip paddle, plurality of leads and plurality of tie bars are externally exposed at peripheral side and bottom surfaces to allow depressions to be formed thereon. In one embodiment, at least one depression is formed on the bottom surface of at least one of the tie bars. In another embodiment, at least one depression is formed on the bottom surface of the chip paddle. In another embodiment, at least one of the leads has at least one depression formed on the bottom surface of the respective lead. The depressions may also be formed on the chip paddle, leads and tie bars simultaneously, or in combination to increase the friction required to readily maintain a sufficient solder joint strength when the package is mounted to a motherboard.

FIGURE 1