SEMICONDUCTOR DEVICE HAVING COMMON SOURCE LINE LAYER, ELECTRONIC SYSTEM INCLUDING THE SAME, AND RELATED METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This patent application claims priority to and the benefit of Korean Patent Application No. 10-2023-0002900 filed in the Korean Intellectual Property Office on 9 January 2023, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to a semiconductor device with a common source line layer, an electronic system including the same, and a method of manufacturing semiconductor device.

BACKGROUND

[0003] Recently, vertically stacked memory devices in which memory cells are vertically stacked on the surface of the substrate are developed. As the number of the stacked memory cells included in the vertically stacked memory devices increases, it is not easy to form the memory cells and a wire structure for connecting them.

SUMMARY

[0004] The present disclosure may provide a semiconductor device with a simple wiring structure.

[0005] The present disclosure may simplify a process for manufacturing a semiconductor device.

[0006] The present disclosure are not limited by the above-described technical object, and the scope of the present disclosure will be clearly comprehended to a person of ordinary skill in the art by the following disclosure.

[0007] An embodiment of the present disclosure provides a semiconductor device including: a cell region including: a channel structure penetrating through a plurality of word lines, and memory cells connected to the plurality of word lines and arranged in three dimensions; a cell contact region in which a cell contact plug connected to a word line of the cell region is disposed; a common source line contact region in which a common source line contact plug is disposed; an input and output contact region in which an input and output contact plug connected to a circuit of the semiconductor device is disposed; a word line cut region separating the word line of the cell region from a word line of a neighboring cell region; a common source line layer connecting the channel structure of the cell region and the common source line contact plug; and an input and output pad as an external pad of the semiconductor device connected to the input and output contact plug. The common source line layer and the input and output pad are disposed at the same vertical level. Each of the common source line layer and the input and output pad includes the same material.

[0008] Another embodiment of the present disclosure provides a method of manufacturing a semiconductor device including: forming a sacrificial layer in a trench formed in a silicon substrate; forming a memory cell structure on a cell region of the silicon substrate on which the sacrificial layer is formed; removing the silicon substrate, forming a first insulation layer to cover the sacrificial layer, and partially removing the first insulation layer to expose an upper surface of the sacrificial layer; removing the sacrificial layer; and forming a metal layer filling a space where the sacrificial layer is removed, and patterning the same. The forming of the memory cell structure includes forming a channel structure penetrating through a plurality of word lines, forming a cell contact plug connected to a word line of the plurality of word lines,

forming a common source line contact plug connected to the channel structure, forming an input and output contact plug connected to a circuit of the semiconductor device, and forming a word line cut insulator separating the plurality of word lines of the cell region from word lines of a neighboring cell region of the silicon substrate.

[0009] The semiconductor device according to an embodiment of the present disclosure may have the common source line layer made of a metal on the rear surface, thereby having simplified the wiring structure.

[0010] The method for manufacturing a semiconductor device according to an embodiment of the present disclosure may simultaneously form the input and output pad, the isolated pad of the cell contact region, and the metal common source line layer, thereby simplifying the process for manufacturing a semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 shows a layout view of a common source line layer of a semiconductor device according to an embodiment.

[0012] FIG. 2 shows a cross-sectional view of a semiconductor device with respect to a line II-II of FIG. 1 according to an embodiment.

[0013] FIGS. 3, 4, 5, 6, 7 and 8 show intermediate processes of a method for manufacturing a semiconductor device according to an embodiment.

[0014] FIG. 9 shows an intermediate process of a method for manufacturing a semiconductor device according to another embodiment.

[0015] FIG. 10 shows a data storage system including a semiconductor device according to an embodiment.

[0016] FIG. 11 shows a perspective view of a data storage system including a semiconductor device according to an embodiment.

DETAILED DESCRIPTION

[0017] The present disclosure will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure.

[0018] The drawings and the descriptions are to be considered as illustrative and not as restrictive. Throughout the specification, the same reference numbers indicate the same constituent elements.

[0019] Parts that are irrelevant to the description are omitted to clearly describe the present disclosure, and like reference numerals designate like elements throughout the specification. The thicknesses of layers, films, panels, regions, etc., are enlarged for clarity. The thicknesses of some layers and areas are exaggerated.

[0020] The singular forms are intended to include the plural forms as well, unless the context clearly indicates otherwise.

[0021] In the specification and the claims, the term "and/or" is intended to include arbitrary combinations of the terms "and" and "or" for the purposes of meaning and interpretation. For example, the expression of "A and/or B" may be understood to signify "A, B, or A and B".

[0022] In the specification and claims, the phrase "at least one of" is intended to include the meaning of "at least one selected from the group of," for the purpose of meaning and interpretation. For example, "at least one of A and B" may be understood to signify "A, B, or A and B".

[0023] Terms such as first, second, and the like will be used only to describe various constituent elements, and are not to be interpreted as limiting these constituent elements. The terms are only used to differentiate one constituent element from other constituent elements.

For example, a first constituent element could be termed a second constituent element, and similarly, a second constituent element could be termed as a first constituent element, without departing from the scope of the present disclosure.

[0024] When an element, such as a layer, a film, a region, or a substrate is described to be "above" another element, it may be directly above another element or there may be an intermediate element. In contrast, when a first element is described to be "directly above" a second element, there is no intermediate element. Throughout the specification, the term "above" a target must be "understood as being disposed above or below the target element, and does not necessarily signify "above" with respect to an opposite direction of gravity.

[0025] For example, spatially relative terms "below" or "above" may be used to facilitate the description of the relationship of one element or a constituent element to other constituent elements as shown in the drawings. The spatially relative terms are intended to include other directions in use or operation in addition to the directions shown in the drawings. For example, when the device shown in the drawing is flipped, the device disposed below another device may be disposed "above" the other device. Therefore, the exemplary term "below" may include lower and upper positions. The device may also be oriented in other directions, the spatially relative term may be analyzed differently depending on the directions.

[0026] When an element (or region, layer, portion, etc.) is described to be "connected" or "combined" to another element in the specification, it may be directly disposed, connected, or combined on the above-noted other element, or an element may be disposed therebetween.

[0027] The term "connected to" or "combined to" may include physical or electrical connections or combinations.

[0028] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the present disclosure belongs. It will be further understood that terms, such as those

defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and/or the present specification, and should not be interpreted in an idealized or overly formal sense, unless expressly so defined herein.

[0029] FIG. 1 shows a layout view of a common source line layer of a semiconductor device according to an embodiment, and FIG. 2 shows a cross-sectional view of a semiconductor device with respect to a line II-II of FIG. 1 according to an embodiment.

[0030] Referring to FIG. 1, the semiconductor device may include a cell region 1 in which memory cells are disposed in a three dimension (3D), a cell contact region 2 in which a cell contact plug and an isolated pad are disposed, a common source line contact region 3 in which a common source line contact plug is disposed, an input and output contact region 5 in which an input and output contact plug and an input and output pad are disposed, and a word line cut region 4 separating word lines of the cell region 1 from word lines of a neighboring cell region 1. The cell contact region 2 may be surrounded by the cell region 1, the common source line contact region 3, and the word line cut region 4, and the input and output contact region 5 may be disposed on one side of the common source line contact region 3.

[0031] A common source line layer 320 may be integrally formed and connected throughout the cell region 1, the common source line contact region 3, and the word line cut region 4. Respective input and output pads 17 may be disposed to be separated from each other in the input and output contact region 5, and isolated pads 15 connected to respective cell contact plugs may be disposed to be separated from each other in the cell contact region 2. The common source line layer 320, the input and output pads 17, and the isolated pads 15 may be disposed at the same vertical level. Each of the common source line layer 320, the input and output pads 17, and the isolated pads 15 may include the same material. For example, each of the common source line layer 320, the input and output pads 17, and the isolated pads 15 may

include at least one of metals such as tungsten, titanium, tantalum, platinum, cobalt, copper, or aluminum as a major component. The major component is meant the component that makes up more than half of the entire weight.

[0032] Referring to FIG. 2, the semiconductor device may have a chip to chip (C2C) structure. The semiconductor device may be a memory device. Here, the C2C structure may signify manufacturing at least one upper chip including a cell region CELL and a lower chip including a peripheral circuit region PERI, and connecting the at least one upper chip and the lower chip by a bonding method. For example, the bonding method may represent a method for electrically or physically connecting a bonding metal pattern formed on an uppermost metal layer of an upper chip and a bonding metal pattern formed on an uppermost metal layer of a lower chip. For another example, when the bonding metal patterns are made of copper (Cu), the bonding method may be a Cu-Cu bonding method. For another example, the bonding metal patterns may be made of aluminum (Al) or tungsten (W).

[0033] The memory device may include at least one upper chip including a cell region. For example, the memory device may be realized to include two upper chips. This is, however, for illustrative purposes, and the number of the upper chips is not limited thereto.

[0034] When the memory device is manufactured by the bonding method, the memory device may be manufactured by manufacturing the upper chip including a cell stack (or, a cell stack region) CELL1 and the lower chip including a peripheral circuit region PERI, and connecting the upper chip and the lower chip according to the bonding method. The upper chip may be inverted and may be connected to the lower chip by the bonding method. Hereinafter, the top and bottom of the upper chip is defined as before the upper chip is inverted. In other words, in FIG. 2, the top of the lower chip refers to the top defined in the +Z-axis direction, and the top of the upper chip refers to the top defined in the -Z-axis direction.

[0035] The peripheral circuit region PERI may include a first substrate 210 and a plurality

of circuit elements 220a, 220b, and 220c formed on the first substrate 210. An interlayer insulating layer 215 including one or more insulation layers may be provided on the circuit elements 220a, 220b, and 220c, and a plurality of metal wires for connecting the circuit elements 220a, 220b, and 220c may be provided in the interlayer insulating layer 215. For example, the metal wires may include first metal wires 230a, 230b, and 230c connected to the circuit elements 220a, 220b, and 220c, and second metal wires 240a, 240b, and 240c disposed on the first metal wires 230a, 230b, and 230c. The metal wires may be made of at least one of various conductive materials. For example, the first metal wires 230a, 230b, and 230c may be made of tungsten with relatively high electrical resistivity, and the second metal wires 240a, 240b, and 240c may be made of copper with relatively low electrical resistivity.

[0036] Although only the first metal wires 230a, 230b, and 230c and the second metal wires 240a, 240b, and 240c are shown and described herein, at least one additional metal wiring may be formed on the second metal wires 240a, 240b, and 240c. In this case, the second metal wires 240a, 240b, and 240c may be made of aluminum. At least part of the additional metal wire formed on the second metal wires 240a, 240b, and 240c may be made of copper that has lower electrical resistivity than aluminum of the second metal wires 240a, 240b, and 240c.

[0037] The interlayer insulating layer 215 may be disposed on the first substrate 210, and may include an insulating material such as a silicon oxide or a silicon nitride.

[0038] The cell stack CELL1 may include at least one memory block. The cell stack CELL1 may include a second substrate 310 and a common source line layer 320. The common source line layer 320 may be made of a metal such as tungsten, titanium, tantalum, platinum, cobalt, copper, or aluminum, and may be disposed to be inserted into the insulation layer 321. The insulation layer 321 may be formed in two layers, and may be two layers of oxide or a mixture of oxide and nitride. The input and output pads 17 of the input and output contact region 5 and the isolated pads 15 of the cell contact region 2, which are made of the same material as the

common source line layer 320, may be disposed within the insulation layer 321. The common source line layer 320, the input and output pads 17, and the isolated pads 15 may have upper portions and lower portions that have different planar shapes. For example, the common source line layer 320, the input and output pads 17, and the isolated pads 15 may have wide lower portions and narrow upper portions. The common source line layer 320 may include a lower portion integrally formed throughout the cell region 1, the common source line contact region 3, and the word line cut region 4 and an upper portion protruding at portions that correspond to a common source line contact plug 380 and channel structures CH. Cross-sectional shapes of the common source line layer 320, the input and output pads 17, and the isolated pads 15 will be described below with reference to FIG. 8.

[0039] On the second substrate 310, a plurality of word lines 330 (331-338) may be stacked along a direction perpendicular to the top surface of the second substrate 310 (z-axis direction). String selection lines and a ground selection line may be disposed above and below the word lines 330, and the word lines 330 may be disposed between the string selecting lines and the ground selecting line. In an embodiment, one of the string selection lines may be the word line 331 and the ground selection line may be the word line 338. In this case, the word lines 330 (332-337) may be disposed between the string selecting line (331) and the ground selecting line (338).

[0040] The second substrate 310 may function as a supporter of the cell stack CELL1, or it may be an insulation layer covering the common source line layer 320, the input and output pads 17, and the isolated pads 15.

[0041] The plurality of channel structures CH may be formed on the cell stack CELL1.

[0042] As shown in a region A1, the channel structures CH may extend in a direction perpendicular to an upper surface of the second substrate 310 and may penetrate through the word lines 330, the string selecting lines, and the ground selecting line. The channel structures

CH may include a data storage layer, a channel layer, and a fill insulation layer. The channel layer may be electrically connected to a first metal wire 350c and a second metal wire 360c. For example, the second metal wire 360c may be a bit line, and may be connected to the channel structures CH through the first metal wire 350c. The second metal wire 360c that is a bit line may extend in a first direction (Y-axis direction) in parallel to the upper surface of the second substrate 310.

[0043] As shown in a region A2, the channel structures CH may include a lower channel LCH and an upper channel UCH connected to each other. For example, the channel structures CH may be formed by a process for the lower channel LCH and a process for the upper channel UCH. The lower channel LCH may extend in a direction perpendicular to the upper surface of the second substrate 310 and may penetrate through the lower word lines 331 and 332. The lower channel LCH may include a data storage layer, a channel layer, and a buried insulation layer, and may be connected to the upper channel UCH. The upper channel UCH may penetrate through the upper word lines 333 to 338. The upper channel UCH may include a data storage layer, a channel layer, and a buried insulation layer, and the channel layer of the upper channel UCH may be electrically connected to the first metal wire 350c and the second metal wire 360c. As a length of the channel in the first direction increases, it may be difficult to form a channel with a constant width because of the process. The memory device according to an embodiment may have channels having improved width uniformity with a lower channel (LCH) and an upper channel (UCH) formed in a sequential process.

[0044] As shown in the region A2, when each of the channel structures CH is formed to include the lower channel LCH and the upper channel UCH, the word line disposed near a boundary of the lower channel LCH and the upper channel UCH may be a dummy word line. For example, the word line 332 and the word line 333 forming the boundary of the lower channel LCH and the upper channel UCH may be dummy word lines. In this case, no data

may be stored in the memory cells connected to the dummy word line. In another way, the number of pages that correspond to the memory cells connected to the dummy word line may be less than the number of pages that correspond to the memory cells connected to a general (or, a normal) word line. A voltage level applied to the dummy word line may be different from a voltage level applied to the general word line, thereby reducing effects given by the non-uniform channel width between the lower channel LCH and the upper channel UCH to the operation of the memory device.

[0045] It is shown in the region A2 that the number of the lower word lines 331 and 332 penetrated by the lower channel LCH is less than the number of the upper word lines 333 to 338 penetrated by the upper channel UCH. However, the present disclosure is not limited thereto, for example, the number of the lower word lines penetrating the lower channel LCH may be equal to or greater than the number of the upper word lines penetrated by the upper channel UCH.

[0046] An upper metal pattern 252 may be formed in an uppermost metal layer of the peripheral circuit region PERI of the upper portion of the channel structures CH, and an upper metal pattern 392 having the same shape as the upper metal pattern 252 may be formed in the uppermost metal layer of the cell stack CELL1. The upper metal pattern 392 of the cell stack CELL1 may be electrically connected to the upper metal pattern 252 of the peripheral circuit region PERI by a bonding method. The bit line 360c may be electrically connected to a page buffer included in the peripheral circuit region PERI. For example, some of the circuit elements 220c of the peripheral circuit region PERI may provide the page buffer.

[0047] Referring to FIG. 2, the word lines 330 of the cell stack CELL1 may extend in the second direction (X-axis direction) parallel to the upper surface of the second substrate 310, and may be connected to a plurality of cell contact plugs 340 (341 to 347). A first metal wire 350b and a second metal wire 360b may be sequentially connected to upper portions of the cell

contact plugs 340 connected to the word lines 330. The cell contact plugs 340 may be connected to the peripheral circuit region PERI through an upper bonding metal 370b of the cell stack CELL1 and an upper bonding metal 270b of the peripheral circuit region PERI.

[0048] The isolated pads 15 made of the same material as the common source line layer 320 may be connected to the lower portion of the cell contact plugs 340.

[0049] The cell contact plugs 340 may be electrically connected to a row decoder included in the peripheral circuit region PERI. For example, some of the circuit elements 220b of the peripheral circuit region PERI provide the row decoder, and the cell contact plugs 340 may be electrically connected to the circuit elements 220b for providing the row decoder through the upper bonding metal 370b of the cell stack CELL1 and the upper bonding metal 270b of the peripheral circuit region PERI.

[0050] The upper bonding metal 370b may be formed on the cell stack CELL1 in the cell contact region 2, and the upper bonding metal 270b may be formed in the peripheral circuit region PERI. The upper bonding metal 370b of the cell stack CELL1 may be electrically connect to the upper bonding metal 270b of the peripheral circuit region PERI by a bonding method. The upper bonding metal 370b and the upper bonding metal 270b may be made of aluminum, copper, or tungsten.

[0051] An upper metal pattern 372a may be formed on the upper portion of the cell stack CELL1, and an upper metal pattern 272a may be formed on the upper portion of the peripheral circuit region PERI in the input and output contact region 5. The upper metal pattern 372a of the cell stack CELL1 may be connected to the upper metal pattern 272a of the peripheral circuit region PERI by a bonding method.

[0052] The common source line contact plugs 380 may be disposed in the common source line contact region 3. The common source line contact plugs 380 may be made of a conductive material such as a metal, a metal compound, or doped polysilicon. The common source line

contact plug 380 may be electrically connected to the common source line layer 320. A first metal wire 350a and a second metal wire 360a may be sequentially stacked on the upper portion of the common source line contact plug 380.

[0053] External pads 205, 305, and 306 may be disposed in the input and output contact region 5 and the common source line contact region 3. Referring to FIG. 2, a lower insulation layer 201 may cover the lower surface of the first substrate 210, and a first external pad 205 may be formed on the lower insulation layer 201. The first external pad 205 may be connected to at least one of the circuit elements 220a disposed in the peripheral circuit region PERI through a first input and output contact plug 203, and may be separated from the first substrate 210 by the lower insulation layer 201. A lateral insulation layer may be disposed between the first input and output contact plug 203 and the first substrate 210 to electrically separate the first input and output contact plug 203 from the first substrate 210.

[0054] A second external pad 305 and/or a third external pad 306 may be disposed on the upper portion of the second substrate 310. The second external pad 305 may be connected to at least one of the circuit elements 220a disposed in the peripheral circuit region PERI through a first substrate plug 307, the input and output pad 17, and a second input and output contact plug 303, and the third external pad 306 may be connected to at least one of the circuit elements 220a disposed in the peripheral circuit region PERI through a second substrate plug 308, the input and output pad 17, and a third input and output contact plug 304.

[0055] Depending on embodiments, the first to third external pads 205, 305, and 306 may be selectively formed. For example, the memory device may be realized to include only the first external pad 205 disposed on the upper portion of the first substrate 210 or include only the second external pad 305 or the third external pad 306 disposed on the upper portion of the second substrate 310.

[0056] Depending on embodiments, the second substrate 310 may be omitted, and the input

and output pad 17 may function as an external pad.

[0057] FIG. 3 to FIG. 8 show a method for manufacturing a semiconductor device according to an embodiment.

[0058] For better comprehension and ease of explanation, in FIGS. 3 through 8, metal wires and bonding metals on top of the channel structure (CH), which are not directly related to the content of the embodiment, are simplified and shown as one layer (superstructure layer 30), and the peripheral circuit region (PERI) is simplified and shown as one block (peripheral circuit block 40). That is, the portion in which the first metal wires 350a, 350b, 350c, second metal wires 360a, 360b, 360c, upper bonding metals 370a and 370b, upper metal patterns 372a and 392, and the like of FIG. 2 are formed is simplified to the superstructure layer 30, and the peripheral circuit region (PERI) is simplified to the peripheral circuit block 40. One 303 of the second and third input and output contact plugs 303 and 304, the common source line contact plug 380, two (346 and 347) of the cell contact plugs 340, the channel structure 13, and word line cut insulators 12 and 14 relating to the content of an embodiment are shown from among the many constituent elements of FIG. 2.

[0059] Referring to FIG. 3, a trench is formed on the silicon substrate 10 and the trench is filled with an aluminum oxide (AlO) to form a sacrificial layer 11. The silicon substrate 10 may be a silicon monocrystalline wafer or a polysilicon layer formed on a semiconductor wafer.

[0060] A word line interlayer insulating layer 25 and a sacrificial insulation layer are alternately stacked on the silicon substrate 10 on which the sacrificial layer 11 may be formed to form a preliminary stacking structure, and the preliminary stacking structure may be patterned according to photolithography and a trim process to thus form a stair structure in the cell contact region 2. An interlayer insulating layer 20 may be formed on the preliminary stacking structure and may be planarized, and the channel structure 13 penetrating the preliminary stacking structure and the interlayer insulating layer 20 may be formed. Openings

penetrating the preliminary stacking structure and the interlayer insulating layer 20 are formed, and the sacrificial insulation layer is removed and the conductive material is filled through the openings to form the word lines 330. The openings may include an opening to be filled with the word line cut insulators 12 and 14 and an opening to be filled with the cell contact plug 340, the common source line contact plug 380, and the input and output contact plug 303. Word line cut insulators 12 and 14, a cell contact plug 340, a common source line contact plug 380, and an input and output contact plug 303 filling the opening may be formed. Formation of the cell contact plug 340, the common source line contact plug 380, and the input and output contact plug 303 may include removing the sacrificial layer and filling the conductive material. Lower ends of the channel structures 13, the cell contact plug 340, the common source line contact plug 380, and the input and output contact plug 303 may be disposed in the sacrificial layer 11. FIG. 2 and FIG. 3 show that the word line cut insulators 12 and 14 have a boundary separated from the interlayer insulating layer 20 or the insulation layer 25, and depending on embodiments, the word line cut insulators 12 and 14, the interlayer insulating layer 20, and the insulation layer 25 may be made of the same material, and the boundary among them may not be formed.

[0061] Referring to FIG. 2 and FIG. 3, the superstructure layer 30 including the first metal wires 350a, 350b and 350c, the second metal wires 360a, 360b and 360c, the upper bonding metals 370a and 370b, and the upper metal patterns 372a and 392, and the interlayer insulating layer insulating the same, may be formed.

[0062] Fabrication of these memory cell structures may be accomplished by a variety of known methods to fabricate vertical memory devices, of which detailed descriptions will be omitted. For example, the method disclosed in Korean Patent Application Publication No. 10-2020-0036503 may be applied.

[0063] Referring to FIG. 4, the memory cell structure of FIG. 3 may be inverted and may

be connected to the peripheral circuit block 40 by a bonding method.

[0064] Referring to FIG. 5, the silicon substrate 10 is etched and removed, the oxide layer or the nitride layer is deposited to form an insulation layer 21, and a chemical mechanical polishing (CMP) process on the insulation layer 21 is progressed to thus expose the sacrificial layer 11. In this instance, the sacrificial layer 11 may be used as a stopping layer of the chemical mechanical polishing.

[0065] Referring to FIG. 6, the exposed sacrificial layer 11 is removed. Removal of the sacrificial layer 11 may include a dry etching process. An ONO (oxide layer 505/nitride layer 504/oxide layer 503) layer on the lower portion of the channel structure 13 exposed by removing the sacrificial layer 11 may be removed to expose a polysilicon layer 502 of the channel structure 13, and form a silicide at a surface of the exposed polysilicon layer 502. The silicide may be a nickel silicide.

[0066] Referring to FIG. 7, a metal layer 320' is formed to fill the space from which the sacrificial layer 11 is removed. The metal layer 320' may, for example, include a metal with low electrical resistance, such as tungsten, titanium, tantalum, platinum, cobalt, copper, or aluminum.

[0067] Referring to FIG. 8, the metal layer 320' may be patterned to form the common source line layer 320, the isolated pads 15, and the input and output pads 17, and a space among the common source line layer 320, the isolated pad 15, and the input and output pad 17 may be filled with an insulation layer 23. Patterning of the metal layer 320' may include a photolithography process. The insulation layer 23 may include a silicon oxide or a silicon nitride. Formation of the insulation layer 23 may include depositing an insulation layer, etching back, CMP, or a photolithography process. Depending on embodiments, the process for forming an insulation layer 23 may be omitted.

[0068] Referring to FIG. 1 and FIG. 8, the common source line layer 320 may be integrally

formed and electrically connected across the cell region 1, the common source line contact region 3, and the word line cut region 4. For example, the common source line layer 320 connected to the common source line contact plug 380 may be connected to the common source line layer 320 connected to the channel structure 13 through the common source line layer 320 of the word line cut region 4.

[0069] Referring to FIG. 8, each of the common source line layer 320, isolation pads 15, and input and output pads 17 may include a first portion filling the area where the sacrificial layer 11 is removed and a second portion formed over the first portion. The first portion may contact the common source line contact plug 380, the channel structure 13, the cell contact plugs 346 and 347, and the input and output contact plug 303, and the second portion may function as a wire for connecting between the common source line layer 320 connected to the common source line contact plug 380 and the common source line layer 320 connected to the channel structure 13. The term "contact" as used herein refers to a direct connection, e.g., touching. The first portion may have a horizontal cross-sectional area that is widest where it abuts the interlayer insulation membrane 20 and narrows as it approaches the second portion. The second portion may have a horizontal cross-sectional area that is widest where it abuts the first portion and narrows as it goes away from the first portion.

[0070] Referring again to FIG. 2, the second substrate 310 covering the common source line layer 320, the isolated pads 15, and the input and output pads 17 may be formed by adhering a substrate or depositing an insulation layer, and the external pads 305 and 306 may be formed on the second substrate 310, thereby the memory device according to an embodiment being manufactured.

[0071] By the above described method, the common source line layer 320, the isolated pads 15, and the input and output pads 17 may be formed together with a metal.

[0072] FIG. 9 shows a method for manufacturing a semiconductor device according to

another embodiment.

[0073] Referring to FIG. 9, a dual damascene process may be applied as a substitute of the process described with reference to FIG. 7 and FIG. 8. For example, after the process shown in FIG. 6 being performed, the pattern of the insulation layer 23 is formed, a barrier metal is deposited, the metal layer of copper may be conformally formed by electroplating and may be planarized by CMP, thereby forming the common source line layer 320, the isolated pads 15, and the input and output pads 17 as shown in FIG. 9.

[0074] Referring to FIG. 9, the common source line layer 320, the isolated pads 15, and the input and output pads 17 may include a first portion filling a space where the sacrificial layer 11 is removed and a second portion formed on the first portion. The second portion may function as a wire for connecting between the common source line layer 320 connected to the common source line contact plug 380 and the common source line layer 320 connected to the channel structure 13. The first portion may have a horizontal cross-sectional area that is widest where it abuts the interlayer insulation layer 20 and narrows as it approaches the second portion. The second portion may have a horizontal cross-sectional area that is narrowest where it abuts the first portion and widens as it goes away from the first portion.

[0075] As described above, according to an embodiment, the common source line layer 320, the isolated pads 15, and the input and output pads 17 may be formed together, and the common source line layer 320 may be made of a metal, thereby simplifying the structure of the semiconductor device and the manufacturing process.

[0076] FIG. 10 shows a data storage system including a semiconductor device according to an embodiment.

[0077] Referring to FIG. 10, the data storage system 1000 may include a semiconductor device 1100 and a controller 1200 electrically connected to the semiconductor device 1100. The data storage system 1000 may be a storage device including one or multiple semiconductor

devices 1100 or an electronic device including a storage device. For example, the data storage system 1000 may be a solid state drive (SSD) device, a universal serial bus (USB) device, a computing system, a medical device, or a communication device including one or multiple semiconductor devices 1100.

[0078] The semiconductor device 1100 may be a non-volatile memory device, for example, the memory device described with reference to FIG. 1 to FIG. 9. The semiconductor device 1100 may include a first semiconductor structure 1100F and a second semiconductor structure 1100S disposed on the first semiconductor structure 1100F. The first semiconductor structure 1100F and the second semiconductor structure 1100S may correspond to the lower chip and the upper chip of FIG. 2, respectively. The first semiconductor structure 1100F may be a peripheral circuit structure including a decoder circuit 1110, a page buffer 1120, and a logic circuit 1130. The second semiconductor structure 1100S may be a memory cell structure including a bit line BL, a common source line CSL, word lines WL, first and second gate upper lines UL1 and UL2, first and second gate lower lines LL1 and LL2, and memory cell strings CSTR between the bit line BL and the common source line CSL.

[0079] Regarding the second semiconductor structure 1100S, the respective memory cell strings CSTR may include lower transistors LT1 and LT2 disposed near the common source line CSL, upper transistors UT1 and UT2 disposed near the bit line BL, and memory cell transistors MCT disposed between the lower transistors LT1 and LT2 and the upper transistors UT1 and UT2. The number of the lower portion transistors LT1 and LT2 and the number of the upper transistors UT1 and UT2 are modifiable in many ways depending on embodiments.

[0080] In the embodiments, the upper transistors UT1 and UT2 may include string selecting transistors, and the lower transistors LT1 and LT2 may include ground selecting transistors. The gate lower lines LL1 and LL2 may be gate electrodes of the lower transistors LT1 and LT2. The word lines WL may be gate electrodes of the memory cell transistors MCT, and the gate

upper lines UL1 and UL2 may be gate electrodes of the upper transistors UT1 and UT2.

[0081] The lower transistors LT1 and LT2 may include a lower erase controlling transistor LT1 and a ground selecting transistor LT2 connected in series. The upper transistors UT1 and UT2 may include a string selecting transistor UT1 and an upper erase controlling transistor UT2 connected in series. At least one of the lower erase controlling transistor LT1 and the upper erase controlling transistor UT2 may be used in an erase operation for erasing data stored in the memory cell transistors MCT by using a GIDL phenomenon.

[0082] The common source line CSL, the first and second gate lower lines LL1 and LL2, the word lines WL, and the first and second gate upper lines UL1 and UL2 may be electrically connected to the decoder circuit 1110 through first connection wires 1115 extending to the second semiconductor structure 1100S from the first semiconductor structure 1100F. The first connection wires 1115 may correspond to the cell contact plugs 340, the first metal wires 230b and 350b, the second metal wires 240b and 360b, the upper bonding metals 270b and 370b of FIG. 2. The bit lines BL may be electrically connected to the page buffer 1120 through second connection wires 1125 extending to the second semiconductor structure 1100S from the first semiconductor structure 1100F.

[0083] The first semiconductor structure 1100F, the decoder circuit 1110, and the page buffer 1120 may perform a control operation on at least one of the memory cell transistors MCT. The decoder circuit 1110 and the page buffer 1120 may be controlled by the logic circuit 1130. The semiconductor device 1100 may communicate with the controller 1200 through an input and output pad 1101 electrically connected to the logic circuit 1130. The input and output pad 1101 may correspond to the input and output pad 17 of FIG. 2. The input and output pad 1101 may be electrically connected to the logic circuit 1130 through an input and output connection wire 1135 extending to the second semiconductor structure 1100S from the first semiconductor structure 1100F. The input and output connection wire 1135 may correspond

to the second input and output contact plug 303 or the third input and output contact plug 304, and the upper metal patterns 272a and 372a of FIG. 2.

[0084] The controller 1200 may include a processor 1210, a NAND controller 1220, and a host interface 1230. Depending on embodiments, the data storage system 1000 may include a plurality of semiconductor devices 1100, and in this case, the controller 1200 may control the semiconductor devices 1100.

[0085] The processor 1210 may control an entire operation of the data storage system 1000 including the controller 1200. The processor 1210 may be operable according to predetermined firmware, and may control the NAND controller 1220 to access the semiconductor device 1100. The NAND controller 1220 may include a NAND interface 1221 for processing communication with the semiconductor device 1100. Control instructions for controlling the semiconductor device 1100, data to be written to the memory cell transistors MCT of the semiconductor device 1100, and data to be read from the memory cell transistors MCT of the semiconductor device 1100 may be transmitted through the NAND interface 1221. The host interface 1230 may provide a communication function between the data storage system 1000 and an external host. When receiving the control instruction from the external host through the host interface 1230, the processor 1210 may control the semiconductor device 1100 in response to the control instruction.

[0086] FIG. 11 shows a perspective view of a data storage system including a semiconductor device according to an embodiment.

[0087] Referring to FIG. 11, the data storage system 2000 may include a main substrate 2001, a controller 2002, at least one semiconductor package 2003, and a DRAM 2004, which are provided on the main substrate 2001. The semiconductor package 2003 and the DRAM 2004 may be connected to the controller 2002 by wire patterns 2005 formed on the main substrate 2001.

[0088] The main substrate 2001 may include a connector 2006 including pins for coupling with an external host. The number of the pins of the connector 2006 and the disposition thereof may be changed depending on the communication interface between the data storage system 2000 and the external host. The data storage system 2000 may communicate with the external host with one of the interfaces such as a universal serial bus (USB), a peripheral component interconnect express (PCI-Express), a serial advanced technology attachment (SATA), or an M-PHY for a universal flash storage (UFS). The data storage system 2000 may be operated by a power voltage supplied by the external host through the connector 2006. The data storage system 2000 may further include a power management integrated circuit (PMIC) for providing the power voltage supplied by the external host to the controller 2002 and the semiconductor package 2003.

[0089] The controller 2002 may write data to the semiconductor package 2003, may read data from the semiconductor package 2003, and may increase an operation rate of the data storage system 2000.

[0090] The DRAM 2004 may be a buffer memory for reducing a speed difference between the semiconductor package 2003 that is a data storage space and the external host. The DRAM 2004 included in the data storage system 2000 may work as a cache memory, and may provide a space for temporarily storing data in an operation for controlling the semiconductor package 2003. When the data storage system 2000 includes the DRAM 2004, the controller 2002 may further include a DRAM controller for controlling the DRAM 2004 in addition to the NAND controller for controlling the semiconductor package 2003.

[0091] The semiconductor package 2003 may include first and second semiconductor packages 2003a and 2003b spaced from each other. The first and second semiconductor packages 2003a and 2003b may respectively include a plurality of semiconductor chips 2200. The first and second semiconductor packages 2003a and 2003b may respectively include a

package substrate 2100, semiconductor chips 2200 disposed on the package substrate 2100, adhesive layers 2300 disposed at bottom surfaces of the semiconductor chips 2200, a connection structure 2400 for electrically connecting the semiconductor chips 2200 and the package substrate 2100, and a molding layer 2500 for covering the semiconductor chips 2200 and the connection structure 2400 on the package substrate 2100.

[0092] The package substrate 2100 may be a flexible printed circuit (FPC) including package upper pads 2130. The respective semiconductor chips 2200 may include an input and output pad 2210. The input and output pad 2210 may correspond to the input and output pad 1101 of FIG. 10. The respective semiconductor chips 2200 may include gate stacking structures 3210 and channel structures 3220. The respective semiconductor chips 2200 may include the semiconductor device described with reference to FIG. 1 to FIG. 9.

[0093] The connection structure 2400 may be a bonding wire for electrically connecting the input and output pad 2210 and the package upper pads 2130. Therefore, regarding the first and second semiconductor packages 2003a and 2003b, the semiconductor chips 2200 may be electrically connected to each other by a bonding wire, and may be electrically connected to the package upper pads 2130 of the package substrate 2100. The semiconductor chips 2200 may be electrically connected to each other by the connection structure including a through substrate via (e.g., a through silicon via (TSV)) instead of the connection structure 2400 based on the bonding wire method. In example embodiments, the semiconductor chips 2200 may be electrically connected to each other by the connection structure including the TSV and the connection structure 2400.

[0094] The controller 2002 and the semiconductor chips 2200 may be included in one package. Depending on embodiments, the controller 2002 and the semiconductor chips 2200 may be mounted on an interposer substrate that is not the main substrate 2001, and the controller 2002 may be connected to the semiconductor chips 2200 by the wire formed on the

interposer substrate.

[0095] While this disclosure has been described in connection with what is presently considered to be practical embodiments, it is to be understood that the disclosure is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a cell region including:

a channel structure penetrating through word lines, and

memory cells connected to the word lines and arranged in three dimensions;

a cell contact region in which a cell contact plug connected to a word line of the cell region is disposed;

a common source line contact region in which a common source line contact plug is disposed;

an input and output contact region in which an input and output contact plug connected to a circuit of the semiconductor device is disposed;

a word line cut region separating the word lines of the cell region from word lines of a neighboring cell region;

a common source line layer connecting the channel structure of the cell region and the common source line contact plug; and

an input and output pad as an external pad of the semiconductor device connected to the input and output contact plug,

wherein the common source line layer and the input and output pad are disposed at the same vertical level, and

wherein each of the common source line layer and the input and output pad includes the same material.

2. The semiconductor device of claim 1, further comprising:

an isolated pad disposed in the cell contact region and connected to the cell contact plug,

wherein the isolated pad is disposed at the same vertical level as the common source line layer, and

wherein each of the isolated pad and the common source line layer includes the same material.

3. The semiconductor device of claim 2, wherein the common source line layer includes a metal as a major component.

4. The semiconductor device of claim 2 or claim 3, wherein the common source line layer is disposed across the cell region, the common source line contact region, and the word line cut region, and is integrally formed.

5. The semiconductor device of any one of claims 2 to 4, wherein the common source line layer, the input and output pad, and the isolated pad are embedded in an insulation layer.

6. The semiconductor device of claim 5, wherein the insulation layer includes an upper layer and a lower layer formed of the same material as or a different material from the upper layer.

7. The semiconductor device of any one of claims 2 to 6, wherein:

each of the common source line layer, the isolated pad, and the input and output pad includes a first portion contacting the channel structure, the common source line contact plug, the cell contact plug, and the input and output contact plug, and a second portion disposed on the first portion,

the first portion has a horizontal cross-sectional area that is widest where it abuts the

channel structure, the common source line contact plug, the cell contact plug, and the input and output contact plug, and that narrows as it approaches the second portion, and

the second portion has a horizontal cross-sectional area that is widest where it abuts the first portion and narrows as it goes away from the first portion.

8. The semiconductor device of any one of claims 2 to 6, wherein:

each of the common source line layer, the isolated pad, and the input and output pad includes a first portion contacting the channel structure, the common source line contact plug, the cell contact plug, and the input and output contact plug, and a second portion disposed on the first portion,

the first portion has a horizontal cross-sectional area that is widest where it abuts the channel structure, the common source line contact plug, the cell contact plug, and the input and output contact plug, and that narrows as it approaches the second portion, and

the second portion has a horizontal cross-sectional area that is narrowest where it abuts the first portion and widens as it goes away from the first portion.

9. A method of manufacturing a semiconductor device, the method comprising:

forming a sacrificial layer in a trench formed in a silicon substrate;

forming a memory cell structure on a cell region of the silicon substrate in which the sacrificial layer is formed;

removing the silicon substrate, forming a first insulation layer to cover the sacrificial layer, and partially removing the first insulation layer to expose an upper surface of the sacrificial layer;

removing the sacrificial layer; and

forming a metal layer filling a space where the sacrificial layer is removed, and

patterning the metal layer,

wherein the forming of the memory cell structure includes:

forming a channel structure penetrating through a plurality of word lines,

forming a cell contact plug connected to a word line of the plurality of word lines,

forming a common source line contact plug connected to the channel structure,

forming an input and output contact plug connected to a circuit of the semiconductor device, and

forming a word line cut insulator separating the plurality of word lines of the cell region from word lines of a neighboring cell region of the silicon substrate.

10. The method of claim 9, wherein the forming and patterning of the metal layer includes:

forming a common source line layer connected to the channel structure and the common source line contact plug,

forming an input and output pad as an external pad of the semiconductor device connected to the input and output contact plug, and

forming an isolated pad connected to the cell contact plug.