SEMICONDUCTOR CONSTRUCTIONS, NAND UNIT CELLS, METHODS OF FORMING SEMICONDUCTOR CONSTRUCTIONS, AND METHODS OF FORMING NAND UNIT CELLS

ABSTRACT

Some embodiments include methods of forming semiconductor constructions Alternating layers of n-type doped material and p-type doped material may be formed The alternating layers may be patterned into a plurality of vertical columns that are spaced from one another by openings The openings may be lined with tunnel dielectric, charge-storage material and blocking dielectric Alternating layers of insulative material and conductive control gate material may be formed within the lined openings Some embodiments include methods of forming NAND unit cells Columns of alternating n-type material and p-type material may be formed The columns may be lined with a layer of tunnel dielectric, a layer of charge-storage material, and a layer of blocking dielectric Alternating layers of insulative material and conductive control gate material may be formed between the lined columns Some embodiments include semiconductor constructions, and some embodiments include NAND unit cells.

FIGURE 11