Description

This invention relates to a display controller capable of driving either of a CRT display unit and liquid crystal display unit.

A visual display unit is an indispensable terminal device for a computer system such as a personal computer and an office computer. Until recently, CRT (cathode-ray tube) display units were used in most of the computer systems as such terminal devices, however, the recent advance in the liquid crystal display technology made it possible to use liquid crystal display units as the terminal devices of computer systems particularly of portable type.

There has been proposed a display controller formed in an LSI device which can drive a display unit in accordance with commands fed from a central processing unit connected thereto. For example, a μPD3301 manufactured by Nippon Electric Co., Ltd. and an HD46505 manufactured by Hitachi, Ltd. can control CRT display units, and a μPD72030G manufactured by Nippon Electric Co., Ltd. and an HD61830 manufactured by Hitachi, Ltd. can control liquid crystal units.

EP-A-0 066 983 discloses a video signal display control apparatus providing the display control functions for both CRT-type display devices and LCD-type or similar display devices to be attached as output display units to an external micro-computer or other control system that provides output video signals.

However this apparatus for controlling the display of video signal information includes two separate display controllers, namely one for controlling the LCD-display and one for controlling the display of a home-use television or similar display. The use of the two completely separate display controllers causes the apparatus of the prior art to be expensive.

A commercially available liquid crystal display unit is generally composed of two (upper and lower) screens which are independently driven, while a CRT display unit can be driven as one screen. Thus, a CRT display unit and a liquid crystal display unit must be driven in different manners from each other. Also the manner of reading data from the video memory for a CRT display unit is different from that for a liquid crystal display unit. For this reason, each of the aforesaid conventional display controllers is designed so as to drive only one of the two kinds of display units. As a result, when it is desired to change the display unit used to another display unit of a different type, not only the display controller but also the control program therefore must be changed.

It is the object of the present invention to provide a display controller which can drive either of a CRT display unit and a liquid crystal display unit, which can be controlled by the same program executed by a central processing unit irrespective of the kind of the display unit connected thereto.

According to the present invention there is provided a display controller capable of selectively driving one of first and second display units, the first display unit having a display screen comprised of a scanning-type screen which provides M rows of N columns of display positions thereon, the second display unit having a display screen constituted by upper and lower scanning-type screens each of which provides P rows of Q columns of display positions thereon, the display controller being further connected to memory means having a plurality of addresses each for storing display data relating to an image of be displayed in a respective one of the display positions of the selected display unit, said display controller comprising:

(a) display unit designating means for designating one of the first and second display units, said designation means outputting a first designation signal when the first display unit is selected, and outputting a second designation signal when the second display unit is selected; characterized by

(b) timing signal generating means 65 responsive to said first designation signal for generating synchronization signals to be supplied to the first display unit for scanning the screen thereof, said timing signal generating means being further responsive to said second designation signal to generate synchronization signals to be supplied to the second display unit for scanning the upper and lower screens thereof;

(c) address data generating means responsive to said first designation signal for generating a first series of address data representative of the addresses of the memory means to sequentially output said generated address data to the memory means in accordance with the scanning of the display screen of the first display unit, said address data generating means being further responsive to said second designation signal for generating a second series of address data representative of those of the address of the memory means corresponding to the upper screen and a third series of address data representative of those of the addresses of the memory means corresponding to the lower screen, said address data generating means alternately outputting each of said second series of address data and each of said third series of address data to the memory means in accordance with the scannings of the upper and lower screens; and

(d) display signal generating means responsive to said first designation signal for generating a first display signal to be supplied to the first display unit based on data read from the memory means in accordance with said first series of address data, said display signal generating means being further responsive to said second designation signal to generate second and third display signals to be supplied to the second display unit based on data read from the memory means in accordance with said second and third series of address data, said second and third display signals being used to display images on the upper and lower screens, respectively.

Examples of the present invention will now be described with reference to the accompanying drawings, in which:-

Fig. 1 is a block diagram of a display system in which a display controller 1 provided in accordance with the present invention is used;

Fig. 2 is an illustration showing the video memory 4 of the display system of Fig. 1;

Fig. 3 is an illustration showing data to be written into the video memory 4 of Fig. 2;

Fig. 4 is an illustration showing the display screen;

Fig. 5 is a block diagram of the liquid crystal display unit 3 of the display system of Fig. 1;

Fig. 6 is a block diagram of the display controller 1 of the display system of Fig. 1;

Fig. 7 is a block diagram of the address generating circuit 21 of the display controller 1 of Fig. 6;

Fig. 8 is a timing chart showing the operation of the gray-scale display circuit 37 of the display controller 1 of Fig. 6;

Fig. 9 is a block diagram of one example of the gray-scale display circuit 37 of the display controller 1 of Fig. 6;

Fig. 10 is an illustration showing the waveforms of the clock pulses ϕ_0 to ϕ_2;

Figs. 11 to 14 are timing charts of the various signals appearing in the display controller 1 when the CRT display unit 2 is connected thereto; and

Figs. 15 to 19 are timing charts of the various signals appearing in the display controller 1 when the LCD 3 is connected thereto.

Fig. 1 shows the structure of a display system to which a display controller 1 provided in accordance with one embodiment of the invention is applied. The display controller 1 is of a character display type and effects, in accordance with data stored in a video memory 4, display of characters using 640 x 192 display dots provided on a screen of a CRT display unit 2 or a liquid crystal display unit (hereinafter referred to as "LCD") 3. The display controller 1 drives either of the CRT display unit 2 and the LCD 3 but does not drive both of them at the same time.

The display system shown in Fig. 1 will now be fully described.

[1] Structure of each circuit element of the display system of Fig. 1

Shown at 5 is a central processing unit (CPU) which is connected to a memory 6 including a ROM for storing programs to be executed by the CPU 5 and a ROM for storing data. The CPU 5 stores display data into the video memory 4 which comprises, as shown in Fig. 2, two areas E_0 and E_1 of the same storage capacity. The area E_0 is selected when a "0" signal is supplied to a terminal CS of the video memory 4, while the area E_1 is selected when a "1" signal is supplied to the terminal CS. An address in each of the areas E_0 and E_1 is designated by an address data supplied to an address terminal AD of the memory 4, and read/write of data is performed through a data terminal DT thereof. The memory 4 also comprises a read/write control terminal R/W.

The construction of the video memory 4 and the relation between the addresses of the memory 4 and display positions of characters on the screen will be described. The display data is formed on a two-byte unit basis, and a character to be displayed is represented by two bytes. Fig. 3 shows the two bytes forming a unit of the display data, wherein the first byte contains a character code for designating a character to be displayed and the second byte contains a foreground color code FCA in the lower four bits and a background color code BCA in the higher four bits. In this case, the color code FCA designates a color of the character and the color code BCA designates a color of the background of the character. The character code CRC and the color codes FCA and BCA for a character are stored in the same addresses of the areas E_0 and E_1. For example, in the case where the character code CRC for a given character is stored in the tenth address of the area E_0, the color codes FCA and BCA for the same character are stored in the tenth address of the area E_1.

The relation between the addresses of the memory 4 and the display positions of characters on the screen will now be described. In this embodiment, a character is displayed on the screen using a 8 x 8 dot matrix, and the total number of dots on the screen is 640 x 192. And therefore, up to 80 x 24 characters can

be displayed on the screen at the same time. Assuming that the display screen is divided into display sections each composed of an 8 x 8 dot-matrix as shown in Fig. 4, each character designated by the corresponding display data in the video memory 4 is displayed in a respective one of the display sections. As shown in Fig. 4, the display sections of the screen are assigned numbers 0 to 1919 which represent corresponding display positions. The character codes representative of the characters to be displayed at the display positions No. 0, No. 1, No. 2, ..., No. 1919 are stored in the consecutive addresses of the area E_0 from the lowest one, while the pairs of character codes FCA and BCA corresponding respectively to the character codes CRC are stored in the consecutive addresses of the area E_1 from the lowest one. In this case, the start address SA where the code of the character to be displayed at the display position No. 0 is stored may be any address in the area E_0. For example, in the case of the start address SA being the 100th address, the codes of the characters to be displayed in the display positions No. 0, No. 1, No. 2, ... No. 1919 are stored respectively in the 100th address, 101st address, 102nd address, ... 2019th address.

Referring again to Fig. 1, a character code CRC outputted from the video memory 4 is loaded onto a latch circuit 7, and an output of the latch circuit 7 is supplied to a character generator 8. The character generator 8 comprises a ROM storing character patterns of the characters used in this system, each character pattern being in the form of an 8 rows x 8 columns dot matrix. When a character code CRC is supplied to an address terminal AD_1 of the character generator 8, one of the character patterns which corresponds to the supplied character code is selected. And, one of the rows of the selected character pattern is selected by data LAD supplied to another address terminal AD_0 of the character generator 8. An eight-bit pattern of the thus selected row (row pattern) of the character pattern is outputted from an output terminal OUT of the character generator 8. A parallel-to-serial (P/S) converter 9 composed of a shift register stores the row pattern outputted from the character generator 8 when a load signal LD_2 is supplied to a load terminal L thereof, and then serially outputs the stored row pattern dot by dot in synchronism with a clock pulse ϕ_0. The dot data thus outputted from the P/S converter 9 is supplied as data DD to the display controller 1. The CRT display unit 2 can display a color image composed of 640 x 192 dots in accordance with color signals RS (red), GS (green) and BS (blue), a horizontal synchronization signal HSY and a vertical synchronization signal VSY all supplied from the display controller 1.

The LCD 3 will now be more fully described with reference to Fig. 5. The LCD 3 includes, as shown in Fig. 5, a liquid crystal display panel 13 and a panel driver circuit 14 provided for driving the display panel 13. The liquid crystal display panel 13 has, for example, 640 horizontal electrodes (column electrodes) and 192 vertical electrodes (row electrodes) for displaying an image composed of a 640 x 192 dot matrix. The liquid crystal display panel 13 is divided into two display blocks A and B of an identical construction which are independently driven. The column electrodes of the display block A are driven by a circuit comprising a 640-bit shift register 15a, a 640-bit latch circuit 16a and an electrode driving circuit 17a, while the column electrodes of the display block B are driven by another circuit comprising a 640-bit shift register 15b, a 640-bit latch circuit 16b and an electrode driving circuit 17b. The row electrodes of the display blocks A and B are driven by a circuit comprising a 96-bit shift register 18 and an electrode driving circuit 19.

To display an image on the liquid crystal display panel 13 of the LCD 3, two sets of serial data for respectively displaying dots on the first (uppermost) rows of dots of the display blocks A and B are first supplied as display data LDa and LDb to the shift registers 15a and 15b, respectively, together with a shift clock SCK. When the display data LDa and LDb each composed of 640 bits have been stored respectively in the shift registers 15a and 15b, the display controller 1 outputs a latch clock signal LC and a frame signal FRM. When the latch clock signals LC is outputted, the data contained in the shift registers 15a and 15b are loaded respectively onto the latch circuits 16a and 16b, and when the frame signal FRM is outputted together with the latch clock signal LC, a bit data of "1" is stored into the first-bit stage of the shift register 18, whereby the dots on the 1st (uppermost) rows of the display blocks A and B are driven. The display controller 1 then outputs the data LDa and LDb for displaying dots on the 2nd rows of the display blocks A and B together with the shift clock signal SCK, and outputs the latch clock signal LC when the data LDa and LDb (each composed of 640 bits) are fully loaded onto the shift registers 15a and 15b. When the latch clock signal LC is outputted, the data contained in the shift registers 15a and 15b are stored into the latch circuits 16a and 16b, and at the same time the bit data of "1" is stored into the second bit-stage of the shift register 18, whereby the dots on the 2nd rows of the display blocks A and B are driven. And thereafter, an operation similar to the above is repeatedly carried out to display dots on the display panel 13.

[2] Structure of display controller 1

Fig. 6 shows the structure of the display controller 1, and Fig. 7 shows the structure of an address generating circuit 21 of the display controller 1 of Fig. 6. Firstly, each circuit element of the display

controller 1 of Fig. 6 will be described.

(a) Display control circuit 22

The display control circuit 22 effects a transfer of data between the CPU 5 (Fig. 1) and the display controller 1. When the CPU 5 outputs a display unit selection data C/L (one bit), a border color code BOC (4 bits) and a start address SA, the display control circuit 22 stores them respectively into a register 23, a border register 24 and a start address register 25 (Fig. 7). The display unit selection data C/L indicates the kind of a display unit to be selected, and is rendered "0" when a CRT display unit is used and is rendered "1" when an LCD is used. The border color code BOC designates a color of the border area or the peripheral marginal area of the screen where a display of image is not made. The start address SA indicates, as described above, that address of the video memory 4 where display data for the dots at the display position No. 0 of the screen is stored. When a display data is outputted from the CPU 5, the display control circuit 22 supplies the display data through a buffer amplifier B1 and a terminal T6 to the data terminal DT of the video memory 4. At this time, the display control circuit 22 enables a buffer amplifier B2 of Fig. 1, disables buffer amplifiers B3 and B4 of Fig. 6, and outputs a read/write control signal RWS (a "1" signal) to the video memory 4. As a result, the display data outputted from the CPU 5 is written into the video memory 4. The read/write control signal RWS is normally held in a "0" state. The display control circuit 22 outputs a memory write enable signal to the CPU 5 during each non-display period such as a vertical retrace line period.

(b) Registers 27 and 28

A character code CRC read out of the video memory 4 (Fig. 1) is stored into the latch circuit 7 shown in Fig. 1, whereas color codes FCA and BCA read from the video memory 4 are temporarily stored into the register 27 in response to a load signal LD_1 and are then stored into the register 28 in response to a load signal LD_3. The color codes FCA and BCA thus stored in the register 28 are supplied respectively to input terminals A and B of a selector 29. The synchronization of the signal timings can be achieved by the provision of the register 28.

(c) Selector 29

The selector 29 outputs data fed to the input terminal A when a "1" signal is supplied to a selection terminal Sa thereof, and outputs data fed to the input terminal B when a "0" signal is supplied to the selection terminal Sa. As shown, the selection terminal Sa is supplied with the data DD outputted from the P/S converter 9 of Fig. 1. And therefore, the foreground color code FCA is outputted from the selector 29 when the data DD is "1", and the background color code BCA is outputted when the data DD is "0".

(d) Selector 30

The selector 30 outputs the color code FCA or BCA fed from the selector 29 when a "1" signal is supplied from an AND gate 31 to a selection terminal Sa thereof. When the signal supplied to the selection terminal Sa is "0", the selector 30 outputs the border color code BOC fed from the border register 24. The output signal of the AND gate 31 is rendered "1" only when a display of image is effected on the screen.

(e) Color palette circuit 31

The color palette circuit 31 converts the color code outputted from the selector 30 into color data RD (red), GD (green) and BD (blue) each composed of three bits. The relationship between the color codes used and the color data RD, GD and BD is shown in Table 1.

Table 1

color code	color	RD			GD			BD		
IRGB		R_2	R_1	R_0	G_2	G_1	G_0	B_2	B_1	B_0
0000	Black	0	0	0	0	0	0	0	0	0
0001	Blue	0	0	0	0	0	0	1	0	0
0010	Green	0	0	0	1	0	0	0	0	0
0011	Cyan	0	0	0	1	0	0	1	0	0
0100	Red	0	1	1	0	0	0	0	0	0
0101	Magenta	1	0	0	0	0	0	1	0	0
0110	Brown	1	0	0	0	1	1	0	0	0
0111	White	1	0	0	1	0	0	1	0	0
1000	Gray	0	0	1	0	0	1	0	0	1
1001	Light Blue	0	0	0	0	0	0	1	1	0
1010	Light Green	0	0	0	1	1	0	0	0	0
1011	Light Cyan	0	0	0	1	1	0	1	1	0
1100	Light Red	1	0	1	0	0	0	0	0	0
1101	Light Magenta	1	1	0	0	0	0	1	1	0
1110	Yellow	1	1	0	1	1	0	0	0	0
1111	White (High Intensity)	1	1	1	1	1	1	1	1	1

(f) DACs 32 to 34

The DACs (Digital-to-Analog Converters) 32 to 34 convert the color data RD, GD and BD into corresponding analog signals, respectively. Analog signals outputted from the DACs 32 to 34 are supplied to the CRT display unit 2 of Fig. 1 as the color signals RS, GS and BS, respectively.

(g) Luminance calculation circuit 36

The luminance calculation circuit 36 produces a luminance or an intensity data YD (3 bits) by effecting the following arithmetic operation on the color data RD, GD and BD:

$$\begin{array}{cccccc} & & R_2 & R_1 & R_0 \\ & & & & R_2 \\ & & & B_2 & B_1 \\ +) & G_2 & G_1 & G_0 & G_2 \\ \hline Y_4 & Y_3 & Y_2 & Y_1 & Y_0 \end{array}$$

Wherein R_0, R_1 and R_2 are the first, second and third bits of the color data RD, respectively, and this is true with G_0 to G_2 and B_0 to B_2. Only the second to fourth bits Y_1 to Y_3 of the calculation result are outputted as the luminance data YD. The aforesaid arithmetic operation bases on the following well-known equation for converting analog RGB signals into a luminance signal:

$$Y = 0.3R + 0.59G + 0.11B$$

(h) Gradation display circuit 37

The gray-scale display circuit 37 is provided for achieving a gray-scale display on the liquid crystal display panel 13 of the LCD 3 in accordance with the luminance data YD. The basic principle of the gray-scale display effected in this embodiment will now be described.

In this embodiment, display of an image is performed on a frame basis, and eight consecutive frames constitute one display period. When the luminance data YD for a given dot (dot X) on the panel 13 is "7" (black), the dot X is displayed in each of the eight frame cycles within a display period, that is to say, eight times per display period. When the luminance data YD of the dot X is "0" (white), the dot X is not displayed in any one of the eight frame cycles within a display period. On the other hand, when the luminance data YD of the dot X is any one of "1" to "6", the dot X is displayed the number of times determined by the luminance data YD within each display period. For example, when the luminance data YD is "6", the dot X is displayed seven times within one display period, and when the luminance data YD is "5", the dot is displayed six times. Thus, in this embodiment, the gray-scale display is achieved based on the number of times of display of each dot within a display period. The wording "display a dot" actually means that the dot on the panel 13 is activated by a voltage, that is to say, data representative of "1" for activating the dot is loaded onto the shift register 15a or 15b shown in Fig. 5. Fig. 8 shows one example of the relationship between each luminance data YD and a display timing of the corresponding dot. It will be appreciated from Fig. 8 that when the luminance data YD for a dot to be displayed is "7", the dot is displayed in the first through eighth frame cycles within each display period. And when the luminance data YD is "4", the dot is displayed in the second, fourth, fifth, seventh and eighth frame cycles within each display period. Fig. 9 shows the construction of one example of the gray-scale display circuit 37 which outputs serial display data LD in accordance with the luminance data YD and the display timings shown in Fig. 8. As shown in Fig. 9, the gray-scale display circuit 37 comprises a counter 39 of a three-bit type which counts up the frame signal FRM. The frame signal FRM is outputted once at the beginning of each frame scanning, and therefore the output of this counter 39 indicates the number of the current frame cycle which is one of the frame cycles No. 0 to No. 7 shown in Fig. 8. The gray-scale display circuit 37 further comprises a decoder 40 for decoding the output of the counter 39, a decoder 41 for decoding the luminance data YD, eight OR gates 42, eight AND gates 43 and an OR gate 44. Each of the OR gates 42 effects a logical OR operation on signals applied to nodes (circles) of the input line thereof. And, the output signal of the OR gate 44 is supplied as the display data LD to a distribution circuit 45 of Fig. 6.

(i) Distribution circuit 45

The distribution circuit 45 outputs those bits of the display data LD used for displaying dots on the display block A as display data LDa, and outputs the remaining bits of the display data LD used for displaying dots on the display block B as display data LDb. More specifically, as the gray-scale display circuit 37 alternately outputs eight-bit serial display data for the display block A and eight-bit serial display data for the display block B, the distribution circuit 45 latches the serial display data LD on a sixteen-bit unit basis, and serially outputs the half (eight bits) of the latched data for the display block A as the display data LDa and the other half (eight bits) for the display block B as the display data LDb in synchronization with the shift clock pulse SCK.

(j) Address generating circuit 21

The address generating circuit 21 generates address data MAD for accessing the video memory 4 to read data therefrom. This address generating circuit 21 comprises, as shown in Fig. 7, a gate circuit 47, an adder 48, the start address register 25, and gate circuits 49 to 52. Each of the gate circuits 50 and 51 is additionally provided with a function to establish a multiplication. More specifically, the lower four bits of input terminals of the gate circuit 50 are supplied with "0" signals and an output of the adder 48 is supplied to the remaining upper bits of the input terminals of the gate circuit 50. And therefore, when the gate circuit 50 is opened, the output of the adder 48 is shifted four bits by this gate circuit 50 and is outputted therefrom. Thus, when opened, the gate circuit 50 outputs data sixteen times as large as the output data of the adder 48. Similarly, the lower six bits of input terminals of the gate circuit 51 are supplied with "0" signals, and therefore, when opened, the gate circuit 51 outputs data sixty four times as large as the output data of the adder 48. The address generating circuit 21 further comprises an OR circuit 53 for effecting a logical OR operation on each pair of bits of the output data of the gate circuits 49 and 50, an OR circuit 54 for effecting a logical OR operation on each pair of bits of the output data of the gate circuits 51 and 52, an adder 55, registers 56 and 57 each of which stores and outputs its input data at the trailing edge of a clock pulse ϕ_1, and a selector 58. This address generating circuit 21 will be more fully described later.

(k) Clock pulse generator 61, Flip-flop 62, Horizontal counter 63, and Vertical counter 64

The clock pulse generator 61 shown in Fig. 6 generates a master clock pulse ϕ_0 and the clock pulse ϕ_1 (see Fig. 10-(b)) produced by dividing the master clock pulse ϕ_0 by eight. The flip-flop (hereinafter referred to as "FF") 62 divides the clock pulse ϕ_1 by two to produce a clock pulse ϕ_2 shown in Fig. 10-(c). The horizontal counter 63 counts up the clock pulse ϕ_2 to form a count output indicative of the horizontal scanning position when the CRT display unit 2 is connected, the count output being indicative of the bit positions of the shift registers 15a and 15b (Fig. 5) into which data are to be stored when the LCD 3 is connected. The vertical counter 64 counts up a signal TG outputted from the timing signal generating circuit 65 to form a count output indicative of the vertical scanning position on the screen. The count output of the vertical counter 64 is supplied to the timing signal generating circuit 65. Also, the upper five bits of the count output of the vertical counter 64 are supplied to input terminal B of the adder 48 shown in Fig. 7, while the lower three bits thereof are supplied as the address data LAD to the character generator 8 shown in Fig. 1.

(l) Timing signal generating circuit 65

The timing signal generating circuit 65 generates, in accordance with the clock pulses ϕ_0 to ϕ_2 and the count outputs of the horizontal and vertical counters 63 and 64, a horizontal synchronization signal HSY and a vertical synchronization signal VSY both to be supplied to the CRT display unit 2. The timing signal generating circuit 65 also generates the shift clock signal SCK, the latch clock signal LC and the frame signal FRM all to be supplied to the LCD 3, and further generates other various timing signals.

[3] Operation of the display system

Prior to beginning a display of characters, the CPU 5 outputs the display unit selection data C/L, the border color code BOC and the data representative of the start address SA. These data are stored into the register 23, the border register 24 and the start address register 25, respectively. The CPU 5 then stores display data into the video memory 4. And, the display of characters on the screen is performed based on the data in the registers 23 to 25 and the video memory 4 in the following manner:

[3-1] In the case of the CRT display unit 2 being connected

(a) Basic timings

When the display unit selection data C/L is "0", the clock pulse generator 61 shown in Fig. 6 generates the master clock pulse ϕ_0 of 14.3 MHz and the clock pulse ϕ_1 obtained by dividing the master clock pulse ϕ_0 by eight. The clock pulse ϕ_1 is further divided by two by the FF 62 to form the clock pulse ϕ_2. The waveforms of these clock pulses ϕ_0 to ϕ_2 are shown in Fig. 10. The horizontal counter 63 is triggered at each trailing edge of the clock pulse ϕ_2, so that the count output of the horizontal counter 63 is changed as shown in Fig. 11-(b) in response to the clock signal ϕ_2 shown in Fig. 11-(a). The timing signal generating circuit 65 generates the signal TG shown in Fig. 11-(c) when the count output of the horizontal counter 63 becomes "56", and supplies the generated signal TG to a reset terminal R of the horizontal counter 63 and to a clock terminal CK of the vertical counter 64. At the trailing edge of this signal TG, the horizontal counter 63 is reset and the vertical counter 64 is triggered. And therefore, the count output of the vertical counter 64 varies as shown in Fig. 11-(d). The numeral on the left-hand side of each hyphen shown in Fig. 11-(d) indicates the upper five bits of the count output of the vertical counter 64, and the numeral on the right-hand side of each hyphen indicates the lower three bits thereof. The signal TG shown in Fig. 11-(c) is again illustrated in Fig. 12-(a), and in response to this signal TG, the count output of the vertical counter 64 is changed as shown in Fig. 12-(b), wherein only the upper five bits of the count output are shown. When the upper five bits of the count output of the vertical counter 64 represent "32", the timing signal generating circuit 65 outputs a reset signal VR shown in Fig. 12-(c). The vertical counter 64 is reset at the trailing edge of the reset signal VR.

The clock pulses ϕ_0 to ϕ_2 and the count outputs of the horizontal and vertical counters 63 and 64 described above determine the basic timings of various timing signals used in this system. The timing signal generating circuit 65 thus generates the various timing signals in accordance with the clock pulses ϕ_0 to ϕ_2 and the count outputs of the horizontal and vertical counters 63 and 64.

(b) Operation of the address generating circuit 21

Referring now to Fig. 7, when the display unit selection data C/L is "0", the output of the AND gate 70 is rendered "0", so that the gate circuit 47 is closed to cause data representative of "0" to be supplied to the input terminal A of the adder 48. As a result, the adder 48 outputs the data fed to its input terminal B, that is, the upper five bits of the count output of the vertical counter 64 (the data constituted by these five bits will be hereinafter referred to as "data V"). Also, when the display unit selection data C/L is "0", the selector 58 supplies the gate circuit 52 with the data fed to the input terminal B thereof, that is, the output data of the register 56.

The clock pulses ϕ_1 and ϕ_2 and the count output of the horizontal counter 63 are again illustrated in Figs. 13-(a) to 13-(c). Shown in Figs. 13-(d) and 13-(e) are waveforms of signals M64 and M16 outputted from the timing signal generating circuit 65. When the signal M64 of "1" is outputted from the timing signal generating circuit 65, the gate circuits 49 and 51 are opened, and when the signal M16 of "1" is outputted, the gate circuit 50 is opened. On the other hand, the gate circuit 52 is opened when the signal M64 is rendered "0". Shown in Fig. 13-(f) is the waveform of a signal CiS which is supplied to a carry input terminal Ci of the adder 55 of Fig. 7.

When the signal M64 is rendered "1" at time t_0 shown in Fig. 13, the gate circuit 49 is opened, so that the data representing the start address SA and contained in the start address register 25 is supplied through the gate circuit 49 to one input terminals of the OR circuit 53. At this time, the gate circuit 50 is closed, so that the other input terminals of the OR circuit 53 are supplied with data representative of "0". As a result, the OR circuit 53 outputs the data representing the start address SA to the input terminal A of the adder 55 (see Fig. 13-(g)). Also, when the signal M64 is rendered "1" at the time t_0, the gate circuit 51 is opened, so that it outputs data sixty four times as large as the data V (i.e., 64V) to one input terminals of the OR circuit 54. At this time, the gate circuit 52 is closed, so that the data 64V is supplied to the input terminal B of the adder 55 (see Fig. 13-(h)). Consequently, the data outputted from the adder 55 at the time t_0 becomes equal to "SA + 64V" (Fig. 13-(i)).

At time t_1, the data "SA + 64V" outputted from the adder 55 is stored into the register 56 and thence supplied through the selector 58 to the input terminal of the gate circuit 52. At this time, the signal M64 falls and the signal M16 rises. As a result, at this time t_1 data "16V" outputted from the gate circuit 50 is supplied through the OR circuit 53 to the input terminal A of the adder 55 (see Fig. 13-(g)), while the data "SA + 64V" outputted from the gate circuit 52, that is, the output of the register 56, is supplied through the OR circuit 54 to the input terminal B of the adder 55 (Fig. 13 (h)). Consequently, data "SA + 80V" is outputted from the adder 55 (Fig. 13-(i)). At time t_2, the data "SA + 80V" outputted from the adder 50 and the data "SA + 64V" outputted from the register 56 are stored respectively into the registers 56 and 57, and these data are outputted therefrom (Figs. 13-(j) and 13-(k)). At this time, both of the signals M64 and M16 are rendered "0" to close the gate circuits 49 to 51 and to open the gate circuit 52. As a result, data representative of "0" and the data "SA + 80V" outputted from the register 56 are supplied to the input terminals A and B of the adder 55, so that the adder 55 continues to output the data "SA + 80V". At time t_3, data at the input and output terminals of the adder 55 and the output data of the registers 56 and 57 become as shown in Figs. 13-(g) to 13-(k), and thereafter these data remain unchanged until the signal CiS is rendered "1" at time t_4 Thus, during the time period from the time t_3 to the time t_4, the data "SA + 80V" is outputted as the address data MAD (Fig. 13-(k)), and supplied through the buffer amplifier B3 and the terminal T3 (Fig. 6) to the address terminal AD of the video memory 4 shown in Fig. 1. Each arrow in Fig. 13 indicates that the data is the same as the next data on the left side.

At time t_4, data "SA + 80V" are stored respectively into the registers 56 and 57, and these data are outputted therefrom. At this time, both of the signals M64 and M16 are "0", so that data representative of "0" and the data "SA + 80V" are supplied respectively to the input terminals A and B of the adder 55. At this time t_4, the signal CiS is rendered "1", and therefore, the adder 55 outputs data representative of "SA + 80V + 1". At the next time t_5, the output data of the adder 55, register 56 and register 57 become equal to "SA + 80V + 2", "SA + 80V + 1" and "SA + 80V", respectively (see Figs. 13-(i), 13-(j) and 13-(k)). And, at time t_6, the output data of the adder 55, register 56 and register 57 become equal to "SA + 80V + 3", "SA + 80V + 2" and "SA + 80V + 1", respectively. And thereafter, an operation similar to the above is repeatedly carried out.

Once the signal CiS is rendered "0" at time t_7 which comes in the middle of the period when the count output of the horizontal counter 63 is "41", the output data of the adder 55 which now represents "SA + 80V + 80" is thereafter kept unchanged, and the outputs of the registers 56 and 57 become as shown in Figs. 13-(j) and 13-(k). When the count output of the horizontal counter 63 again becomes equal to "55", the signal M64 is again outputted, whereby an operation similar to the above is repeated.

As will be appreciated from Fig. 13-(k), during the time when the count output of the horizontal counter 63 varies from "2" to "41", the address data MAD is changed from "SA + 80V" to "SA + 80V + 79". For example, if both of the data SA and V are "0", the address data MAD is changed from "0" to "79" as shown in Fig. 13-(m), and if the data SA is "0" but the data V is "1", the address data MAD is changed from "80" to "159" as shown in Fig. 13-(n). It should be noted that the address data MAD thus produced is effective only when the count output of the horizontal counter 63 is within the range of from "2" to "41". When the count output of the horizontal counter 63 is not within the above range, data read from the video memory 4 by the address data MAD are not used for the actual display operation.

As will be seen from Figs. 12-(a) and 12-(b), when the upper five bits of the count output of the vertical counter 64 (that is, the data V) is "0", the signal TG is outputted eight times. On the other hand, the cycle of the signal TG is equal to that of the count operation of the horizontal counter 63. And therefore, if the start address SA is "0", the address data MAD is changed from "0" to "79" eight times while the data V is "0". And, data are read from the video memory 4 by these address data MAD to effect a display of characters on the first row (the uppermost row) shown in Fig. 4 as will be more fully described later. When the data V is "1", the address data MAD is changed from "80" to "159" eight times to read from the video memory 4 data for displaying characters on the second row, and, when the data V is "23" a display of characters is effected on the lowermost row. On the other hand, a non-display period including the vertical retrace time is provided when the data V is within the range of from "24" to "32". The reason why the same address data MAD is outputted eight times is that each character is constituted by eight rows of dots.

(c) Character display operation

Figs. 14-(a) to 14-(c) show the clock pulse ϕ_1, the count output of the horizontal counter 63 and the address data MAD, wherein it is assumed that the start address SA is "0". It is also assumed that within the time range of Fig. 14 the count output of the vertical counter 64 is "0 - 0", that is to say, both of the upper five bits and lower three bits of the count output of the vertical counter 64 are "0". And therefore, time t_{10} shown in Fig. 14 is equal to the time t_{10} shown in Fig. 11. Shown in Fig. 14-(d) is the waveform of the signal ESS outputted from the timing signal generating circuit 65 to the terminal CS of the video memory 4 shown in Fig. 1, Fig. 14-(e) the waveform of the load signal LD_0 supplied to the load terminal L of the latch circuit 7 (Fig. 1), Fig. 14-(f) the waveform of the load signal LD_1 supplied to the load terminal L of the register 27 (Fig. 6), Fig. 14-(g) the waveform of the load signal LD_2 supplied to the load terminal L of the P/S converter)(Fig. 1), Fig. 14-(h) the waveform of the load signal LD_3 supplied to the load terminal L of the register 28 (Fig. 6), and Fig. 14-(i) the waveform of the clock pulse ϕ_0 (Fig. 10-(a)) supplied to the clock terminal CK of the P/S converter 9.

When the address data MAD and the signal ESS in the "0" state are outputted to the memory 4 at the time t_{10} shown in Fig. 14, the character code CRC is read from the address "0" in the area E_0 of the memory 4, this character code being hereinafter referred to as "CRC-0". When the load signal LD_0 is outputted to the latch circuit 7 at the next time t_{11}, the character code CRC-0 is stored into the latch circuit 7 and thence outputted to the address terminal AD_1 of the character generator 8. At this time, the address terminal AD_0 of the character generator 8 is supplied with the address data LAD (the lower three bits of the count output of the vertical counter 64) representative of "0". And therefore, when the character code CRC-0 is supplied to the character generator 8, an eight-bit dot pattern of the first row of the character pattern designated by the character code CRC-0 is read from the character generator 8 and supplied to the P/S converter 9. At time t_{12}, the signal ESS is rendered "1", so that the color codes FCA and BCA are read from the address "0" of the area E_1 of the video memory 4. When the load signal LD_1 is outputted to the register 27 shown in Fig. 6 at time t_{13}, the color codes FCA and BCA read from the memory 4 are stored into the register 27. At the next time t_{14}, the load signal LD_2 is supplied to the P/S converter 9, so that the dot pattern read from the character generator 8 is stored into the P/S converter 9. And, when the load signal LD_3 is supplied to the load terminal L of the register 28 at time t_{15}, the color codes FCA and BCA in the register 27 are stored into the register 28. The dot pattern stored in the P/S converter 9 is then serially outputted as the data DD in accordance with the clock pulse ϕ_0 and supplied to the selection terminal Sa of the selector 29 (Fig. 6) as shown in Fig. 14-(j). Thus, when the data DD is "1" the selector 29 outputs the foreground color code FCA to the selector 30, and when the data DD is "0" the selector 29 outputs the background color code BCA to the selector 30. At this time, the selection terminal Sa of the selector 30 is supplied with a "1" signal as will be described later. And therefore, the color code FCA or BCA thus outputted from the selector 29 is supplied through the selector 30 to the color palette circuit 31 to be converted into the color data RD, GD and BD. The color data RD, GD and BD thus obtained are then converted respectively into the analog color signals RS, GS and BS by the DACs 32 to 34 and supplied to

the CRT display unit 2. On the other hand, the timing signal generating circuit 65 supplies the CRT display unit 2 with the horizontal synchronization signal HSY shown in Fig. 11-(e) and the vertical synchronization signal VSY shown in Fig. 12-(d). And therefore, when the color signals RS, GS and BS are supplied to the CRT display unit 2, the eight dots on the first row of the dot-matrix at the display position No. 0 shown in Fig. 4 are displayed in colors determined by the color signals RS, GS and BS. Thus, when the P/S converter 9 (Fig. 1) outputs the data DD of eight bits during the time period between the time t_{15} and the time t_{16}, a color display of dots is made on the first row of the dot-matrix at the display position No. 0.

On the other hand, during the time period between the time t_{15} and the time t_{16}, the address data MAD is rendered "1" and in addition the signals ESS and LD_0 to LD_3 are outputted in accordance with the same timings as those signals outputted during the time period between the time t_{10} and the time t_{15}. As a result, the first row portion (dot pattern) of the character pattern designated by the character code CRC-1 in the address "1" of the area E_0 of the memory 4 is loaded onto the P/S converter 9 at the time t_{16}. Also, the color codes FCA and BCA in the address "1" of the area E_1 of the memory 4 are stored into the register 28. And, when the dot pattern in the P/S converter 9 is serially outputted as the data DD during the period between the time t_{16} and the time t_{17}, display of dots is made on the first row of the dot-matrix at the display position No. 1 And thereafter, a display operation similar to the above is repeatedly carried out. Fig. 11-(f) shows the address data MAD varying in accordance with the above operation, and Fig. 11-(g) shows the positions of the dots and their display timings.

When all of the dots on the first rows of the dot-matrices of the display position Nos. 0 to 79 have been displayed, the count output of the vertical counter 64 is changed to "0 - 1" (see Fig. 11-(d) at time t_{20}), so that data representative of "1" is supplied as the address data LAD to the address terminal AD_0 of the character generator 8. And, during the time when the count output of the horizontal counter 63 varies from "2" to "41", the dots on the second rows of the dot-matrices of the display position Nos. 0 to 79 are displayed (see Fig. 11-(g)). Thus, when the upper five bits of the count output of the vertical counter 64 is "0", the dots on the first to eighth rows of the dot-matrices of the display position Nos. 0 to 79 are sequentially displayed. In the similar manner, when the upper five bits of the count output of the vertical counter 64 is "1", display of the dots of the dot-matrices of the display position Nos. 80 to 159 is made, ... and when the upper five bits of the count output of the vertical counter 64 is "23", display of the dots of the dot-matrices of the display position Nos. 1840 to 1919 is made.

The waveforms of the signals HD and VD both generated by the timing signal generating circuit 65 are shown in Fig. 11-(h) and in Fig. 12-(e), respectively. As will be appreciated from Figs. 11 and 12, these signals HD and VD should be rendered "1" when the selector 29 shown in Fig. 6 outputs color codes to display dots on the screen. And therefore, the output of the AND gate 31 fed to the selection terminal Sa of the selector 30 (Fig. 6) is rendered "1" during the time when the display of dots are actually performed, and is rendered "0" during other periods. Thus, during the non-display periods, the selector 30 outputs the border color code BOC contained in the border register 24. And, the border area surrounding the 640 X 192 display positions is displayed in accordance with this border color code BOC.

[3-2] In the case where the LCD 3 is connected

(a) Basic timings

The waveforms of the clock pulses ϕ_0 to ϕ_2 in this case are the same as those shown in Fig. 10, but the period of the clock pulse ϕ_0 is now 10.7 MHz. The waveforms of the clock pulse ϕ_2 in this case is shown in Fig. 15-(a), the variation of the count output of the horizontal counter 63 in Fig. 15-(b), the waveform of the signal TG in Fig. 15-(c), and the variation of the count output of the vertical counter 64 in Fig. 15-(d). Shown in Figs. 15-(e) and 15-(f) are the waveforms of the latch clock signal LC and the frame signal FRM, respectively. As shown, the latch clock signal LC is outputted each time the count output of the horizontal counter 63 becomes equal to "85", while the frame signal FRM is outputted when the count output of the horizontal counter 63 is equal to "85" and when the count output of the vertical counter 64 is equal to "0 - 0". Thus, the frame signal FRM is outputted once per vertical scanning. The latch clock LC and the frame signal FRM thus outputted are supplied to the LCD 3. Figs. 15-(g) and 15-(h) show the waveforms of the signals HD and HD_1 outputted from the timing signal generating circuit 65, the signal HD_1 being supplied to one input terminal of the AND gate 68 (Fig. 6). A flip-flop 69 divides the clock pulse ϕ_0 by two to produce a clock pulse ϕ_{0a} which is supplied to the other input terminal of the AND gate 68. When the signal HD_1 is in the "1" state, this clock pulse ϕ_{0a} passes through the AND gate 68 and is thence supplied as the shift clock signal SCK to the LCD 3 and the distribution circuit 45 (see Fig. 19). Fig. 16-(a) shows the signal TC, Fig. 16-(b) the variation of the upper five bits of the count output of the vertical counter 64, Fig.

16-(c) the reset signal VR to the vertical counter 64, and Fig. 16-(d) the signal VD.

(b) Operation of the address generating circuit 21

When the LCD 3 is connected, data representative of "1" is stored in the register 23 (Fig. 6) as the display unit selection data C/L. When the display unit selection data C/L is rendered "1", the AND gate 70 shown in Fig. 7 is enabled to open, so that the clock pulse ϕ_2 is supplied to the gate circuit 47. As a result, when the clock pulse ϕ_2 is in the "0" state, data representative of "0" is supplied to the input terminal A of the adder 48, whereas data representative of "12" is supplied to the input terminal A when the clock pulse ϕ_2 is in the "1" state. The data representative of "12" corresponds to the number of rows of the character display positions in the display block A (see Figs. 4 and 5). When the display unit selection data C/L is "1", the output data of the register 57 is supplied through the selector 58 to the gate circuit 52.

Fig. 17 corresponds to Fig. 13 and shows the timings of the signals generated when the LCD 3 is connected. The signals M64, M16 and CiS generated when the LCD 3 is connected are different in timing from those generated when the CRT 2 is connected. Also, the data supplied respectively to the input terminal A of the adder 48 and the input terminal of the gate circuit 52 when the CRT 2 is connected are different from those supplied when the LCD 3 is connected. However, each circuit element shown in Fig. 7 performs the same operation in both cases. And, in the case where the LCD 3 is connected, the address data MAD varies as shown in Fig. 17-(k). More specifically, if both of the start address SA and the data V (the upper five bits of the count output of the vertical counter 64) are "0", as shown in Fig. 17-(m), data representative of "0" and "80 X 12" (or "960") are sequentially outputted when the count output of the horizontal counter 63 is "4", data representative of "1" and "80 X 1 + 1" (or "961") are sequentially outputted when the count output is "5", ... and data representative of "79" and "80 X 12 + 79" (or "1039") when the count output is "83". The data representative of "0", "1", "2", ... "79" designate those addresses of the video memory 4 in which the character codes CRC of the characters to be displayed on the first row of display positions in the display block A are stored. On the other hand, the data representative of "960", "961", ... "1039" designate those addresses of the video memory 4 in which the character codes CRC of the characters to be displayed on the first row of display positions in the display block B are stored. Similarly, when the start address SA is "0" but the data V is "1", as shown in Fig. 17-(n), data indicative of the addresses storing the character codes CRC of the characters to be displayed on the second rows of display positions in the display blocks A and B are alternately outputted during the time when the count output of the horizontal counter 63 varies from "4" to "83". The similar operation is performed when the data V takes any one of "2" to "11".

Thus, as shown in Fig. 17, data indicative of the addresses storing character codes of the characters to be displayed in the display blocks A and B are outputted in a time sharing manner.

(c) Display of characters

Fig. 18 is a timing chart corresponding to that shown in Fig. 14, wherein it is assumed that the count output of the vertical counter 64 is "0 - 0". During the period between the time t_{30} and the time t_{31} in Fig. 18, the character code CRC-0 and the color codes FCA and BCA are read respectively from the address "0" of the area E_0 and the address "0" of the area E_1 of the video memory 4. The read color codes FCA and BCA are stored into the register 28 shown in Fig. 6, and the dot pattern of the first row of dots of the character pattern designated by the read character code CRC-0 is stored into the P/S converter 9. During the period between the time t_{31} and the time t_{32}, the dot pattern in the P/S converter 9 is serially supplied as data DD to the selector 29, so that the color codes FCA and BCA in the register 28 are selectively outputted therefrom. Each of the thus outputted color codes is converted into color data RD, GD and BD by the color palette circuit 31. The luminance calculation circuit 36 converts the color data RD, GD and BD into luminance data YD which is then converted into display data LD to be supplied to the distribution circuit 45.

On the other hand, during the period between the time t_{31} and the time t_{32}, the character code CRC and the color codes FCA and BCA are read respectively from the addresses "960" of the areas E_0 and E_1 of the video memory 4. And, these read character and color codes are loaded onto the P/S converter 9 and the register 28. Then, during the period between the time t_{32} and the time t_{33}, the data in the P/S converter 9 is serially outputted as the data DD to the selector 29. Consequently, the color codes FCA and BCA are selectively outputted from the selector 29 and converted into the display data LD which is then fed to the distribution circuit 45. And thereafter, an operation similar to the above is repeated.

The distribution circuit 45 latches the data LD (Fig. 19-(b)) on a sixteen-bit unit basis and outputs those bits of the latched data LD for the display block A as data LDa in accordance with the shift clock SCK, as

shown in Fig. 19-(e). The distribution circuit 45 also outputs those bits of the latched data LD for the display block B as data LDb in accordance with the shift clock SCK, as shown in Fig. 19-(f). The thus outputted data LDa and LDb are shifted into the shift registers 15a and 15b, and then loaded into the latch circuits 16a and 16b by the latch clock LC, whereby display of dots is made in accordance with the loaded data LDa and LDb.

The above-described display system is so designed as to display characters, however it is apparent that the present invention can be applied to a graphic display system of a dot-map type.

Claims

1. A display controller capable of selectively driving one of first and second display units, the first display unit (2) having a display screen comprised of a scanning-type screen which provides M rows of N columns of display positions thereon, the second display unit (3) having a display screen (13) constituted by upper (A) and lower (B) scanning-type screens each of which provides P rows of Q columns of display positions thereon, the display controller (1) being further connected to memory means (4) having a plurality of addresses each for storing display data relating to an image to be displayed in a respective one of the display positions of the selected display unit, said display controller (1) comprising:

   (a) display unit designating means (22) for designating one of the first and second display units (2, 3), said designation means (22) outputting a first designation signal (C) when the first display unit (2) is selected, and outputting a second designation signal (L) when the second display unit (3) is selected;

   characterized by

   (b) timing signal generating means (65) responsive to said first designation signal for generating synchronization signals to be supplied to the first display unit (2) for scanning the screen thereof, said timing signal generating means being further responsive to said second designation signal to generate synchronization signals to be supplied to the second display unit (3) for scanning the upper and lower screens (13 A, B) thereof;

   (c) address data generating means (21) responsive to said first designation signal (c) for generating a first series of address data representative of the addresses of the memory means (4) to sequentially output said generated address data to the memory means (4) in accordance with the scanning of the display screen of the first display unit (2), said address data generating means (21) being further responsive to said second designation signal (L) for generating a second series of address data representative of those of the address of the memory means (4) corresponding to the upper screen (13 A) and a third series of address data representative of those of the addresses of the memory means corresponding to the lower screen (13 B), said address data generating means (21) alternately outputting each of said second series of address data and each of said third series of address data to the memory means (4) in accordance with the scannings of the upper and lower screens (13 A, B); and

   (d) display signal generating means (31-34, 36, 37) responsive to said first designation signal (C) for generating a first display signal to be supplied to the first display unit (2) based on data read from the memory means (4) in accordance with said first series of address data, said display signal generating means being further responsive to said second designation signal (L) to generate second and third display signals to be supplied to the second display unit (3) based on data read from the memory means (4) in accordance with said second and third series of address data, said second and third display signals being used to display images on the upper and lower screens (13 A, B), respectively.

2. A display controller according to claim 1, wherein the first display unit (2) is a CRT display unit and the second display unit (3) is a liquid crystal display unit.

3. A display controller according to claim 2, wherein each of the addresses of the memory means indicated by said second series of address data is disposed apart from a respective one of the addresses of the memory means indicated by said third series of address data by the number of addresses corresponding to "P x Q", where P is the number of rows and Q is the number of columns of display positions on the upper display screen (13 A) of the second display unit (3).

* C L M S *

shown in Fig. 19-(e). The distribution circuit 45 also outputs those bits of the latched data LD for the display block B as data LDb in accordance with the shift clock SCK, as shown in Fig. 19-(f). The thus outputted data LDa and LDb are shifted into the shift registers 15a and 15b, and then loaded into the latch circuits 16a and 16b by the latch clock LC, whereby display of dots is made in accordance with the loaded data LDa and LDb.

The above-described display system is so designed as to display characters, however it is apparent that the present invention can be applied to a graphic display system of a dot-map type.

Claims

1. A display controller capable of selectively driving one of first and second display units, the first display unit (2) having a display screen comprised of a scanning-type screen which provides M rows of N columns of display positions thereon, the second display unit (3) having a display screen (13) constituted by upper (A) and lower (B) scanning-type screens each of which provides P rows of Q columns of display positions thereon, the display controller (1) being further connected to memory means (4) having a plurality of addresses each for storing display data relating to an image to be displayed in a respective one of the display positions of the selected display unit, said display controller (1) comprising:

   (a) display unit designating means (22) for designating one of the first and second display units (2, 3), said designation means (22) outputting a first designation signal (C) when the first display unit (2) is selected, and outputting a second designation signal (L) when the second display unit (3) is selected;

   characterized by

   (b) timing signal generating means (65) responsive to said first designation signal for generating synchronization signals to be supplied to the first display unit (2) for scanning the screen thereof, said timing signal generating means being further responsive to said second designation signal to generate synchronization signals to be supplied to the second display unit (3) for scanning the upper and lower screens (13 A, B) thereof;

   (c) address data generating means (21) responsive to said first designation signal (c) for generating a first series of address data representative of the addresses of the memory means (4) to sequentially output said generated address data to the memory means (4) in accordance with the scanning of the display screen of the first display unit (2), said address data generating means (21) being further responsive to said second designation signal (L) for generating a second series of address data representative of those of the address of the memory means (4) corresponding to the upper screen (13 A) and a third series of address data representative of those of the addresses of the memory means corresponding to the lower screen (13 B), said address data generating means (21) alternately outputting each of said second series of address data and each of said third series of address data to the memory means (4) in accordance with the scannings of the upper and lower screens (13 A, B); and

   (d) display signal generating means (31-34, 36, 37) responsive to said first designation signal (C) for generating a first display signal to be supplied to the first display unit (2) based on data read from the memory means (4) in accordance with said first series of address data, said display signal generating means being further responsive to said second designation signal (L) to generate second and third display signals to be supplied to the second display unit (3) based on data read from the memory means (4) in accordance with said second and third series of address data, said second and third display signals being used to display images on the upper and lower screens (13 A, B), respectively.

2. A display controller according to claim 1, wherein the first display unit (2) is a CRT display unit and the second display unit (3) is a liquid crystal display unit.

3. A display controller according to claim 2, wherein each of the addresses of the memory means indicated by said second series of address data is disposed apart from a respective one of the addresses of the memory means indicated by said third series of address data by the number of addresses corresponding to "P x Q", where P is the number of rows and Q is the number of columns of display positions on the upper display screen (13 A) of the second display unit (3).

4. A display controller according to claim 3 further comprising counter means operable in synchronism with said synchronization signals generated by said timing signal generating means (65) for outputting data "V" representative of the number of the row of the display position currently scanned on the display screen of the designated display unit (2, 3), and wherein said address data generating means (21) comprises:

calculation means (49-58) responsive to said first designation signal for calculating "N x V", where N is the number of columns of display positions on the display screen of the first display unit (2), said calculation means being further responsive to said second designation signal to calculate "Q x V" and "Q x V + P x Q", where P is the number of rows and Q is the number of columns of display positions on the display screen of the second display unit (3);

first address register means (56) responsive to said first designation signal for being loaded with said "N x V" before beginning of each of horizontal scanning of the display screen of the first display unit (2), said first address register means (56) being further responsive to said second designation means for being loaded with said "Q x V" before beginning of each of horizontal scanning of the display screen of the second display unit (2);

second address register means (57) responsive to said second designation signal for being loaded with said "Q x V + P x Q" before beginning of each of the horizontal scanning of the display screen of the second display unit (3);

means (55) responsive to said first designation signal for incrementing the contents of said first address register means (56) in accordance with the horizontal scanning of the display screen of the first display unit (2) and outputting the contents of said first address register means (56) as said first series of address data; and

means (55) responsive to said second designation signal for incrementing the contents of both of said first and second address register means (56, 57) in accordance with the horizontal scannings of the upper and lower screens (13 A, B) of the second display unit (3) and alternately outputting the contents of said first and second address register means as said second and third series of address data, respectively.

5. A display controller according to claim 4, wherein each of the display data stored in the memory means (4) comprises a character code (CRC) representative of a character to be displayed in the corresponding display position and a pair of color codes (FCA, BCA) for respectively designating foreground and background colors of said character, and wherein said display signal generating means comprises:

character generator means (8) responsive to each of the character codes read from the memory means (4) for generating a bit pattern of a character represented by the corresponding character code;

selector means (29) for selectively outputting color codes read from the memory means with said character code in accordance with said bit pattern; and

first conversion means (31) for converting each of the color codes outputted from said selector means (2) into corresponding color component signals to be outputted as said first display signal.

6. A display controller according to claim 5, wherein said display signal generating means further comprises second conversion means (36) responsive to said second designation signal for converting said color component signals outputted from said first conversion means into a corresponding luminance signal, and a signal distribution means (45) for outputting those of the luminance signals corresponding to the display positions on the upper screen (13 A) as said second display signal and outputting those of the luminance signals corresponding to the display positions on the lower screen (13 B) as said third display signal.

Patentansprüche

1. Anzeigesteuergerät zum wahlweisen Betrieb einer ersten oder einer zweiten Anzeigeeinheit, wobei die erste Anzeigeeinheit (2) einen Abtastanzeigeschirm mit M Reihen und N Spalten von Anzeigepositionen aufweist und die zweite Anzeigeeinheit (3) einen Anzeigeschirm (13) aufweist, der aus einem oberen (A) und einem unteren (B) Abtastschirm besteht, von denen jeder P Reihen mit Q Spalten von Anzeigepositionen hat, wobei das Anzeigesteuergerät (1) ferner mit Speichermitteln (4) verbunden ist, die eine Vielzahl von Adressen haben, die jeweils für die Speicherung von Anzeigedaten bestimmt sind, die sich auf ein Bild beziehen, das in den jeweiligen Anzeigepositionen einer ausgewählten Anzeigeeinheit darzustellen ist, welches Anzeigegerät (1) folgendes aufweist:

(a) Anzeigeeinheitbestimmungsmittel (22) zum Bestimmen der ersten oder zweiten Anzeigeeinheit (2, 3), welche Bestimmungsmittel (22) ein erstes Anzeigesignal (C) ausgeben, wenn die erste Anzeigeeinheit (2) ausgewählt ist, und die ein zweites Anzeigesignal (L) ausgeben, wenn die zweite Anzeigeeinheit (3) gewählt ist, gekennzeichnet durch:

(b) Zeitsignalerzeugungsmittel (65), die auf das erste Bestimmungssignal ansprechen, um Synchronisationssignale zu erzeugen, die an die erste Anzeigeeinheit (2) geliefert werden, um deren Schirm abzutasten, wobei die Zeitsignalerzeugungsmittel ferner auf das zweite Bestimmungssignal ansprechen, um Synchronisationssignale zu erzeugen, die zu der zweiten Anzeigeeinheit (3) geliefert werden, um deren oberen und unteren Schirm (13 A, B) abzutasten;

(c) Adressdatenerzeugungsmittel (21), die auf das erste Bestimmungssignal (C) ansprechen, um eine Serie von Adressdaten zu erzeugen, die repräsentativ für die Adressen der Speichermitteln (4) sind, um entsprechend dem Abtastvorgang des Anzeigeschirmes der ersten Anzeigeeinheit (2) sequentiell die erzeugten Adressdaten an die Speichermittel (4) auszugeben, wobei die Adressdatenerzeugungsmittel (21) ferner auf das zweite Bestimmungssignal (L) ansprechen, um eine zweite Serie von Adressdaten, die repräsentativ für diejenigen Adressen der Speichermittel (4) sind, die dem oberen Schirm (13 A) entsprechen, und eine dritte Serie von Adressdaten zu erzeugen, die für diejenigen Adressen der Speichermittel repräsentativ sind, die dem unteren Schirm (13 B) entsprechen, wobei ferner die Adressdatenerzeugungsmittel (21) alternierend jeweils die zweite Serie von Adressdaten und jeweils die dritte Serie von Adressdaten an die Speichermittel (4) entsprechend dem Abtastvorgang des oberen und unteren Schirm (13 A, B) ausgeben; und durch

(d) Anzeigesignalerzeugungsmittel (31 - 34, 36, 37), die auf das erste Bestimmungssignal (C) ansprechen, um ein erstes an die Anzeigeeinheit (2) zu lieferndes Anzeigesignal auf der Basis der von den Speichermitteln (4) gemäß der ersten Serie von Adressdaten ausgelesenen Daten zu erzeugen, wobei die Anzeigesignalerzeugungsmittel ferner auf das zweite Bestimmungssignal (L) ansprechen, um zweite und dritte, an die zweite Anzeigeeinheit (3) zu liefernde Anzeigesignale auf der Basis der aus den Speichermitteln (4) gemäß der zweiten Serie und dritten Serie von Adressdaten ausgelesenen Daten zu erzeugen, wobei die zweiten und dritten Anzeigesignale verwendet werden, um Bilder jeweils auf dem oberen bzw. unteren Schirm (13 A, B) zu erzeugen.

2. Anzeigesteuergerät nach Anspruch 1, bei dem die erste Anzeigeeinheit (2) eine Kathodenstrahlröhrenanzeigeeinheit und die zweite Anzeigeeinheit (3) eine Flüssigkristallanzeigeeinheit ist.

3. Anzeigesteuergerät nach Anspruch 2, bei dem jeweils die Adressen der Speichermittel, die durch die zweite Serie von Adressdaten angezeigt werden, jeweils entfernt von entsprechenden Adressen der Speichermittel liegen, die durch die dritte Serie von Adressdaten angezeigt werden, wobei die Entfernung durch die Zahl von Adressen gegeben ist, die "P x Q" ist, wobei P die Anzahl der Reihen und Q die Anzahl der Spalten der Anzeigepositionen auf dem oberen Anzeigeschirm (13 A) der zweiten Anzeigeeinheit (3) sind.

4. Anzeigesteuergerät nach Anspruch 3, das ferner Zählmittel aufweist, die synchron mit den von den Zeitsignalerzeugungsmitteln (65) erzeugten Synchronisationssignalen betreibbar sind, um Daten "V" auszugeben, die repräsentativ für die Nummer der Reihe der Anzeigepositionen ist, die momentan auf dem Anzeigeschirm der ausgewählten Anzeigeeinheit (2, 3) abgetastet wird, wobei ferner die Adressdatenerzeugungsmittel (21) folgendes aufweisen:

Berechnungsmittel (49 - 58), die auf das erste Bestimmungssignal ansprechen, um "N x V" zu berechnen, wobei N die Anzahl der Spalten der Anzeigepositionen auf dem Anzeigeschirm der ersten Anzeigeeinheit (2) ist, wobei die Berechnungsmittel ferner auf das zweite Bestimmungssignal ansprechen, um "Q x V" und "Q x V + P x Q" zu berechnen, wobei P die Anzahl der Reihen und Q die Anzahl der Spalten der Anzeigepositionen auf dem Anzeigeschirm der zweiten Anzeigeeinheit (3) sind;

erste Adressregistermittel (56), die auf das erste Bestimmungssignal ansprechen, um mit dem Wert "N x V" beladen zu werden, bevor die jeweiligen Horizontalabtastungen des Anzeigeschirms der ersten Anzeigeeinheit (2) begonnen werden, welche ersten Adressregistermittel (56) ferner auf die zweiten Anzeigemittel ansprechen, um mit dem Wert "Q x V" beladen zu werden, bevor jeweils die Horizontalabtastung des Anzeigeschirms der zweiten Anzeigeeinheit (2) begonnen wird;

zweite Adressregistermittel (57), die auf das Bestimmungssignal ansprechen, um mit dem Wert " Q x V + P x Q" beladen zu werden, bevor jeweils die Horizontalabtastung des Anzeigeschirms der zweiten Anzeigeeinheit (3) begonnen wird;

Mittel (55), die auf das erste Bestimmungssignal ansprechen, um den Inhalt der ersten Adressregi-

stermittel (56) entsprechend der Horizontalabtastung des Anzeigeschirms der ersten Anzeigeneinheit (2) zu erhöhen und die Inhalte der ersten Anzeigeregistermittel (56) als die erste Serie von Adressdaten auszugeben; und

Mittel (55), die auf das zweite Bestimmungssignal ansprechen, um den Inhalt der ersten und der zweiten Adressregistermittel (56, 57) entsprechend den Horizontalabtastungen des oberen und des unteren Schirms (13 A, B) der zweiten Anzeigeeinheit (3) zu erhöhen und alternierend jeweils die Inhalte der ersten und der zweiten Adressregistermittel als die zweite bzw. dritte Serie von Adressdaten auszugeben.

5. Anzeigesteuergerät nach Anspruch 4, bei dem die in den Speichermitteln (4) gespeicherten Anzeigedaten jeweils einen Schriftzeichencode (CRC), der für ein in den entsprechenden Anzeigepositionen anzuzeigendes Schriftzeichen repräsentativ ist, und ein Paar von Farbcodes (FCA, BCA) aufweisen, um jeweils Vordergrund- bzw. Hintergrundfarben des Schriftzeichen zu bestimmen, wobei ferner die Anzeigesignalerzeugungsmittel folgendes aufweisen:

Schriftzeichenerzeugungsmittel (8), die jeweils auf die aus den Speichermitteln (4) ausgelesenen Schriftzeichencodes ansprechen, um ein Bitmuster eines durch den entsprechenden Schriftzeichencode repräsentierten Schriftzeichens zu erzeugen;

Auswahlmittel (29), um selektiv Farbcodes auszugeben, die von den Speichermitteln mit dem Schriftzeichencode entsprechend dem Bitmuster gelesen werden; und

erste Konversionsmittel (31), um die von den Auswahlmitteln (2) ausgegebenen Farbcodes in entsprechende Farbkomponentensignale zu konvertieren, die als das erste Anzeigesignal ausgegeben werden.

6. Anzeigesteuergerät nach Anspruch 5, bei dem die Anzeigesignalerzeugungsmittel ferner zweite Konversionsmittel (36) aufweisen, die auf das zweite Bestimmungssignal ansprechen, um die von den ersten Konversionsmitteln ausgegebenen Farbkomponentensignale in ein entsprechendes Luminanzsignal zu verwandeln, und die ferner Signalverteilungsmittel (45) aufweisen, um die den Anzeigepositionen auf dem oberen Schirm (13 A) entsprechenden Luminanzsignale als das zweite Anzeigesignal und die den Positionen auf dem unteren Schirm (13 B) entsprechenden Luminanzsignale als das dritte Anzeigesignal auszugeben.

Revendications

1. Unité de commande d'affichage capable de piloter de manière sélective l'une d'une première et d'une seconde unités d'affichage, la première unité d'affichage (2) comportant un écran d'affichage constitué d'un écran du type à balayage qui possède M lignes et N colonnes de positions d'affichage, la seconde unité d'affichage (3) comportant un écran d'affichage (13) constitué par des écrans, du type à balayage, supérieur (A) et inférieur (B), dont chacun possède P lignes et Q colonnes de positions d'affichage, l'unité de commande d'affichage 1 étant en outre reliée à un moyen de mémoire (4) possédant une pluralité d'adresses, chacune pour mémoriser une donnée d'affichage relative à une image à afficher dans l'une respective des positions d'affichage de l'unité d'affichage sélectionnée, ladite unité de commande d'affichage (1) comprenant :

(a) un moyen de désignation d'unité d'affichage (22) pour désigner l'une de la première et de la seconde unités d'affichage (2, 3), ledit moyen de désignation (22) émettant un premier signal de désignation (C) lorsque la première unité d'affichage (2) est sélectionnée, et émettant un second signal de désignation (L) lorsque la seconde unité d'affichage (3) est sélectionnée ;

caractérisé par :

(b) un moyen générateur de signaux de synchronisation (65) sensible audit premier signal de désignation pour produire des signaux de synchronisation destinés à être délivrés à la première unité d'affichage (2) pour le balayage de son écran, ledit moyen générateur de signaux de synchronisation étant en outre sensible audit second signal de désignation pour produire des signaux de synchronisation destinés à être délivrés à la seconde unité d'affichage (3) pour balayer ses écrans supérieur et inférieur (13 A, B) ;

(c) un moyen générateur de données d'adresse (21) sensible audit premier signal de désignation (C) pour produire une série de données d'adresse représentatives des adresses du moyen de mémoire (4) pour sortir séquentiellement lesdites données d'adresse produites vers le moyen de mémoire (4) en fonction du balayage de l'écran d'affichage de la première unité d'affichage (2), ledit moyen générateur de données d'adresse (21) étant en outre sensible audit second signal de désignation

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(L) pour produire une deuxième série de données d'adresse représentatives de celles des adresses du moyen de mémoire (4) qui correspondent à l'écran supérieur (13 A) et une troisième série de données d'adresse représentatives de celles des adresses du moyen de mémoire qui correspondent à l'écran inférieur (13 B), ledit moyen générateur de données d'adresse (21) sortant de façon alternée chacune desdites deuxième série de données d'adresse et chacune desdites troisième série de données d'adresses vers le moyen de mémoire (4) en fonction des balayages des écrans supérieur et inférieur (13 A, B) ; et,

(d) un moyen générateur de signal d'affichage (31 à 34, 36, 37) sensible audit premier signal de désignation (C) pour produire un premier signal d'affichage destiné à être délivré à la première unité d'affichage (2) en se basant sur les données lues dans le moyen de mémoire (4) en fonction de ladite première série de données d'adresse, ledit moyen générateur de signal d'affichage étant en outre sensible audit second signal de désignation (L) pour produire des deuxième et troisième signaux d'affichage destinés à être délivrés à la seconde unité d'affichage (3) en se basant sur les données lues dans le moyen de mémoire (4) en fonction desdites deuxième et troisième séries de données d'adresse, lesdits deuxième et troisième signaux d'affichage étant utilisés pour afficher des images, respectivement, sur les écrans supérieur et inférieur (13 A, B).

2. Unité de commande d'affichage selon la revendication 1, dans laquelle la première unité d'affichage (2) est un affichage à CRT (tube à rayons cathodiques) et la seconde unité d'affichage (3) est une unité d'affichage à cristaux liquides.

3. Unité de commande d'affichage selon la revendication 2, dans laquelle chacune des adresses du moyen de mémoire indiquées par ladite seconde série de données d'adresse est disposée séparée, de l'une respective des adresses du moyen de mémoire indiqué par ladite troisième série de données d'adresse, du nombre d'adresses correspondant à "P x Q", où P est le nombre de lignes et Q est le nombre de colonnes des positions d'affichage de l'écran d'affichage supérieur (13 A) de la seconde unité d'affichage (3).

4. Unité de commande d'affichage selon la revendication 3, comprenant en outre un moyen de comptage manoeuvrable en synchronisme avec lesdits signaux de synchronisation produits par ledit moyen générateur de signaux de synchronisation (65) pour sortir une donnée "V" représentative du nombre de lignes de la position d'affichage en cours de balayage sur l'écran d'affichage de l'unité d'affichage désignée (2, 3), et dans laquelle ledit moyen générateur de données d'adresse (21) comprend :

un moyen de calcul (49 à 58) sensible audit premier signal de désignation pour calculer "N x V", où N est le nombre de colonnes des positions d'affichage sur l'écran d'affichage de la première unité d'affichage (2), ledit moyen de calcul étant en outre sensible audit second signal de désignation pour calculer "Q x V" et "Q x V + P x Q", où P est le nombre de lignes et Q est le nombre de colonnes des positions d'affichage sur l'écran d'affichage de la seconde unité d'affichage (3) ;

un premier moyen de registre d'adresse (56) sensible audit premier signal de désignation destiné à être chargé avec ledit "N x V" avant le commencement de chaque balayage horizontal de l'écran d'affichage de la première unité d'affichage (2), ledit premier moyen de registre d'adresse (56) étant en outre sensible audit second moyen de désignation pour être chargé avec ledit "Q x V" avant le commencement de chaque balayage horizontal de l'écran d'affichage de la seconde unité d'affichage (2) ;

un second moyen de registre d'adresse (57) sensible audit second signal de désignation pour être chargé avec ledit "Q x V + P x Q" avant le commencement de chacun des balayages horizontaux de l'écran d'affichage de la seconde unité d'affichage (3) ;

un moyen (55) sensible audit premier signal de désignation pour incrémenter le contenu dudit premier moyen de registre d'adresse (56) en fonction du balayage horizontal de l'écran d'affichage de la première unité d'affichage (2) et pour sortir le contenu dudit premier de registre d'adresse (56) comme étant ladite première série de données d'adresse ; et,

un moyen (55) sensible audit second signal de désignation pour incrémenter le contenu à la fois dudit premier et dudit second moyens de registre d'adresse (56, 57) en fonction des balayages horizontaux des écrans supérieur et inférieur (13 A, B) de la seconde unité d'affichage (3) et pour sortir de façon alternée, respectivement, le contenu dudit premier et dudit second moyens de registre d'adresse, comme étant lesdites seconde et troisième séries de données d'adresse.

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5. Unité de commande d'affichage selon la revendication 4, dans laquelle chacune des données mémorisées dans le moyen de mémoire (4) comprend un code de caractère (CRC) représentatif d'un caractère à afficher dans la position d'affichage correspondante et une paire de codes de couleur (FCA, BCA) pour désigner respectivement des couleurs d'avant plan et d'arrière plan dudit caractère, et dans laquelle ledit moyen générateur de signal d'affichage comprend :

un moyen générateur de caractères (8) sensible à chacun des codes de caractère lus dans le moyen de mémoire (4) pour produire un dessin binaire d'un caractère représenté par le code de caractère correspondant ;

un moyen de sélection (29) pour sortir de manière sélective des codes de couleur lus dans le moyen de mémoire avec ledit code de caractère en fonction dudit dessin binaire ; et,

un premier moyen de conversion (31) pour convertir chacun des codes de couleur sorti dudit moyen de sélection (2) en des signaux de composantes de couleur correspondants destinés à être sortis comme étant ledit premier signal d'affichage.

6. Unité de commande d'affichage selon la revendication 5, dans laquelle ledit moyen générateur de signal d'affichage comprend en outre un second moyen de conversion (36), sensible audit second signal de désignation, pour convertir lesdits signaux de composantes de couleur, sortis dudit premier moyen de conversion, en un signal de luminance correspondant, et un moyen de répartition de signaux (45) pour sortir ceux des signaux de luminance qui correspondent aux positions d'affichage sur l'écran supérieur (13 A) comme étant ledit second signal d'affichage et pour sortir ceux des signaux de luminance qui correspondent aux positions d'affichage sur l'écran inférieur (13 B) comme étant ledit troisième signal d'affichage.