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(21) International Application Number: ☒ PCT/US95/14483 (22) International Filing Date: ☒ 6 November 1995 (06.11.95) (30) Priority Data: 08/335,267 ☒ 7 November 1994 (07.11.94) ☒ US (71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 S. Federal Way, Boise, ID 83706-9632 (US). PLS CHECK PFB (72) Inventors: AKRAM, Salman; Apartment #33, 3713 Gekeler Road, Boise, ID 83706 (US). FARNWORTH, Warren, M.; 2004 S. Banner, Nampa, ID 83686-7271 (US). WOOD, Alan, G.; 1366 E. Versailles Court, Boise, ID 83706 (US). (74) Agent: FLETCHER, Michael, G.; P.O. Box 4433, Houston, TX 77210 (US).		(81) Designated States: AL, AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, LS, MW, SD, SZ, UG). Published With international search report. PLS CHECK Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
(54) Title: METHOD FOR FABRICATING A SELF-LIMITING SILICON BASED INTERCONNECT FOR TESTING BARE SEMI-CONDUCTOR DICE (57) Abstract <p>A method for forming a self-limiting, silicon based interconnect for making temporary electrical contact with bond pads on a semiconductor die is provided. The interconnect includes a silicon substrate having an array of contact members adapted to contact the bond pads on the die for test purposes (e.g., burn-in testing). The interconnect is fabricated by: forming the contact members on the substrate; forming a conductive layer on the tip of the contact members; and then forming conductive traces to the conductive layer. The conductive layer is formed by depositing a silicon containing layer (e.g., polysilicon, amorphous silicon) and a metal layer (e.g., titanium, tungsten, platinum) on the substrate and contact members. These layers are reacted to form a silicide. The unreacted metal and silicon containing layer are then etched selective to the conductive layer which remains on the tip of the contact members. Conductive traces are then formed in contact with the conductive layer using a suitable metallization process. Bond wires are attached to the conductive traces and may be attached to external test circuitry. Alternately, another conductive path such as external contacts (e.g., slide contacts) may provide a conductive path between the conductive traces and external circuitry. The conductive layer, conductive traces and bond wires provide a low resistivity conductive path from the tips of the contact members to external test circuitry.</p>		

