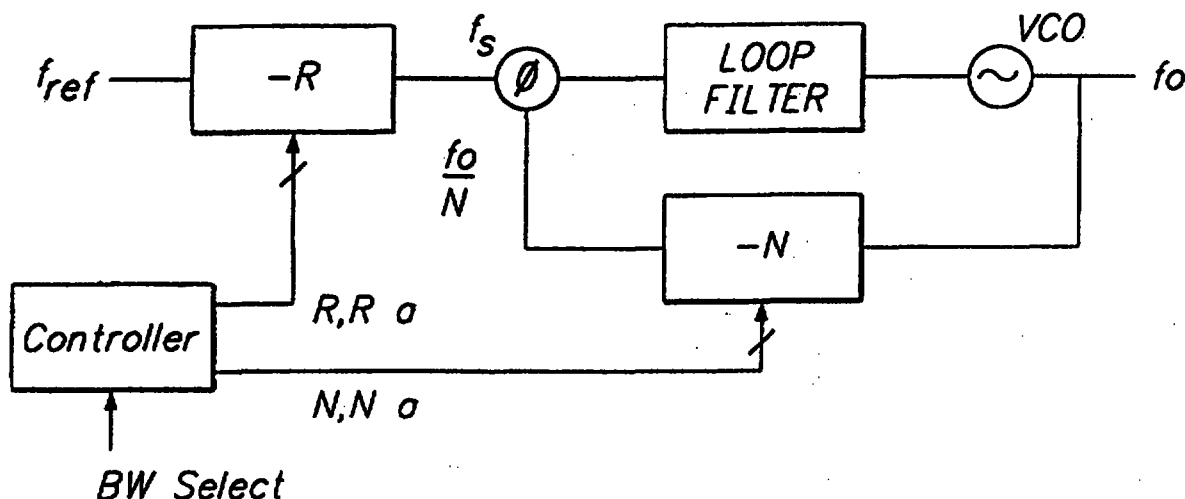




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H03L 7/107, 7/18		A1	(11) International Publication Number: WO 00/31874
			(43) International Publication Date: 2 June 2000 (02.06.00)
(21) International Application Number: PCT/US99/24466 (22) International Filing Date: 21 October 1999 (21.10.99) (30) Priority Data: 09/197,523 23 November 1998 (23.11.98) US (63) Related by Continuation (CON) or Continuation-in-Part (CIP) to Earlier Application US 09/197,523 (CON) Filed on 23 November 1998 (23.11.98) (71) Applicant (for all designated States except US): TROPICAN, INC. [US/US]; Suite 150, 20813 Stevens Creek Boulevard, Cupertino, CA 95014 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): SANDER, Brian [US/US]; 5504 Perugia Circle, San Jose, CA 95138 (US). (74) Agent: URE, Michael, J.; Burns, Doane, Swecker & Mathis, L.L.P., P.O. Box 1404, Alexandria, VA 22313-1404 (US).		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.	

(54) Title: PHASE LOCK LOOP ENABLING SMOOTH LOOP BANDWIDTH SWITCHING



(57) Abstract

The present invention, generally speaking, provides a PLL that enables smooth switching of loop bandwidth without changing the loop filter. In accordance with one aspect of the invention, the loop bandwidth of a phase locked loop including an output frequency divider (5) and a reference frequency divider (1) is changed by changing a divisor of the output frequency divider (5) by a factor and changing a divisor of the reference frequency divider (1) by substantially the same factor. If the factor is greater than one, the loop bandwidth is decreased. If the factor is less than one, then the bandwidth is increased. In accordance with another aspect of the invention, a phase locked loop includes an oscillator (4) having a control input, a phase comparator (2), a loop filter (3), and a feedback path including an output frequency divider (5). A reference frequency divider (1) is also provided. A controller (6) is coupled to the output frequency divider (5) and to the reference frequency divider (1) for changing a divisor of each at substantially the same time in response to a bandwidth select signal. The controller (6) changes the divisor by substantially the same factor, changing the loop bandwidth without affecting the output frequency of the phase lock loop.