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INTEGRATED DYNAMIC POWER DISSIPATION CONTROL SYSTEM FOR VERY LARGE SCALE INTEGRATED (VLSI) CHIPS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention is related to very large scale integrated circuit chips and more specifically to a method and apparatus for maintaining functional operation when chip temperatures exceed operating temperature specifications.

Prior Art

A notebook computer is a small, lightweight, portable, battery-powered, lap-top personal computer (PC) that uses a thin, lightweight, display screen such as a liquid crystal display (LCD). Notebook PCs typically run several hours on rechargeable batteries, weigh 4-7 pounds, fold up, and can be carried like a briefcase. Because of their small size and portability these small devices are often times exposed to environments where the temperature range for which the microprocessor CHIPS were designed is greatly exceeded. This could lead to intermittent operation of the device and a shortened lifetime of the integrated circuit chips that make up the device's logical circuits.

Phase-locked loop (PLL) clocks are placed on integrated circuit chips to minimize clock delay skew between a board-level system clock and latches fabricated on the chip. The delay skew is created by the number of buffering levels needed on the chip to distribute the clock signal to all of the latches on the chip. PLL's can also change the frequency of the board level system clock so that the chip clock frequency is higher or lower than the board level system clock. It is well known that logical circuits consume power in proportion to the frequency at which they operate. The higher the operational frequency, the higher the power dissipation. By controlling the clock frequency to the logic one can control the power dissipation.

It is therefore an object of this invention to provide a method and means for controlling the temperature of a very large scale integrated (VLSI) circuit chip by controlling phase locked loop (PLL) clock circuitry existing on the chip.

SUMMARY OF THE INVENTION

Briefly, the above object is accomplished in accordance with the invention by providing chip logic, a phase locked loop (PLL) clocking circuit, a temperature sensing circuit, and a power management circuit, all fabricated on a very large scale integrated (VLSI) circuit chip. The temperature sensing circuit directly measures the chip temperature, producing a temperature output signal. The power management circuit, which is connected to the temperature sensing circuit and to the chip logic, responds to the temperature output signal and to a functional state of the chip logic to generate a control signal to the PLL. The PLL responds to the control signal to change the operation of the PLL, by either stopping the clock or modifying the operating frequency thereof, depending upon the state of the control signal.

An advantage of this invention is that excessive system temperatures on a chip are regulated by controlling the effective duty cycle of a chip clock.

A further advantage of this invention is that it allows a device to operate at reduced system performance levels while temperatures at the chip level are being reduced.

A further advantage of this invention is that it allows a device to operate at above specified system performance levels when temperatures at the chip are below designated levels.

The foregoing and other objects, features, and advantages of the invention will be apparent from the following more particular

description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a diagram of a prior art phase locked loop clock circuit;

FIGURE 2 is a diagram of a system in which the present invention is embodied,

FIGURE 3 is a flow diagram of a method of dynamically maintaining chip temperatures in accordance with the present invention;

FIGURE 4 is a timing diagram of the operation of the invention in a stop clock mode; and,

FIGURE 5 is a timing diagram of the operation of the invention in a modify frequency mode.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIGURE 1 is a diagram of a prior art phase locked loop (PLL) clock circuit that is capable of frequency multiplication. An input signal (10) from a system clock is divided by a divide by P ($/P$) frequency divider (12). The PLL consists of a closed loop including a phase detector (16), a voltage control oscillator (VCO 20), and a divide by N ($/N$) frequency divider (24). A phase difference and frequency difference between the signals (14) and (26) are detected in the phase detector (16) and an error signal (18) corresponding to the detected differences is output to the VCO (20). The VCO provides an output (22) that is phase-locked with the input signal (10). The $/N$ frequency divider (24) divides the frequency of the signal (22) by N and feeds it back to the phase detector (16) so that the frequency is locked. The variables P and N of the frequency dividers can be programmed with values to provide a variable frequency output selected by the values of P and N. The $/P$ circuit provides one pulse out for every P pulses applied. Likewise, the

/N circuit provide one pulse out for every N pulses applied. The frequency out of the PLL is $N \cdot F / P$, where F is the input frequency, and N and P are integers greater than zero and represent a frequency division of an applied signal.

Refer to FIGURE 2 which is a diagram of a power dissipation control system in which the present invention is embodied. The power dissipation control system uses a phase locked loop (30) which is of the layout shown in FIGURE 1. The PLL (30), a temperature sensor (32), a power management circuit (34), an AND circuit (36) and chip logic (38) are all fabricated on a very large scale integrated circuit (VLSI) chip. The temperature sensor (32) measures the chip temperature and generates a temperature monitoring signal (33) to the power management circuit (34). The chip logic (38) generates a chip status signal (46) to the power management circuit (34) that indicates the functional state of the chip logic. Using the temperature monitoring signal (33) and the chip status signal (46), the power management circuit determines if it is necessary to raise or lower the chip temperature. Two methods are available to the power management circuit for lowering the chip temperature. It can either stop the PLL clock for a period of time or it can reprogram the frequency divider circuits in the PLL.

Stopping the PLL output from reaching the chip logic stop all functions on chip logic so that no power is dissipated in the chip logic. Gating the output of the PLL in the AND (36) permits the PLL to continue operation and therefore provides a way to restart the chip clock without having to wait for the PLL to regain lock.

Reprogramming the frequency divider circuits in the PLL to reduce the frequency will change the effective duty cycle of the PLL and hence will reduce the power consumption in the chip logic. The chip logic will then function at lowered performance levels. The chip logic can also signal that it needs a higher frequency. In this case, the power management circuit can reprogram the frequency divider circuits in

the PLL to increase the frequency, provided the power dissipation as measured by the temperature sensor is in an acceptable range. The chip logic will then function but at raised performance levels.

Refer now to FIGURE 3 which is a flow diagram of a method of dynamically maintaining chip temperatures in accordance with the present invention. A temperature threshold level (T) is chosen for normal operation of the chip logic (52). The chip temperature is sensed (54). If the chip temperature (t) is greater than the threshold (T) the flow proceeds to decision block (58). The chip logic generates a chip status signal to the power management circuit that indicates that the chip is or is not in stop clock mode. If in stop clock mode, a yes from decision block (58) causes the flow to proceed to block (60) wherein the stop clock signal is asserted. When the temperature drops to the threshold (T) a yes occurs from decision block (62) and the stop clock signal is deasserted (64).

If at decision block (58) the chip logic did not signal stop clock mode, the flow proceeds to assert the divide by P signal to lower the PLL frequency. Reprogramming the frequency divider circuit in the PLL to reduce the frequency will change the effective duty cycle of the PLL and hence will reduce the power consumption in the chip logic.

The chip logic can also signal that it needs a higher frequency (70). In this case, the power management circuit can reprogram the divide by N frequency divider circuit in the PLL to increase the frequency, provided the power dissipation as measured by the temperature sensor is lower than the threshold (T). The chip logic will then function at raised performance levels.

Refer to FIGURE 4 which is a timing diagram of the operation of the invention in stop clock mode. The system clock (10) of FIGURE 2 is running at a frequency F in this example and the chip clock is running at a fraction of the system clock frequency, $1/2 F$. The chip status signal line (46) of FIGURE 2 indicates stop clock mode. The

power management circuit (34) receives a signal (33) from the temperature sensor indicating that the temperature (t) at the chip is greater than a set threshold temperature (T). In response to the chip status signal (46) and the temperature signal (33) the power management circuit asserts the stop clock signal (44). This causes the chip clock to stop. When the temperature (t) returns to the threshold temperature (T), the stop clock signal is deasserted by the power management circuit and the chip clock is gated from the AND (36) to the chip logic and operation of the chip logic resumes.

Refer to FIGURE 5 which is a timing diagram of the operation of the invention in modify frequency mode. The system clock (10) of FIGURE 2 is running at a frequency F in this example and the chip clock is running at a fraction of the system clock frequency, $1/2 F$. The chip status signal line (46) of FIGURE 2 indicates modify frequency mode. The power management circuit (34) receives a signal (33) from the temperature sensor indicating that the temperature (t) at the chip is greater than a set threshold temperature (T). In response to the chips status signal (46) and the temperature signal (33) the power management circuit asserts the /P control signal (40). This reprograms the /P frequency divider to a higher value of P which causes the chip clock to seek a correspondingly lower frequency. When the temperature (t) returns to the threshold temperature (T), the /P control signal (40) is deasserted by the power management circuit This reprograms the /P frequency divider to the previous value of P which causes the chip clock to return to its normal frequency.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and detail may be made therein without departing from the scope of the invention.

**WHAT IS CLAIMED IS:**

1. An integrated circuit chip comprising:
 - chip logic including a functional state output;
 - sensing means for measuring a temperature of said chip;
 - clocking means having a clock output connected to said chip logic; and,
 - power management means connected to said chip logic, to said sensing means and to said clocking means;
 - said power management means including control means responsive to said sensing means and to said functional state output of said chip logic for generating a control signal to said clocking means;
 - said clocking means including selecting means responsive to said control signal for changing an operating frequency of said clocking means, depending upon a state of said control signal.
2. The integrated circuit chip in accordance with claim 1 wherein:
 - said clocking means includes programmable frequency means;and,
 - said selecting means includes programming means for changing said programmable frequency means to a different operating frequency of said clocking means.
3. The integrated circuit chip in accordance with claim 1 wherein:
 - said selecting means includes gate means at said clock output for preventing said clock output from reaching said chip logic.
4. The integrated circuit chip in accordance with claim 1 wherein:
 - said selecting means includes means for selectively either disabling said clock output or modifying an operating frequency of said clocking means, depending upon states of said control signal.
5. An integrated circuit chip comprising:
 - a chip logic including a functional state output;
 - a temperature sensing circuit;



a phase locked loop (PLL) clock having a PLL clock output connected to said chip logic; and,

a power management circuit connected to said chip logic, to said temperature sensing circuit and to said PLL;

said power management circuit including means responsive to said temperature output signal and to said functional state output of said chip logic for generating a control signal to said PLL;

said PLL including means responsive to said control signal for changing an operating frequency thereof, depending upon a state of said control signal.

6. The integrated circuit chip in accordance with claim 5 wherein:

said PLL includes a programmable frequency divider; and,

said means responsive to said control signal includes means for changing said programmable frequency divider to a different operating frequency of said PLL.

7. The integrated circuit chip in accordance with claim 5 wherein:

said means responsive to said control signal includes a gate at an output of said PLL.

8. The integrated circuit chip in accordance with claim 5 wherein:

said PLL includes a programmable frequency divider; and,

said means responsive to said control signal includes means for selectively either disabling said PLL clock output or to modifying an operating frequency thereof, depending upon states of said control signal.

9. A method of controlling heat dissipation in an integrated circuit chip having chip logic thereon, said chip logic including a functional state output; a method comprising steps of:

A. establishing a threshold temperature (T);

B. sensing a temperature (t) of said chip;

C. clocking said chip with an output of a phase locked loop (PLL) clock connected to said chip logic; and,



D. modifying said output of said PLL in accordance with a predetermined relationship between said temperature (t) and said threshold temperature (T).

10. The method in accordance with claim 9 wherein said PLL includes a programmable frequency divider, said step D including a step of:

E. programming said frequency divider to a lower frequency value upon a condition that said temperature (t) is greater than said threshold temperature (T).

11. The method in accordance with claim 9 wherein said PLL has a programmable frequency divider, said step D including the step of:

E. programming said frequency divider to a higher frequency value upon a condition that said temperature (t) is less than said threshold temperature (T).

12. The method in accordance with claim 9 wherein said step D includes a step of:

E. preventing said output of said PLL from reaching said chip logic upon a condition that said temperature (t) is less than said threshold temperature (T).

13. The method in accordance with claim 9 wherein said PLL includes a gate at an output of said PLL, said step D including a step of:

E. deactivating said gate to thereby prevent said output of said PLL from reaching said chip logic upon a condition that said temperature (t) is less than said threshold temperature (T).



ABSTRACT OF THE DISCLOSURE

Chip logic, a phase locked loop (PLL) clocking circuit, a temperature sensing circuit, and a power management circuit, are integrated on a very large scale integrated (VLSI) circuit chip. The temperature sensing circuit directly measures the chip temperature, producing a temperature output signal. The power management circuit, which is connected to the temperature sensing circuit and to the chip logic, responds to the temperature output signal and to a functional state of the chip logic to generate a control signal to the PLL. The PLL responds to the control signal to either stop the clock signal or modify the operating frequency thereof, depending upon the state of the control signal.



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FIGURE 1 PRIOR ART

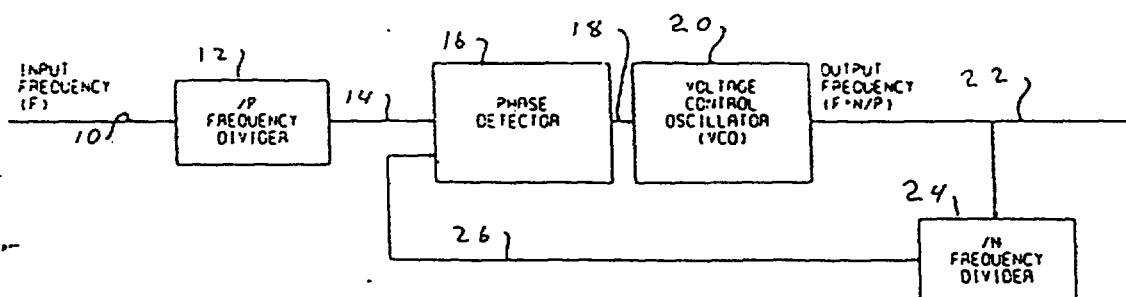


FIGURE 2

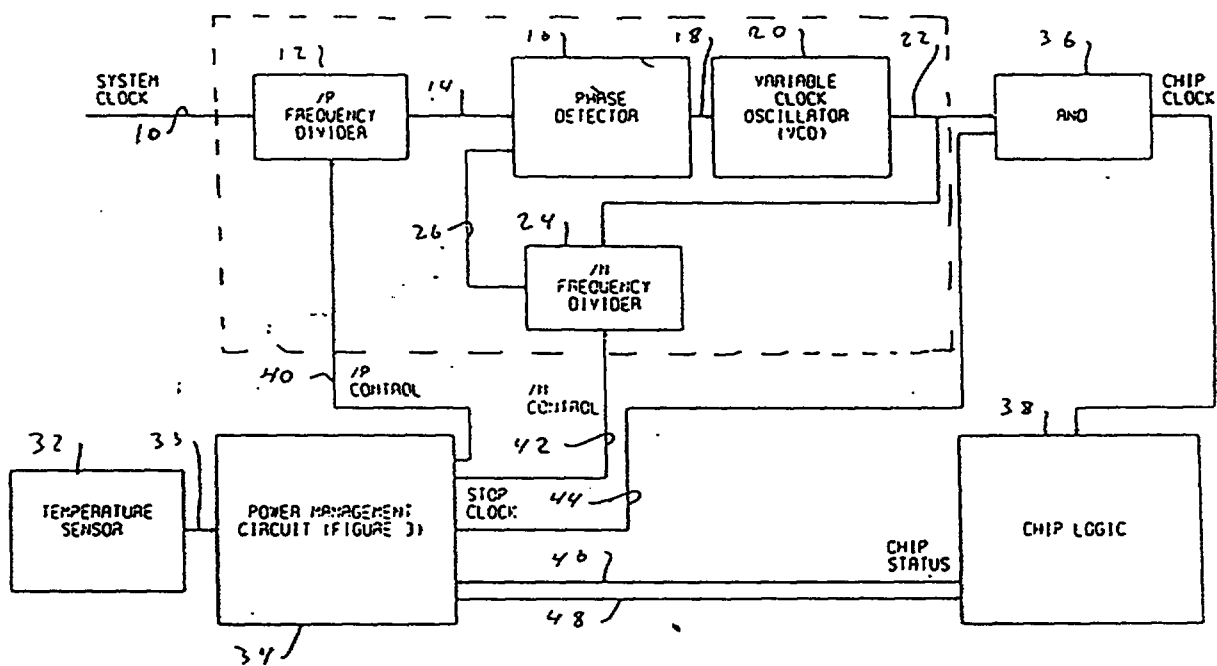
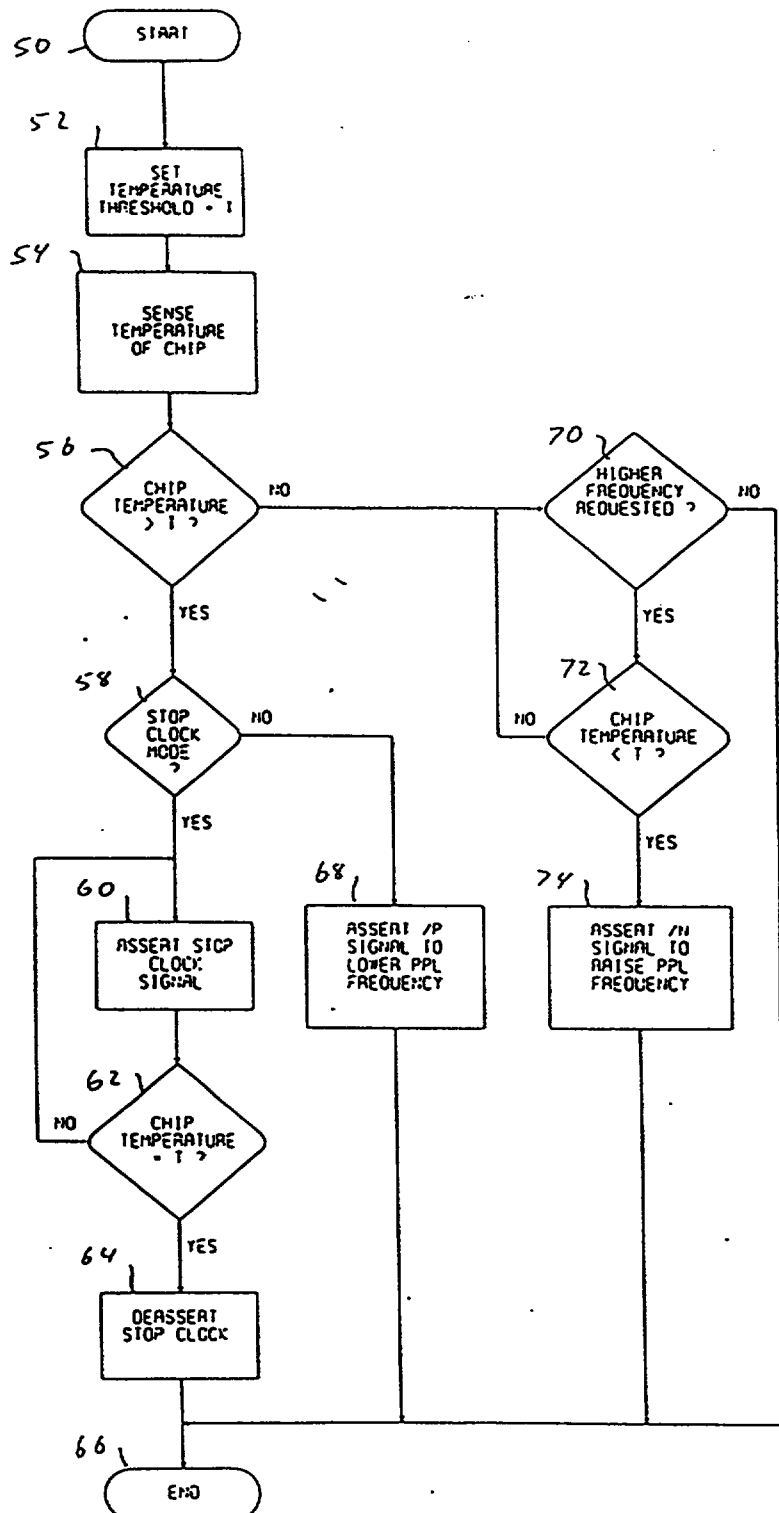




FIGURE 3



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FIGURE 4

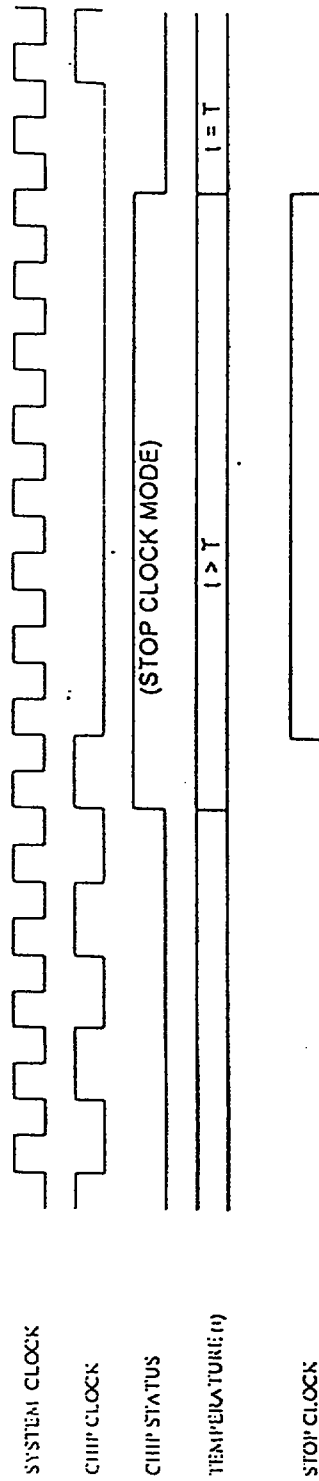
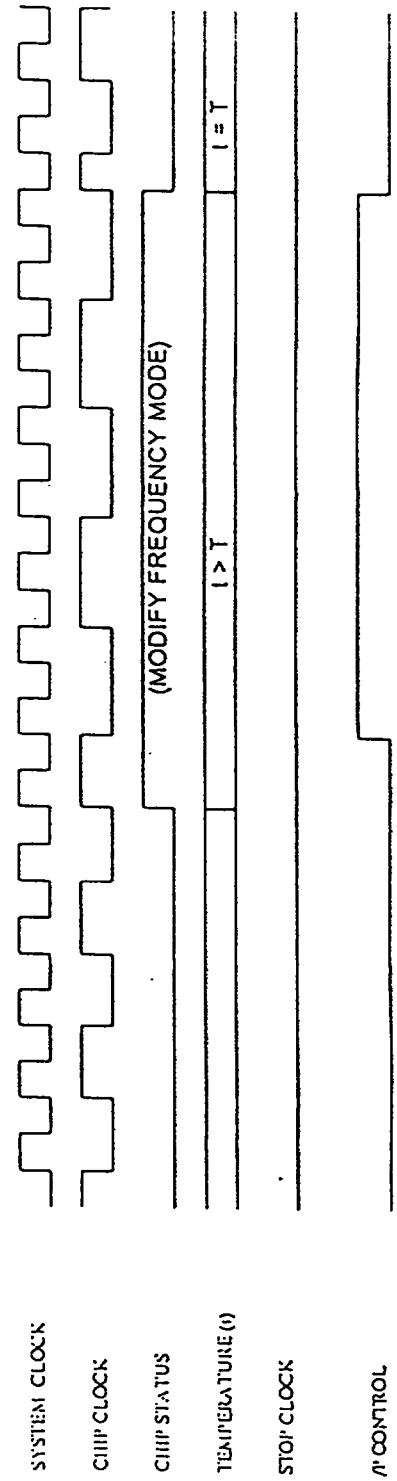


FIGURE 5



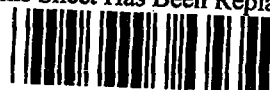
INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/02097

Box III TEXT OF THE ABSTRACT (Continuation of Item 5 of the first sheet)

Chip logic(38), a phase locked loop(PLL) clocking circuit(30) a temperature sensing circuit(32), and a power management circuit(34), are integrated on a very large scale integrated (VLSI) circuit chip. The temperature sensing circuit(32) directly measures the chip temperature, producing a temperature output signal. The power management circuit(34), which is connected to the temperature sensing circuit(32) and to the chip logic(38), responds to the temperature output signal and to a functional state of the chip logic(38) to generate a control signal to the PLL(30). The PLL(30) responds to the control signal to either stop the clock signal or modify the operating frequency thereof, depending upon the state of the control signal.

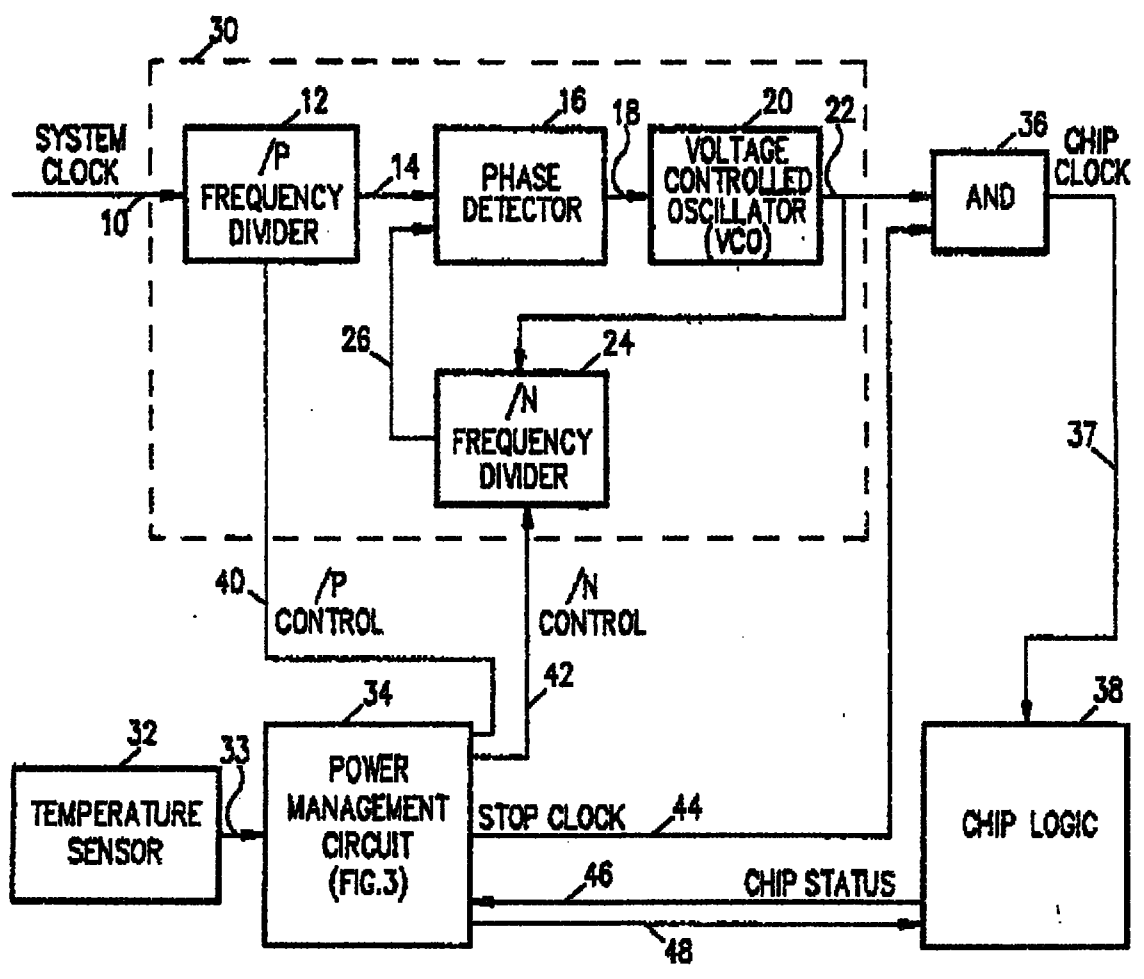
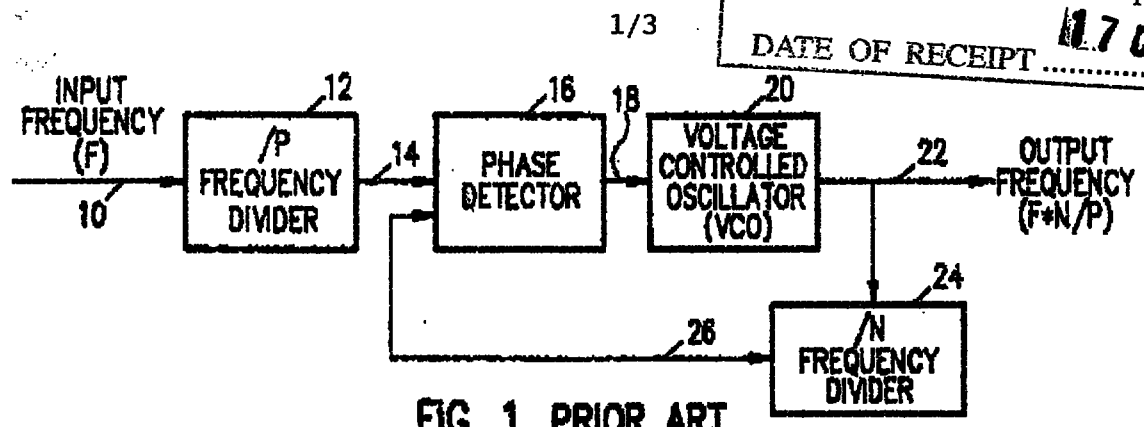
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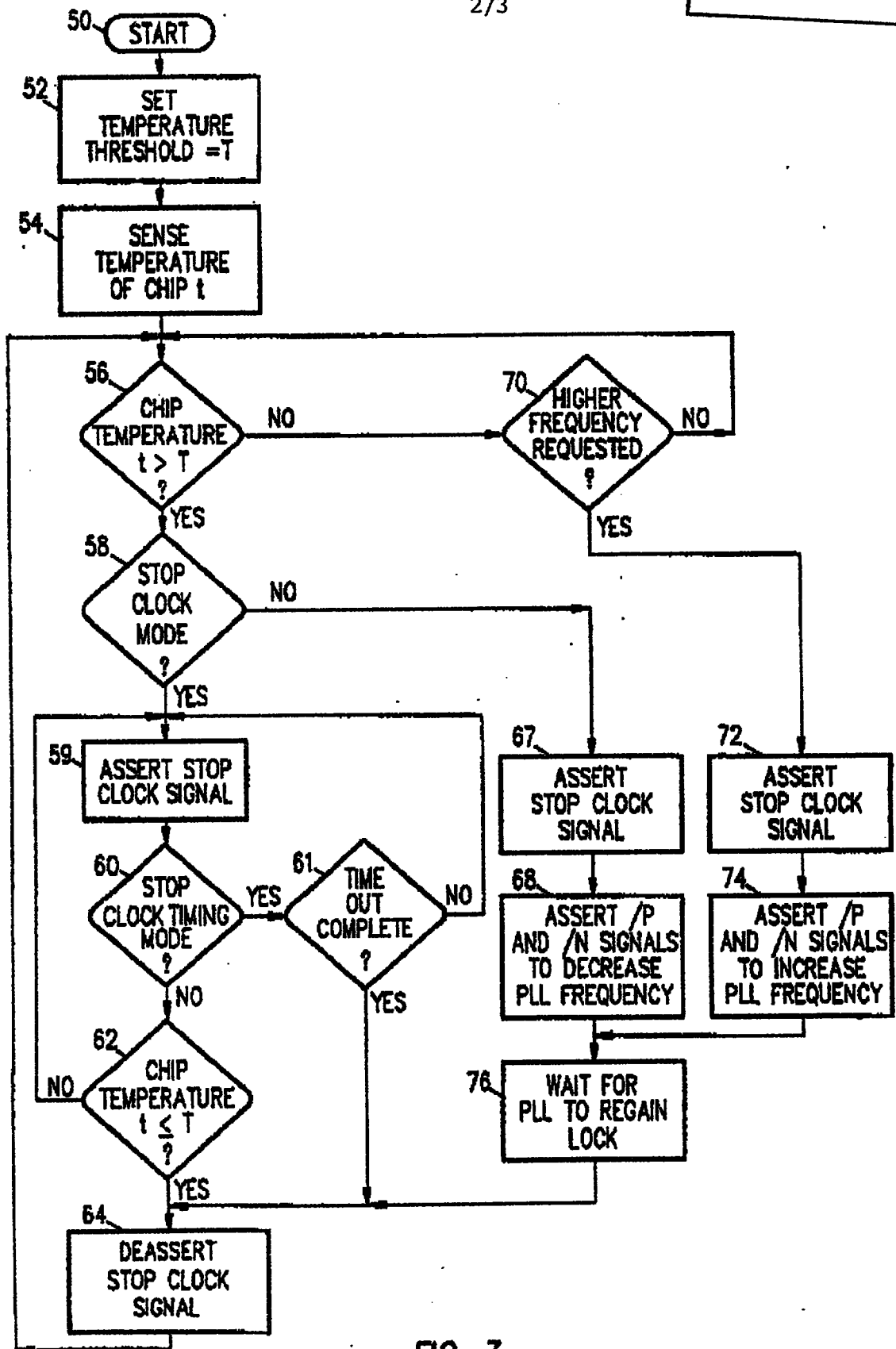
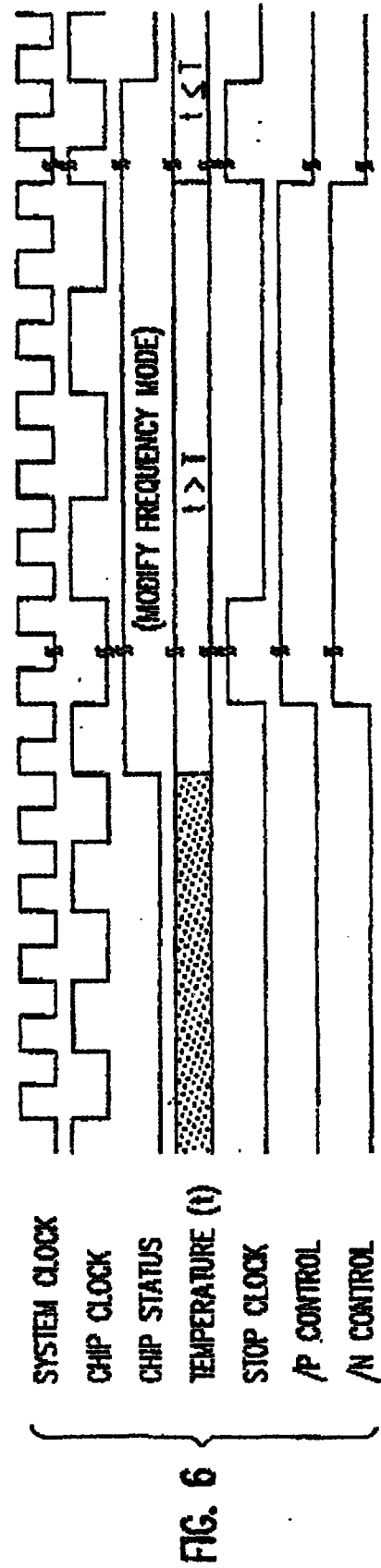
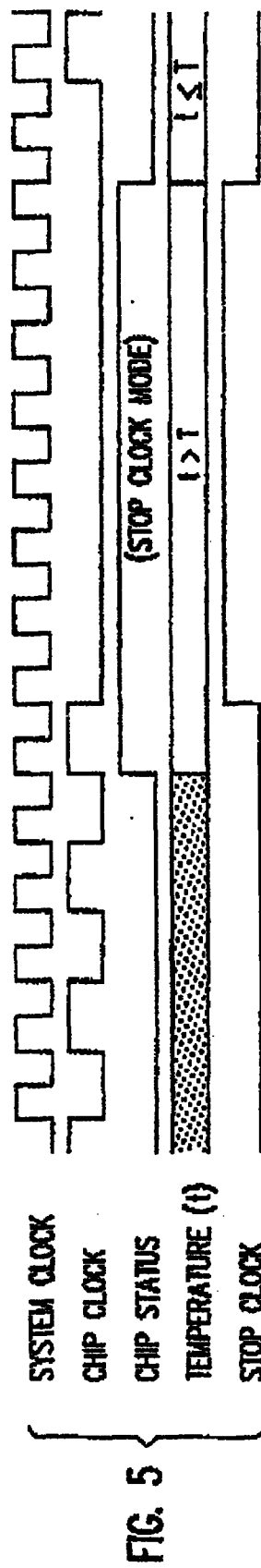
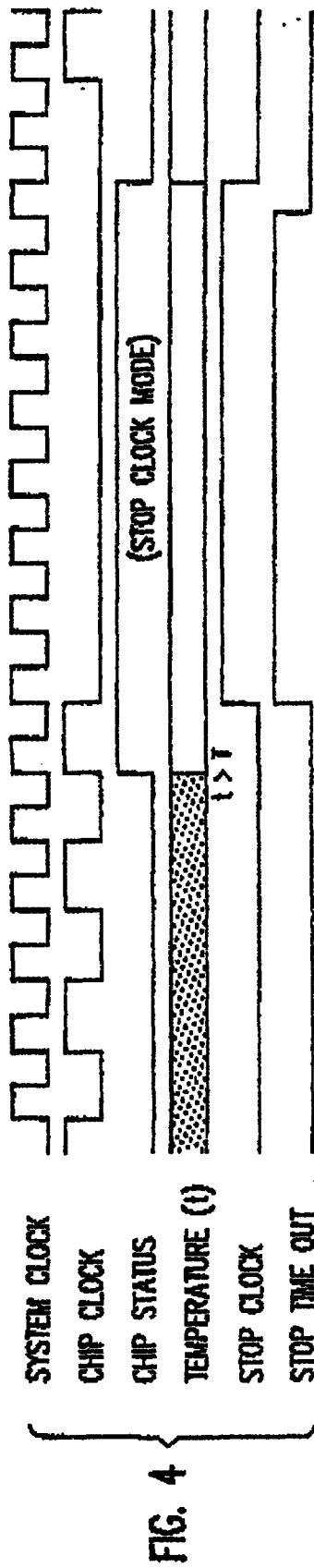


FIG. 3



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INTEGRATED DYNAMIC POWER DISSIPATION CONTROL SYSTEM FOR VERY
LARGE SCALE INTEGRATED (VLSI) CHIPS

ABSTRACT OF THE DISCLOSURE

Chip logic, a phase locked loop (PLL) clocking circuit, a temperature sensing circuit, and a power management circuit, are integrated on a very large scale integrated (VLSI) circuit chip. The temperature sensing circuit directly measures the chip temperature, producing a temperature output signal. The power management circuit, which is connected to the temperature sensing circuit and to the chip logic, responds to the temperature output signal and to a functional state of the chip logic to generate a control signal to the PLL. The PLL responds to the control signal to either stop the clock signal or modify the operating frequency thereof, depending upon the state of the control signal.

Fig. 2

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