3D INTEGRATED CIRCUIT PACKAGE AND METHOD OF FABRICATION THEREOF

FIELD OF THE INVENTION

The invention relates to three-dimensional (3D) integrated circuit packages and to a method of fabricating a 3D integrated circuit (IC) package. In particular, but not exclusively the invention relates to 3D IC packages having a plurality of stacked ICs in a single package.

BACKGROUND

3D IC integration involves integration of IC components such as memory chips, microprocessor chips and other logic devices into a single compact package. To maintain the package at a size that is usable within state of the art applications, components are bonded in a three dimensional 'face to face' configuration rather than the conventional two dimensional configuration in which substrates are spaced apart in a side by side or 'lateral' configuration. Consequently, the overall size of a 3D integrated package may be comparable to the size of a single device as fabricated according to conventional 2D IC technologies.

In addition to the benefit of a reduced size of a 3D assembly of multiple components compared with conventional 2D assemblies, 3D integration also allows generally incompatible technologies (such as GaAs and Si) to be combined in a single compact assembly, resulting in improved performance and functionality. For example, a GaAs IC may be mounted to a silicon IC in a 3D configuration to form a single package. In the alternative 2D technology, the silicon and GaAs ICs would require to be packaged separately and mounted to a printed circuit board or other substrate in a spaced apart lateral configuration. Such a configuration can result in reduced performance of systems based on 2D technologies compared with 3D technologies. This is due at least in part to an increased distance between components of respective different ICs. In addition, an increased number of physical connections are required between the ICs which can further limit performance and reliability.

Whilst 3D integration of devices is known to result in systems of smaller size and increased speed, state-of-the-art 3D integration technologies are generally more

expensive than corresponding 2D integration technologies due to increased sophistication of associated processes and relatively low process yields.

SUMMARY OF INVENTION

It is an aim of embodiments of the invention at least partially to mitigate at least some of the above-mentioned problems.

It is an aim of embodiments of the invention to provide an improved method of fabricating a 3D IC package (or '3D package').

It is an aim of embodiments of the invention to provide an improved 3D IC package.

In a first aspect of the invention there is provided a method of fabricating a 3D integrated circuit structure comprising the steps of: providing a wafer having a plurality of wafer integrated circuits formed thereon, each of said wafer integrated circuits being provided with a plurality of wafer contact elements; providing a plurality of die elements, each of said die elements being configured to be connected electrically to one of said wafer integrated circuits, said die elements each having a plurality of die contact elements; with the die elements at respective predetermined locations on the surface of the wafer the locations of the die contact elements corresponding to locations of said wafer contact elements of the wafer integrated circuits; providing a positioning member in predetermined juxtaposition with said wafer, the positioning member having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of respective die elements when provided on said wafer such that respective corresponding contact elements of the wafer integrated circuits and die elements are aligned with one another, the method further comprising the step of placing each one of a plurality of die elements on said wafer within one of a set of respective lateral boundaries defined by said formations, and bonding said die elements to said wafer.

The term 'die element' is intended to include reference to a substrate on which an integrated circuit has been formed, the substrate having been cut from a larger substrate such as a silicon wafer or any other kind of wafer on which a plurality of integrated circuits have been formed. The die element may be ready for bonding to a further

substrate. In some embodiments, the die element is ready for bonding to said further substrate without a requirement for further cutting of the die element to decrease the size of its footprint.

The term also includes reference to an integrated circuit formed directly on a substrate that is ready to be bonded to a further integrated circuit on a wafer without cutting of said substrate.

In a second aspect of the invention there is provided a structure comprising: an integrated circuit wafer having a plurality of integrated circuits formed thereon, each of said wafer integrated circuits being provided with a plurality of wafer contact elements; a plurality of die elements on said wafer, each die element having a plurality of die contact elements at locations corresponding to locations of said wafer contact elements; and a positioning member, the positioning member being provided in juxtaposition with said wafer and having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of a die element provided on said wafer within a set of said boundaries, respective corresponding contact elements of the wafer and die element being bonded to one another by means of a diffusion bond.

In a third aspect of the invention there is provided a positioning member for use in positioning a plurality of die elements on a wafer, the wafer having a plurality of wafer integrated circuits provided thereon, said integrated circuits each having a plurality of contact elements, said die elements each having a plurality of die contact elements provided thereon, with the positioning member provided in predetermined juxtaposition with said wafer, the positioning member having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of respective die elements provided on the wafer surface such that respective corresponding contact elements of the wafer integrated circuits and die elements are aligned with one another.

In an embodiment of the invention there is provided a 3D integrated circuit structure comprising a wafer integrated circuit cut from a wafer and a die element, the wafer integrated circuit having a set of wafer integrated circuit contact elements formed

thereon, the die element having a set of die contact elements formed thereon at locations corresponding to the integrated circuit contact elements, respective contact elements of the wafer integrated circuit and die element being bonded to one another by means of a diffusion bond.

Some embodiments of the invention have the advantage of reducing a cost of fabricating a 3D integrated circuit structure. Some embodiments of the invention have the advantage of allowing a decrease in the size and/or spacing of contact elements of the die element and wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention will now be described hereinafter, by way of example only, with reference to the accompanying drawings, in which:

FIG. 1 is a cross-sectional schematic diagram of an integrated circuit die element according to an embodiment of the invention.

FIG. 2 is a perspective view of a positioning member for use in some embodiments of the invention.

FIG. 3 is a cross-sectional schematic diagram of a process of fabricating a positioning member for use in some embodiments of the invention.

FIG. 4 is a cross-sectional schematic diagram of a positioning member according to some embodiments of the invention positioned over a wafer.

FIG. 5 is an exploded view of an embodiment of the invention showing a wafer, mask member and integrated circuit die element according to an embodiment of the invention.

FIG. 6 is a cross-sectional schematic diagram of an integrated circuit die element located in a positioning member on an integrated circuit wafer according to an embodiment of the invention.

FIG. 7 is a cross-sectional schematic diagram showing a process of bonding integrated circuit die elements to a wafer according to an embodiment of the invention.

FIG. 8 is a cross-sectional schematic diagram showing (a) a press member having a plurality of local protrusions and (b) a secondary press member element, provided over a protrusion member.

FIG. 9 is a cross-sectional schematic diagram showing integrated circuit elements bonded to a wafer according to an embodiment of the invention.

FIG. 10 is a cross-sectional schematic diagram of an integrated circuit according to an embodiment of the invention having a guard ring and a seal member.

FIG. 11 is a cross-sectional schematic diagram showing profiles of protrusions of positioning members according to some embodiments of the present invention.

FIG. 12 is a plan-view schematic diagram showing protrusions of a positioning member according to some embodiments of the present invention.

FIG. 13 shows a process of dicing an integrated circuit wafer to form a plurality of die elements.

FIG. 14 is a cross-sectional schematic diagram of a positioning member according to an embodiment of the invention.

FIG. 15 is a cross-sectional schematic diagram of a positioning member formed on an integrated circuit wafer according to a further embodiment of the invention.

FIG. 16 is a plan view diagram of a die element in an aperture defined by discrete post elements.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a cross-sectional schematic illustration of a discrete integrated circuit (IC) die element 100 prior to bonding to an integrated circuit wafer (or 'wafer') 200 bearing a plurality of integrated circuits. The die element 100 has a substrate 110 over which an integrated circuit layer 120 has been formed. Bondpads 130, 132 are provided over the integrated circuit layer 120 to facilitate attachment of the die to the wafer. The bondpads

130, 132 are formed from copper by means of a damascene process. The bondpads are separated from one another by an insulating medium. According to the embodiment of FIG. 1 the insulating medium is a layer of silicon oxide.

Other materials are also useful for forming the bondpads 130, 132 and insulating medium 133. Other fabrication processes are also useful.

Some of the bondpads (labelled 130) are connected to one or more electrical elements of the integrated circuit. Such bondpads 130 may be connected to said one or more electrical elements by means of via elements 131 as shown in FIG. 1.

Some of the bondpads (labelled 132) are not connected to electrical elements of the integrated circuit layer 120. Rather, such bondpads 132 are formed for the purpose of providing additional mechanical strength to the interface to be formed between the die element 100 and the wafer 200.

FIG. 2 is a schematic illustration of a positioning member 300 according to an embodiment of the invention. The positioning member 300 is used to correctly position a plurality of die elements 100 at a required location on the surface of the wafer 200 prior to bonding of the die elements 100 to the wafer 200.

In order to facilitate correct positioning of the die elements 100, the positioning member 300 is in the form of a generally planar stencil element. The positioning member 300 is formed from a silicon wafer. In some embodiments of the invention the silicon wafer from which the positioning member 300 is formed is of a comparable size to that of the integrated circuit wafer 200 to which the die elements 100 are to be bonded.

The positioning member 300 is provided with a plurality of apertures (also referred to as 'windows') 313 at locations of the positioning member 300 corresponding to positions at which die elements 100 are to be bonded to the wafer 200. Respective different apertures 313 are formed to be of a size corresponding to that of the particular corresponding die element 100 that is to be bonded at that location. It will be appreciated that die elements 100 need not all be the same size. Thus, the apertures of the positioning member 300 may be of correspondingly different sizes.

According to the embodiment of FIG. 2 the apertures 313 are formed to be around 10μm wider than the corresponding die element 100. As discussed below, the maximum difference in size between the apertures 313 and die elements 100 will depend on the size and spacing of bondpads of the die elements 100 and wafer 200, as well as the precision with which apertures 313 may be formed, and the precision with which die elements 100 may be cut from a host wafer.

According to the embodiment of FIG. 2 the apertures 313 of a positioning member are each of the same size.

In some embodiments one or more reference indices 314 are provided on each positioning member 300 in order to assist in correctly orienting the positioning member 300 with respect to a wafer 200.

FIG. 3 illustrates a process of fabricating a positioning member 300 according to some embodiments of the invention.

The positioning member 300 of FIG. 2 is formed from a silicon wafer having a thickness in the range from around 720 to around 750μm. Other thicknesses are also useful. Other materials are also useful. In some embodiments, the positioning member is formed from at least one selected from amongst glass, ceramic, quartz, and a metallic material such as aluminium, stainless steel, titanium, copper, or any other suitable material.

FIG. 3(a) shows a wafer 300 following the formation of a layer of photoresist 311 over a free surface of the wafer, and patterning of the photoresist 311 to expose portions of the wafer at locations of the wafer where it is required to form apertures 313 (FIG. 3(c)) The silicon substrate was subsequently subjected to a dry etch process to form wells 312 around 400μm in depth at these locations.

FIG. 3(b) shows the structure of FIG. 3(a) following reversal of the orientation of the wafer (also referred to as 'flipping' of the wafer) in order to expose a rear surface 301 of the wafer.

FIG. 3(c) shows the structure of FIG. 3(b) following a process of thinning of the wafer 300 from the rear surface 301 by mechanical grinding in order to form through-apertures 313 in the wafer 300.

As can be seen from FIG. 3(a), the through-apertures 313 have a width 'B' slightly larger than a corresponding width 'A' of the die element 100 to be positioned in that aperture.

FIG. 4 shows the positioning member 300 of FIG. 3 arranged to overlie a substrate 200 in a process of forming a 3D integrated circuit structure. The positioning member 300 is located so that edges 315 of apertures 313 define a boundary on the surface of the wafer 200 within which it is required to locate a corresponding die element 100.

FIG. 5 is an exploded view of the structure of FIG. 4 showing a location at which a die element 100 is to be positioned.

In some embodiments of the invention positioning member 300 is placed in direct contact with the integrated circuit wafer 200. In some embodiments of the invention the positioning member is positioned such that a gap exists between the positioning member 300 and the wafer 200.

In some embodiments a recess is provided on a side of the positioning member 300 facing the wafer 200 in order to reduce a size of a surface area of the positioning member 300 in contact with the wafer 200.

In some embodiments of the invention a spacer element is provided between the wafer 200 and the positioning member 300.

In some embodiments of the invention, die elements 100 are positioned in apertures 313 of the positioning member 300 by means of 'pick and place' apparatus. The pick and place apparatus may comprise a vacuum tweezer arrangement.

Some embodiments of the invention have the advantage that relatively low precision pick and place apparatus may be used to place die elements on an integrated circuit wafer, whilst still accomplishing relatively high precision positioning of the die elements on the wafer. This is because in some embodiments of the invention the apertures 313 of the

positioning member 300 assist in the process of correctly locating and aligning die elements 100 with bondpads 230, 232 of the wafer 200.

FIG. 6 is a cross-sectional schematic illustration of a die element 100 situated in an aperture 313 of a positioning member 300 overlying an integrated circuit wafer 200. A lateral dimension of the die element shown is A mm, whilst a corresponding dimension of the aperture 313 of the positioning member is B mm.

As can be seen from FIG. 6, the values of A and B must be selected such that the magnitude of the difference 'C' between A and B (where C = B-A) is less than or equal to the maximum permitted misalignment of bondpads 130, 132 of the die element with respect to corresponding bondpads 230, 232 of the integrated circuit wafer. Account must also be taken of other process tolerances in determining expected ranges of the values of A and B, such as the accuracy with which the apertures 313 may be defined, and the accuracy with which die elements 100 may be cut.

FIG. 7 shows the structure of FIG. 6 during a process of diffusion bonding of respective corresponding bondpads of the die element 100 and wafer 200 to one another. A die element 100 has been placed in each of the apertures 313 formed in the positioning member 300.

According to the embodiment of FIG. 7, the positioning member 300 and wafer 200 are clamped together by means of a bonding chuck 400. The bonding chuck 400 is arranged to prevent relative movement between the positioning member 300 and wafer 200.

A press member 500 is placed over the structure in abutment with a rear face of each of the die elements 100. In some embodiments the press member is pressed against the die elements 100 by means of pressing apparatus and the structure heated under vacuum conditions. In some embodiments the weight of the press member 500 alone is sufficient to promote adequate bonding without a requirement to apply further pressure to the press member 500.

The press member 500 is configured to distribute pressure evenly over the die elements 100 so as to reduce a risk of cracking or other damage to the die elements 100 or wafer

200. In some embodiments the press member 500 also serves to distribute heat evenly over the structure so that uniform heating of the die elements 100 and wafer 200 occurs.

According to the present embodiment the press member 500 is a graphite sheet and pressing apparatus is used to press the press member 500 against the die elements 100. The graphite sheet is of a thickness sufficient to maintain its mechanical integrity whilst still being sufficiently malleable to provide a substantially even pressure over the wafer 200 when the die elements 100 are pressed against the wafer 200. In some embodiments of the invention the graphite sheet is around 2mm in thickness. Other thicknesses are also useful. For example, in some embodiments graphite sheet having a thickness in the range from around 1mm to around 3mm is used. Other materials are also useful for forming the press member 500.

According to the embodiment of FIG. 7 the structure is heated to a temperature in the range of from around 250°C to around 450°C for a period of from around 60 minutes to around 30 minutes. The pressure applied to the press member 500 is in the range from around 15 to around 100psi (i.e. around 103 to around 690kPa). During the heating process, interdiffusion of copper occurs between respective bondpads of the die element 100 and integrated circuit wafer 200, resulting in the formation of a diffusion bond.

In some embodiments, the structure is heated in the presence of an inert gas atmosphere such as one of nitrogen, argon, or any other suitable gas or mixture thereof.

In some embodiments of the invention, a thickness of die elements 100 is lower than that of the positioning member 300 in which the elements 100 are placed. Consequently, in some embodiments the press member 500 to be used with such die elements is formed to have local raised formations at locations corresponding to those of the die elements 100. The formations allow the press member to contact the die elements and apply pressure thereto during the bonding process.

FIG. 8 shows an embodiment in which a thickness of die elements 100 is lower than a thickness of the positioning member 300. FIG. 8(a) shows an embodiment of the invention in which a press member 510 is provided having a plurality of local formations 512 configured to protrude into apertures 313 of the positioning member 300. This allows pressure to be applied to the die elements 100 despite their reduced thickness relative to the positioning member 300.

FIG. 8(b) shows an embodiment of the invention in which a secondary press member element 520 is provided, for use in combination with the press member 500 of FIG. 7. The secondary press member element 520 is provided with a plurality of protrusion members 522 in a corresponding manner to the formations of the press member 510 of FIG. 8(a). In use, the protrusion members 522 are urged against die elements 300 provided in apertures 313 of the positioning member 300 by applying pressure to the protrusion members 522 by means of the press member 500.

FIG. 9 shows the structure of FIG. 7 or FIG. 8 following a process of thinning of the die elements 100 using mechanical and/or chemical-mechanical planarisation (CMP) technologies. In some embodiments a dry etch or a wet etch technique may alternatively be used to thin the die elements. Other thinning processes are useful.

In some embodiments the die elements 100 are thinned down to a thickness D (FIG. 9) of around 10μm.

FIG. 10 shows the structure of FIG. 9 following a process of dicing of wafer 200 to form a 3D IC package 800. Two die-seal options and two input/output connection options are shown.

In FIG. 10 portions of a guard ring 700 may be seen. The guard ring 700 is formed to generally surround bondpads 130, 132, 232, 230 of the die element 100 and wafer 200. The guard ring is formed from a die guard ring element 701 and an IC wafer guard ring element 702 of corresponding shapes, the ring elements being provided at corresponding locations of the die element 100 and wafer 200.

In the embodiment of FIG. 10 the guard ring is formed from copper. Other materials are also useful.

Each of the ring elements 701, 702 is provided in the form of a ring structure surrounding respective contact elements of a package 800. During the bonding process, the die guard ring element 701 and wafer guard ring element 702 are joined together to form a generally air-tight seal. The presence of the guard ring 700 reduces a risk of deterioration of the bondpads 130, 132, 232, 230 due to exposure to ambient atmospheric conditions thereby reducing a risk of premature device failure.

In some embodiments of the invention an oxide spacer seal member 600 is formed instead of or in addition to a guard ring 700. In the embodiment shown in FIG. 10, both a guard ring 700 and a seal member 600 are shown, It will be appreciated that in some embodiments a guard ring 700 is provided and not a seal member 600, whilst in other embodiments a seal member 600 is provided and not a guard ring 700.

The seal member 600 is formed around a peripheral edge 103 of the die element 100 and forms a generally air tight seal between the peripheral edge 103 and a surface of the IC wafer 200.

The seal member 600 may be formed by depositing a blanket layer of silicon oxide over the structure. Portions of the blanket layer over the die element 100 and wafer 200 may then be removed to leave a seal member 600 substantially as shown in FIG. 10.

Removal of portions of the blanket layer may be performed by means of an anisotropic etching process such as a reactive ion etching (RIE) process. Alternatively, a blocking layer may be formed over the blanket layer and patterned to expose only portions of the blanket layer to be removed.

In the embodiment of FIG. 10 the blanket layer is formed from silicon oxide. Other materials are also useful, such as silicon nitride, silicon oxynitride and any other suitable material capable of blocking passage of moisture and air from an external environment of the package 800 to the bondpads 130, 132, 230, 232.

As mentioned above, in FIG. 10 two types of input/output connection to the 3D package are shown. One type of connection, shown on the left hand side of the die element 100, is a solder bump 900 provided on a further contact element. The other type of connection, shown on the right hand side of the die element 100, is an ultrasonically welded wirebond connection 950. Other types of connection are also useful.

In some embodiments of the invention edges 315 of the positioning member 300 that define apertures 313 are shaped to promote location of a die element 100 within an aperture 313 by pick and place apparatus.

FIG. 11(a) and (b) are cross-sectional schematic diagrams of portions of edges 1315, 2315 defining apertures 1313, 2313 respectively, in positioning members according to some embodiments of the invention. It can be seen that the edges are either tapered along a portion of their width between an upper surface 1316 and a lower surface 1317 as shown in FIG. 11(a), or tapered along their entire width between an upper surface 2316 and a lower surface 2317 (FIG. 11(b)).

Other cross-sectional shapes are also useful. For example curved shapes, or any other suitable shape to assist placement of the die elements may be used.

In some embodiments of the invention protrusions 3316 are provided along edges 3315 of a positioning member that define apertures 3313 (FIG. 12) of the positioning member. The protrusions are arranged to define the boundary of a region in which a die element 100 may be placed. The protrusions have the advantage that an area of potential contact between a die element 100 and a positioning member 300 may be reduced relative to some embodiments of the invention.

In some embodiments of the invention the die elements 100 are formed by cutting or cleaving a wafer 100W (FIG. 13) having a plurality of die elements 100 formed thereon. In some embodiments of the invention, cutting is performed by means of a laser cutting device. In some embodiments cutting is performed by means of a sawing operation.

The wafer 100W is cut or cleaved such that portions 103 of sidewalls of the die elements 100 that may contact positioning member 300 when the die is located within an aperture 3313 are sufficiently smooth to allow alignment of bondpads 130, 132 of the die element 100 with corresponding bondpads 230, 232 of the wafer 200 within a required tolerance.

In order to accomplish this, in some embodiments of the invention the fabrication process requires that trenches 102 are first formed in a face 101 of the wafer 100W having the integrated circuit layer 120 formed thereover (FIG. 13 (a), (b)).

The trenches are formed to have sidewalls 103 having a depth d.

Subsequently, a cut is made along line A-A (FIG. 13(a)) to release die elements 100 from the wafer 100W as shown in FIG. 13(c). The quality of the cut along line A-A according to the embodiment of FIG. 13 does not need to be as high (in terms of

smoothness at least) as that of the cut to form trenches 102. This is because the positioning member and die element are configured such that the portion of each sidewall of die element 100 formed in this cutting process will not contact the positioning member when the face 101 of the die element is in abutment with the wafer 200.

The die elements are then positioned within apertures 3313 of a positioning member 3000 with faces 101 of the die elements (bearing bondpads 130, 132) facing towards the wafer 200 to which the die elements are 100 to be bonded.

FIG. 14 is a schematic diagram showing die elements 100 positioned within apertures 3313 of positioning member 3000. As can be seen from FIG. 14, with the die element 100 located ready for bonding to wafer 200, the depth d of sidewall 103 is greater than a distance h from a surface of the wafer 200 of an upper portion of an edge 3316E of a corresponding protrusion 3316. Consequently, an area of contact between a die element 100 and a protrusion 3316 will generally always correspond to a relatively smooth sidewall 103 of a trench 102.

It will be appreciated that the precision with which die elements 100 may be positioned on a face of a wafer 200 will depend to some extent upon the precision with which corresponding edges of the protrusions 3316 and die elements 100 are formed. Thus, in some embodiments of the invention trenches 102 are formed to have relatively smooth walls (e.g. by cutting with a relatively high precision cutting system) whilst remaining portions 104 of edges of die elements 100 are formed to have relatively rough walls compared with those of the trenches 102. Consequently, relatively inexpensive cutting techniques may be made to perform cuts along lines A-A of FIG. 13(a). This assists in reducing a cost of fabricating 3D structures according to some embodiments of the invention.

In some embodiments of the invention laser cutting is used to dice wafer 100W. Laser cutting has the advantage that more precise cutting of the wafer 100W may be performed thereby facilitating more precise positioning of die elements on a wafer by means of a positioning member according to some embodiments of the invention. This in turn enables a higher number density of bondpads to be incorporated in 3D packages according to some embodiments of the invention.

In some embodiments of the invention the positioning member is formed directly on the surface of the wafer 200 to which it is required to bond a die element, rather than being formed separately. FIG. 15 is a cross-sectional schematic illustration showing a wafer 4200 on which a positioning member 4300 has been formed. According to the embodiment shown, the positioning member 4300 is formed from a porous oxide material. In some embodiments, other materials are used to form the positioning member 4300. In some embodiments, the positioning member is formed by spin coating followed by a conventional lithographic technique to form apertures in the spin coated layer. At least one selected from amongst spin-on-glass (SOG), polyimide, benzocyclobutene (BCB), photosensitive organic polymers, and epoxy or epoxy-based photoresist may be used to form the positioning member 4300.

In some embodiments of the invention, the positioning member is formed directly on the surface of the wafer 200 to a thickness of from about 50 to about 200μm. Other thicknesses are also useful.

In some embodiments of the invention, the positioning member is in the form of a plurality of spaced apart post elements 4310 (FIG. 16) arranged to define a perimeter of an area 4350 within which it is required to constrain movement of a die element placed therein.

In some embodiments the post elements are formed from a metallic material, whilst in other embodiments the posts are formed from a non-metallic material. In some embodiments the posts are formed by means of a high precision materials dispensing system such as an ultrasonic spray system or an injection dispensing system. Other systems are also useful. Other methods of forming the post elements are also useful, including methods.

An advantage of the formation of post elements is that in some embodiments of the invention an amount of material required to be introduced onto a surface of a wafer is reduced relative to a method in which a wafer is coated with a blanket layer of material that is subsequently patterned to form a positioning member.

In some embodiments, the positioning member is formed by dispensing or otherwise forming a material on the IC wafer away from an area in which integrated circuit devices such as transistors and other devices have been formed. Thus, exposure of such areas

to deposited material, etch media and other process environments can be reduced or substantially eliminated.

Once die elements have been bonded to the wafer 4200, the positioning member 4300 may be removed. Normal removal techniques may be used, such as a wet or dry etching process, or any other suitable removal technique.

Some embodiments of the invention have the advantage that a level of precision required of a pick and place instrument used to place die elements on a wafer is reduced relative to systems not employing a positioning member 300 according to embodiments of the invention.

Some embodiments of the invention have the advantage that each die element 100 may be tested before placement on a wafer 200, and malfunctioning die elements 100 rejected before placement. Consequently, only correctly functioning die elements 100 are placed on a wafer 200 according to some embodiments of the invention.

This is in contrast to known 3D package fabrication technologies in which a first entire wafer is bonded to a second entire wafer. Following bonding of the first and second wafers, the wafers are diced, resulting in 3D packages comprising two dies bonded to one another.

It will be appreciated that the yield of working packages according to such technologies will be dependent upon the yields associated with each of the separate processes of forming the die elements 100 and wafers 200, and upon the process of wafer to wafer bonding.

In a fabrication process according to embodiments of the present invention the integrated circuits being bonded to a wafer are pre-diced, allowing malfunctioning die elements 100 to be rejected. Therefore only working die elements 100 are bonded to wafers 200, resulting in a considerably higher yield of working packages compared with known 3D package fabrication technologies.

Furthermore, embodiments of the invention allow integrated circuits having different sized substrates to be bonded to one another. This is because the die elements 100 to

be bonded to an integrated circuit wafer 200 are cut in a separate process to the cutting of the integrated circuit wafer 200 following a bonding process.

In known wafer-to-wafer bonding systems the cutting operation to form die elements 100 and the cutting of the integrated circuit wafer 200 are performed after the bonding process has been performed, resulting in a 3D package having two substrates of substantially the same size bonded to one another.

It will be appreciated that the feature of some embodiments of the present invention that substrates of different sizes can be bonded together has the advantage that more efficient use of substrate material and fabrication facilities may be made.

By way of example, the number of memory ICs that can be formed on a single wafer generally exceeds the number of microprocessors that can be formed on a wafer of comparable size. The number of memory chips that may be formed on a single wafer may for example be around 1000, whilst the number of microprocessor chips may for example be around 10.

Considering the situation in which it is required to connect one memory chip IC to one microprocessor IC, In prior art processes in which wafer-to-wafer bonding is performed, followed by dicing of the pair of bonded wafers, this would result in wastage of 890 memory ICs.

In contrast, in some embodiments of the present invention each of the 900 memory ICs would be formed, tested, diced and stored ready for bonding to a wafer 200 bearing microprocessor or other devices.

It will be appreciated that a process according to some embodiments of the invention allows an increase in yield of 3D packages. Furthermore, in some embodiments of the invention a reduction in overall cost of 3D packages is achieved.

Some embodiments of the invention have the further advantage that a thickness of 3D packages may be reduced relative to prior art packages. This is because integrated circuit wafer 200 provides a support substrate for die elements 100 bonded to it, allowing the die elements 100 to be subjected to a thinning process in their final bonded locations.

This is in contrast to prior art processes in which a first integrated circuit substrate is thinned before being mounted to a second integrated circuit substrate. The risk of fracture or other damage to the first integrated circuit substrate is considerably higher than that in the case of processes according to some embodiments of the present invention in which thinning is performed as a post-bonding step.

Some embodiments of the invention have the further advantage that a reduced number of processing steps are required relative to known 3D package manufacturing technologies.

According to some known manufacturing technologies soldering processes are used in order to bond wafers together to form 3D packages. Consequently, the wafers must be subjected to a solder bump formation process whereby solder bumps are formed on bondpads of the wafer. Following the formation of solder bumps, the wafers are diced and then bonded to wafers by heating to melt the solder.

According to some embodiments of the invention the process of forming solder bumps is not required. Rather, the bondpads are formed from copper, and respective bondpads bonded to one another by a thermal diffusion bonding process that does not require the presence of solder or any other joining medium.

Some embodiments of the invention have the advantage that two integrated circuits on respective different substrates can be bonded to one another with greater positional precision with respect to one another than prior art apparatus and methods. This allows the employment of a finer pitch between contact elements of the integrated circuits to be bonded together. This allows a larger number of contact elements to be used for a given size of integrated circuit.

Some embodiments of the invention have the advantage that die elements may be placed on an integrated circuit wafer to which they are to be bonded in a more rapid manner than prior art technologies. Furthermore, some embodiments have the further advantage that the die elements may be placed on an integrated circuit wafer with greater positional accuracy than prior art 3D package technologies.

Some embodiments of the invention have the advantage that they enable a reduction in a cost of the process of fabricating 3D packages and a reduction in the time required to perform a process of fabricating a 3D package.

Throughout the description and claims of this specification, the words "comprise" and "contain" and variations of the words, for example "comprising" and "comprises", means "including but not limited to", and is not intended to (and does not) exclude other moieties, additives, components, integers or steps.

Throughout the description and claims of this specification, the singular encompasses the plural unless the context otherwise requires. In particular, where the indefinite article is used, the specification is to be understood as contemplating plurality as well as singularity, unless the context requires otherwise.

Features, integers, characteristics, compounds, chemical moieties or groups described in conjunction with a particular aspect, embodiment or example of the invention are to be understood to be applicable to any other aspect, embodiment or example described herein unless incompatible therewith.

CLAIMS

1. A method of fabricating a 3D integrated circuit structure comprising the steps of:

providing a wafer having a plurality of wafer integrated circuits formed thereon, each of said wafer integrated circuits being provided with a plurality of wafer contact elements;

providing a plurality of die elements, each of said die elements being configured to be connected electrically to one of said wafer integrated circuits, said die elements each having a plurality of die contact elements; with the die elements at respective predetermined locations on the surface of the wafer the locations of the die contact elements corresponding to locations of said wafer contact elements of the wafer integrated circuits;

providing a positioning member in predetermined juxtaposition with said wafer, the positioning member having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits,

said formations defining respective sets of lateral boundaries arranged to constrain movement of respective die elements when provided on said wafer such that respective corresponding contact elements of the wafer integrated circuits and die elements are aligned with one another, the method further comprising the step of

placing each one of a plurality of die elements on said wafer within one of a set of respective lateral boundaries defined by said formations, and bonding said die elements to said wafer.

2. A method as claimed in claim 1 wherein the step of bonding said die elements to said wafer comprises the step of forming electrical connections between respective corresponding contact elements of the wafer and said die elements.

3. A method as claimed in claim 1 wherein said die elements each comprise a generally planar substrate and said formations of the positioning member are configured to constrain lateral movement of die elements provided with the generally planar substrate of the die element substantially parallel to a surface of the wafer.

5. A method as claimed in claim 1 wherein said positioning member is formed directly on said wafer.

6. A method as claimed in claim 1 wherein said positioning member is formed separately to the wafer and is not formed directly on said wafer.

7. A method as claimed in claim 2 wherein the step of forming said electrical connections comprises the step of forming diffusion bonds directly between respective corresponding contact elements of the die elements and wafer integrated circuits.

8. A method as claimed in claim 2 wherein the step of forming said electrical connection comprises the step of applying a pressure between said die elements and said wafer by applying pressure to a press member provided in face to face contact with said die elements, said press member comprising a deformable material.

10. A method as claimed in claim 9 wherein said press member comprises a graphite sheet.

11. A method as claimed in claim 1 wherein said respective corresponding contact elements of the wafer integrated circuits and die elements comprise copper.

12. A method as claimed in claim 1 wherein said formations of the positioning member each comprise a plurality of pillar elements.

13. A method as claimed in claim 1 wherein said formations of the positioning member comprise apertures formed in a generally planar member.

14. A method as claimed in claim 1 wherein the positioning member is formed from at least one selected from amongst glass, ceramic, quartz, aluminum, stainless steel, titanium, copper, a porous oxide, spin-on-glass (SOG), polyimide, benzocyclobutene (BCB), photosensitive organic polymers, epoxy photoresist and epoxy-based photoresist.

15. A method a claimed in claim 1 comprising the step of subsequently reducing a thickness of said die elements or said wafer by means of a thinning process.

16. A method as claimed in claim 1 comprising the step of providing a first seal element on each of said die elements around the contact elements of each of said die elements, and a second seal element around the contact elements of each wafer

integrated circuit, the method further comprising the step of bonding the first and second seal elements to one another to form a gastight seal between each die element and the wafer thereby to prevent ingress of air and moisture to said contact elements.

17. A method as claimed in claim 16 wherein the first and second seal elements each comprise a metallic material, preferably copper.

18. A method as claimed in claim 1 comprising the step of forming a seal member around a peripheral edge of each die element, said seal member providing a gastight seal between the die element and the wafer thereby to prevent ingress of air and moisture to said contact elements.

19. A method as claimed in claim 18 wherein the step of forming said seal members comprises the step of forming a blanket layer of a material over said structure, and subsequently removing portions of said blanket layer by means of an anisotropic etch process, whereby the seal member is provided by portions of the seal member that remain following said etch process.

20. A method as claimed in claim 1 comprising the step of bonding a plurality of die elements to each wafer integrated circuit.

21. A method as claimed in claim 1 further comprising the step of cutting said wafer thereby to form a plurality of free standing 3D integrated circuit structures each comprising a portion of said wafer, each portion of said wafer having an integrated circuit formed thereon, said integrated circuit having one or more die elements bonded thereto.

22. A method as claimed in claim 21 wherein at least one of said one or more die elements is of a size smaller than that of the portion of the wafer to which it is bonded.

23. A method as claimed in claim 1 wherein the step of providing a plurality of die elements comprises the step of providing a die element wafer having a plurality of die element integrated circuits formed thereon;

forming trenches of a first depth around each die element integrated circuit on a side of the wafer on which said circuits are formed thereby to define a perimeter of each die element;

subsequently separating the die elements from each other along said perimeter of each die element by a cutting or cleaving operation.

24. A method as claimed in claim 23 wherein said trenches are provided with sidewalls, and said formations of said positioning member are arranged whereby with the positioning member in said predetermined juxtaposition with said wafer, said lateral boundaries are defined by a portion of the positioning member having a height above the integrated circuit wafer surface that is up to a value less than or equal to said first depth of said trench, whereby with a die element provided on the wafer surface within a set of said lateral boundaries, contact between the die element and said formations is limited to portions of the die element that formerly provided said sidewalls of said trenches.

25. A method as claimed in claim 24 wherein the positioning member comprises a generally planar element and said formations comprise a plurality of apertures, each aperture having a lip along at least a portion of a perimeter thereof, said lip being arranged whereby with the positioning member in said predetermined juxtaposition with said wafer and said die element in contact with said wafer surface within a set of said lateral boundaries, contact between said formations and said die element is limited to said lip.

26. A method as claimed in claim 25 wherein said lip is provided around an entire perimeter of each of said apertures thereby to define said lateral boundaries of said positioning member.

27. A structure comprising:

an integrated circuit wafer having a plurality of integrated circuits formed thereon, each of said wafer integrated circuits being provided with a plurality of wafer contact elements;

a plurality of die elements on said wafer, each die element having a plurality of die contact elements at locations corresponding to locations of said wafer contact elements; and

a positioning member, the positioning member being provided in juxtaposition with said wafer and having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of a die element provided on said wafer within a set of said boundaries,

respective corresponding contact elements of the wafer and die element being bonded to one another by means of a diffusion bond.

28. A positioning member for use in positioning a plurality of die elements on a wafer, the wafer having a plurality of wafer integrated circuits provided thereon, said integrated circuits each having a plurality of contact elements, said die elements each having a plurality of die contact elements provided thereon,

with the positioning member provided in predetermined juxtaposition with said wafer, the positioning member having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of respective die elements provided on the wafer surface such that respective corresponding contact elements of the wafer integrated circuits and die elements are aligned with one another.

29. A structure as claimed in claim 28 wherein said positioning member is formed directly on said wafer, preferably from at least one selected from amongst a porous oxide, spin-on-glass (SOG), polyimide, benzocyclobutene (BCB), photosensitive organic polymers, and epoxy or epoxy-based photoresist.

30. A structure as claimed in claim 28 wherein said positioning member is formed separately from the wafer and is not formed directly on said wafer, preferably from at least one selected from amongst a glass, ceramic, quartz, aluminum, stainless steel, titanium, copper and a porous oxide.

3D INTEGRATED CIRCUIT PACKAGE AND METHOD OF FABRICATION THEREOF

ABSTRACT

A method of fabricating a 3D integrated circuit structure comprising the steps of: providing a wafer having a plurality of wafer integrated circuits formed thereon, each of said wafer integrated circuits being provided with a plurality of wafer contact elements; providing a plurality of die elements, each of said die elements being configured to be connected electrically to one of said wafer integrated circuits, said die elements each having a plurality of die contact elements; with the die elements at respective predetermined locations on the surface of the wafer the locations of the die contact elements corresponding to locations of said wafer contact elements of the wafer integrated circuits; providing a positioning member in predetermined juxtaposition with said wafer, the positioning member having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of respective die elements when provided on said wafer such that respective corresponding contact elements of the wafer integrated circuits and die elements are aligned with one another, the method further comprising the step of placing each one of a plurality of die elements on said wafer within one of a set of respective lateral boundaries defined by said formations, and bonding said die elements to said wafer.

(FIG. 1)