

HEMT PIEZOELECTRIC STRUCTURES WITH ZERO ALLOY DISORDER

This invention relates to manufacturing of semiconducting substrates for use in making electronic components.

The technical domain of the invention may be defined
5 in general as preparation of layers of semiconducting materials based on nitride on a support.

General presentation of prior art

Semiconducting materials based on nitrides of III
10 elements in the periodic table occupy an increasingly important place in the electronic and optoelectronic fields.

These materials intended for manufacturing of HEMT (High Electron Mobility Transistors) are used to make
15 electronic circuits dedicated to high frequency and high power applications.

Such materials based on nitrides of III elements present a number of advantages - as an illustration, they

do not require doping the material contrary to what is known in materials such as materials based on arsenide.

An example HEMT made on a semiconducting material based on III-N, or nitrides of III elements ((In, Ga, Al)/N) is shown in Figure 1.

The material includes a barrier layer 20 made of Gallium and Aluminium nitride (AlGaN) developed on a channel layer 21 made of Gallium nitride (GaN), itself developed on a support 22.

The HEMT transistor also comprises a source electrode 23 and a drain electrode 24 on the front face 25 of the barrier layer 20 of AlGaN, and a grid electrode 26 between the source electrode 23 and the drain electrode 24.

Due to the presence of Aluminium in the AlGaN barrier layer 20, the barrier layer has a wider prohibited energy band than the channel layer 21 of GaN. Silicon impurities in the AlGaN barrier layer 20 supply electrons to the crystal that tend to accumulate in a region 27 with the lowest potential (a quantum well) just under the interface 28 between the AlGaN barrier layer 20 and the GaN channel layer 21.

This forms a sheet of electrons 27 that forms a two-dimensional electron gas (2 DEG). The mobility of electrons in this gas is high since they are physically separated from silicon atoms residing in the AlGaN barrier layer 20.

Although the first studies on semiconducting materials based on III-N were carried out in the 1970s, the real advantage of this type of material only became clear after p type conduction was obtained in a GaN channel layer

followed by marketing of blue diodes by Nichia Chemicals [1].

Devices based on AlGaN/GaN structures with two-dimensional electron gases [9,11] now have much better characteristics than the corresponding products in other material systems [6,7].

Semiconducting materials based on III-N form a very innovative semiconductor system with the following specific features:

- 10 - a prohibited band width varying from 0.8 eV to 6.2 eV,
- the possibility of making continuous alloys of AlGa_N, thus enabling the production of heterostructures with a large degree of freedom,
- 15 - a very weak crystalline mesh parameter mismatch between gallium nitride (Ga_N) and Aluminium nitride (Al_N), so that complex structures can be made without creation of crystalline defects:

$$\Delta a/a = (a_{\text{GaN}} - a_{\text{AlN}})/a_{\text{GaN}} = 1\%$$

- 20 where:
 - a_{GaN} is the mesh parameter of Ga_N,
 - a_{AlN} is the mesh parameter of Al_N,
 - $\Delta a/a$ is the mesh parameter mismatch (a mesh parameter mismatch less than or equal to 1% is the sign of a quasi pseudomorphic coherent growth),
- 25 - excellent electronic properties (good mobility of electrons, high saturation speed, high breakdown field),
- excellent thermal and chemical stability,
- good thermal properties (dissipation of heat),

- the presence of a strong polarisation field to obtain large charge transfers in two-dimensional electron gases (2 DEG).

Therefore, semiconducting materials based on III-N
5 have better performances than semiconducting materials based on "classical" III-V, particularly concerning the mobility of charge carriers and the charge density.

Mobility of charge carriers

10 From the point of view of production of the material, mobility and the current density per unit surface area of AlGa_N/Ga_N structures will be governed by four preponderant parameters:

- the defect density in the layers ^[18],
- 15 - the surface roughness (RMS) and the chemical roughness at the AlGa_N/Ga_N interface (alloy disorder in the AlGa_N barrier layer) ^[19,20],
- the distance from the electron gas (2 DEG) to the interface, that can be modulated by inserting a spacer
20 (undoped potential barrier) to limit diffusion of electrons at the interface ^[21],
- the state of strain in the HEMT structure (in the AlGa_N and Ga_N layers) that has an influence on the piezo-electric field ^[22] (there is also an intense spontaneous
25 polarisation field in wurtzite heterostructures ^[23] that participate in the charge transfer).

Charge density

Exceptional charge transfers observed in AlGaN/GaN structures ($n_s \sim 10^{20} - 3 \times 10^{13} \text{ cm}^{-2}$) are induced by a particular polarisation field: the piezoelectric polarisation field. This is also referred to piezo induced High Electron Mobility Transistor (Piezo-HEMT).

AlGaN/GaN structures have a Wurtzite type hexagonal structure. Piezo-electric polarisation originates from non-centrosymmetry of this Wurtzite structure.

There are several models that describe the piezo-electric polarisation phenomenon. The simplest is the Ambacher et al. model ^[22] that is briefly summarised below with reference to Figure 2. Starting from this model, it is possible to determine what material parameters have an influence on the charge density of transistor structures made on III-N based semiconducting materials.

A substrate comprising a Ga (Al) layer in the front face 1 or growth face is shown in Figure 2.

This substrate comprises a support 2, a GaN channel layer 3, and an AlGaN barrier layer 4. The support 2 is a semiconducting or non-semiconducting material. For example, the support 2 may be made of SiC or Si. The GaN channel layer 3 is deposited on the front face 5 of the support 2. This GaN channel layer 3 is relaxed. The AlGaN barrier layer 4 is located on the front face 6 of the GaN channel layer 3. This AlGaN barrier layer 4 is strained. The AlGaN barrier layer 4 is an $\text{Al}_x\text{Ga}_{1-x}\text{N}$ type alloy where x represents the molar fraction of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy.

If there is no external electric field, the total polarisation field P of an $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ structure along an axis $[0001]$ is equal to the sum of a spontaneous polarisation field P_{SP} and a piezoelectric polarisation field P_{PE} induced by strain in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer 4.

The spontaneous polarisation field $P_{\text{SP}}(x)^{[23]}$ in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer 4 is expressed as a function of spontaneous polarisation constants of Gallium nitride (GaN) and Aluminium nitride (AlN), assuming a linear variation:

$$P_{\text{SP}}(x) = -0.52x - 0.029 \text{ C/m}^2 \quad (\text{I})$$

where x represents the molar fraction of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy.

The sign of the spontaneous polarisation field P_{SP} will depend on the polarity of the crystal. In the classical case of a substrate 1 comprising a Gallium layer (Aluminium, Indium) in front face (growth face), the spontaneous polarisation field P_{SP} is negative (in other words is opposite to the growth axis $[0001]$). Therefore the spontaneous polarisation field P_{SP} points from the growth face 1 towards the support 2.

The piezo-electric polarisation field $P_{\text{PE}}(x)$ in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer 4 is expressed as a function of piezoelectric constants $e_{33}(x)$ and $e_{31}(x)$ of the alloy $\text{Al}_x\text{Ga}_{1-x}\text{N}$:

$$P_{\text{PE}}(x) = e_{33}(x)\epsilon_{zz} + e_{31}(x)(\epsilon_{xx} + \epsilon_{yy}) \quad (2)$$

where:

- x represents the molar fraction of the alloy $\text{Al}_x\text{Ga}_{1-x}\text{N}$,

- $e_{33}(x)$ and $e_{31}(x)$ are the piezo-electric constants of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy,

• ϵ_{xx} , ϵ_{yy} and ϵ_{zz} represent deformations of the length, width and height of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy.

The piezoelectric constants $e_{33}(x)$ and $e_{13}(x)$ of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ are calculated from the piezoelectric constants e_{33} and e_{13} of GaN and the piezoelectric constant e_{33} and e_{13} of AlN.

As an example, a table giving the piezoelectric constants of GaN and of AlN is:

Material	P_{SP} (C/m ²)	e_{33} (C/m ²)	e_{31} (C/m ²)
AlN	- 0.081	1.46	-0.60
GaN	-0.029	0.73	-0.49

Table II: piezoelectric constants of GaN and AlN [23]

10 If the deformations ϵ_{ij} are developed in equation (2) as a function of the elastic constants $C_{ij}(x)$ of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy and the mesh parameters of the GaN channel layer and the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer, the result is:

$$P_{PE}(x) = 2 \frac{a(x)-a_0}{a_0} (e_{31}(x)-e_{33}(x) \frac{C_{13}(x)}{C_{33}(x)}) \quad (3)$$

15 where: • a_0 represents the mesh parameter of GaN,

• $a(x)$ represents the mesh parameter of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy,

• $C_{13}(x)$ and $C_{33}(x)$ represent the elastic
20 constants of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy.

The elastic constants $C_{13}(x)$ and $C_{33}(x)$ of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloy are calculated starting from elastic constants C_{13} and C_{33} of GaN and AlN assuming a linear variation as a function of x . The values of the elastic constants C_{13} and C_{33} of GaN
25 and AlN commonly used in the literature are as given by

Wright et al. These values agree well with experimental data, particularly data by Polian et al. for GaN.

As an example, a table giving the elastic constants of GaN and of AlN is:

5

Material	C ₁₃	C ₃₃	Reference
AlN	108	373	Wright et al.
GaN	103	405	Wright et al.

Table III: Elastic constants of GaN and AlN

In equation (3), the quantity " $e_{31}(x) - e_{33}(x) \times (C_{13}(x)/C_{33}(x))$ " is negative for the entire composition range. Consequently, the piezo-electric polarisation $P_{PE}(x)$ will be negative for the barrier layer of $Al_xGa_{1-x}N$ strained in tension.

The polarisation discontinuity at the $Al_xGa_{1-x}N/GaN$ interface between the barrier layer of $Al_xGa_{1-x}N$ and the channel layer of GaN generates a positive charge distribution at the $Al_xGa_{1-x}N/GaN$ interface, for which the density is written as follows:

$$\sigma = P(AlGaN) - P(GaN)$$
$$\sigma = P_{SP}(AlGaN - P_{PE}(AlGaN) - P_{SP}(GaN) \tag{4}$$

Equations (1), (3) and (4) are used to calculate the charge density σ/e (where $e = 1.6 \times 10^{-19}$ C) for strained structures.

If the Aluminium content in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer is between 5% and 30%, the charge density induced by the polarisation is between $2 \times 10^{12} \text{ cm}^{-2}$ and $2 \times 10^{13} \text{ cm}^{-2}$.

In order to compensate for this high positive charge, a two-dimensional electron gas will be formed at the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ interface 6. Therefore, there is an additional contribution to that induced by the band structure.

The simple model by Ambacher et al described above demonstrates dependence between the charge density induced by polarisation and the concentration of Aluminium in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer 4.

Thus, the charge carrier mobility and charge density properties of transistor structures obtained starting from a III-N-based semiconducting material depend on parameters such as the chemical roughness at the $\text{AlGaIn}/\text{GaIn}$ interface and the Aluminium concentration in the AlGaIn barrier. These parameters are related to methods of producing the semiconducting material based on III-N, and generate problems with the reliability of transistor structures made on said semiconducting material.

Figure 6a is a sectional view illustrating a semiconducting material of the prior art based on III-N. This material comprises a classical barrier layer 40 on a channel layer 41.

A drawback of the semi-conducting material of the prior art is the non-homogeneous distribution of Ga and Al atoms in the barrier layer 40. This is due in particular to the difference in behaviour of Ga and Al in terms of diffusion capacity, and to segregation effects which follow this difference in behaviour.

This non homogeneous distribution of Ga and Al atoms in the barrier layer 40 induces non-homogeneity of the piezoelectric field 38 at the interface 39 between the channel layer 41 and the barrier layer 40. Indeed, the
5 direction and the intensity of the piezoelectric field locally depend on the distribution of Ga and Al atoms in the barrier layer 40.

The non-homogeneity of the piezoelectric field induces fluctuations in the electronic density at this interface
10 39. As a consequence, the power output by a transistor structure made on the semi-conducting material comprising this AlGaN barrier layer will be distributed non-homogeneously.

Moreover, the non-homogeneous distribution of Ga and
15 Al atoms induces non-homogeneity of the electron distribution (particularly in the channel layer).

Document W002/093650 describes a process for making a semi-conducting structure comprising a barrier layer including an alternation of layers of GaN and AlN, each
20 layer of AlN and GaN being in the range of 5 to 20 Angstrom thick.

As will be apparent when reading the description of the present invention, an embodiment of W002/093650 thus shares with the present invention alternating layers of
25 binary materials for making a larger layer of material.

The process disclosed in W002/093650 allows increasing the electron mobility within the structure.

However, W002/093650 does not address the issue of increasing the homogeneity of the electron distribution
30 (particularly in the channel layer).

And in this respect the process disclosed by WO02/093650 does not provide a solution for increasing the homogeneity of the electron distribution in the layers of the structure. It will be appreciated that this known
5 process does not suggest a solution as provided by the invention, which specifically addresses the issue of homogeneity and which provides specific means to treat this issue.

Moreover, WO02/093650 does not allow increasing
10 homogeneity of the piezoelectric field at the interface between the barrier layer and the channel layer and thus does not allow limiting the fluctuations in the electronic density at this interface.

It can also be noted that other processes disclose
15 alternating elementary layers of different materials for making a larger layer.

And some of these known processes even disclose selecting very thin elementary layers - which is an advantageous feature of the invention. Reference is made in
20 this respect to US6100542. However, a known process such as the one disclosed in US6100542 does not address layers of materials based on nitrides, but materials based on arsenide.

It thus appears that the existing processes for making
25 structures with layers based on nitrides are associated to some limitations. It is a general object of the invention to address these limitations.

And more precisely, an aim of the present invention is to increase the homogeneity of the electron distribution,
30 particularly in the channel layer.

Another aim of the invention is to increase the homogeneity of the piezoelectric field at the interface between the barrier layer and the channel layer and thus to homogenise the electronic density at this interface.

5 Another aim of the invention is to improve the electronic properties of semi-conducting materials based on III-N, particularly by improving methods of producing the semi-conducting material based on III-N.

10 Summary of the invention

The invention relates to a semiconducting substrate based on elements in columns III and V in the periodic table, to be used for example for manufacturing of HEMT of HEMT type transistor structures, comprising a support, a
15 channel layer on the support and a barrier layer on the channel layer,
wherein the barrier layer is composed of an alternation, at the atomic scale, of layers of first and second III-V binary semi-conducting alloys.

20 Thus, and as will become clearer in the following, the alternation of layers of binary alloys in the barrier layer has the following advantages:

- a reduced alloy disorder at the atomic scale,
- zero alloy non-homogeneities at the nanometric
25 scale and at the microscopic scale,
- a perfect alloy order according to a privileged crystalline axis,
- a maximum piezoelectric field along a preferred crystalline axis,
- 30 - an optimum electron piezoelectric injection,

- a very uniform electronic density per unit surface area,

- a reduced electronic diffusion at interfaces and in the barrier layer due to the reduced alloy disorder,

5 - improved structure reliability due to the absence of any alloy non-homogeneities.

Indeed, by improving the distribution of Ga and Al atoms in the barrier layer, it allows increasing the homogeneity of the electron distribution. It also allows
10 increasing the homogeneity of the piezoelectric field at the interface between the barrier layer and the channel layer, and thus to homogenise the electronic density at this interface.

More particularly, by limiting the parameters:

15 - of roughness at the interface between the channel layer and the barrier layer,
 - of non-homogeneity of the Aluminium concentration in the barrier layer, and
 - of non homogeneity of Gallium concentration in
20 the channel layer,

it allows increasing the homogeneity of the piezoelectric field as described above.

Furthermore, it will be understood in the following that when a layer A is mentioned as being "on" a layer B,
25 it may be directly on layer B, or it may be located above layer B and separated from said layer B by one or several intermediate layers.

It will also be understood that when a layer A is said to be "on" a layer B, it may cover the entire surface of
30 the layer B, or a portion of said layer B.

Preferred non-limitative aspects of the semiconductor according to the invention are as follows:

- the channel layer comprises an alternation, at the atomic scale, of layers of third and fourth III-V binary semi-conducting alloys
- the semi-conducting substrate further includes a buffer layer between the support and the channel layer, the buffer layer comprising an alternation, at the atomic scale, of layers of fifth and sixth III-V binary semi-conducting alloys;
- the number of atomic monolayers in each binary alloy of the alternation of the barrier layer or of the channel layer or of the buffer layer is comprised between 1 and 20;
- the number of atomic monolayers in each binary alloy of the alternation of the barrier layer or of the channel layer or of the buffer layer varies between a first value on a back face of the barrier layer or of the channel layer or of the buffer layer, and a second value on a front face of the barrier layer or of the channel layer or of the buffer layer, the back face being closer to the support than the front face;
- the first and second values are comprised between 1 and 20;
- the first, second, third, fourth, fifth and sixth binary alloys are chosen from among AlN, GaN, BN, and InN;
- the barrier layer further includes a layer of III-V semi-conducting ternary alloy;
- the alternation, at the atomic scale, of layers of first and second III-V semi-conducting binary alloys is

located between the support and said layer of III-V semi-conducting ternary alloy;

- the barrier layer comprises a plurality of layers of III-V semi-conducting ternary alloy, each layer of III-V semi-conducting ternary alloy being located between a layer of the first binary alloy and a layer of the second binary alloy of the alternation;

- the barrier layer further includes a layer of the III-V semi-conducting ternary alloy on the alternation, at the atomic scale, of layers of first and second III-V semi-conducting binary alloys;

- the channel layer further comprises a plurality of layers of III-V semi-conducting ternary alloy, each layer of III-V semi-conducting ternary alloy being located between a layer of the third binary alloy and a layer of the fourth binary alloy of the alternation;

- the number of atomic monolayers in each layer of the ternary alloy located between two layers of the binary alloys is comprised between 1 and 5;

- the channel layer is made of a layer of ternary alloy of AlGa_N, or InGa_N, or AlBN, or InBN, or InAlN;

- the channel layer is made of a layer of binary alloy of GaN, or AlN, or BN, or InN;

- the semi-conducting substrate further comprises a buffer layer between the support and the channel layer, the buffer layer being made of a layer of binary alloy of GaN, or AlN, or BN, or InN;

- the semi-conducting substrate further comprises a buffer layer between the support and the channel layer, the

buffer layer being made of a layer of ternary alloy of AlGa_N, or InGa_N, or AlBN, or InBN, or InAl_N

- the support is made of a material chosen from among Si, SiC, AlN, Sapphire, and GaN;

5 - the thickness of the barrier layer (53) is comprised between 2nm and 500 nm.

The invention also relates to a method for preparation of a semi-conducting substrate comprising a support, a channel layer on the support and a barrier layer on the
10 channel layer, wherein the methods comprises the following step (no order being imposed):

a. creation of an initial barrier layer by:

- i) deposit of at least one atomic monolayer of a first binary alloy;
- 15 ii) deposit of at least one atomic monolayer of a second binary alloy;
- iii) repetition of steps i) and ii) if necessary until the required thickness is obtained.

One aspect of the above method is that the semi-
20 conducting substrate is that it is obtained by individually fitting monolayers of AlN binary alloy and monolayers of GaN binary alloy in order to obtain a barrier layer as homogeneous as possible. In this respect it is important to notice that the invention addresses the structure at the
25 detailed scale of the monolayer, and an accurate definition of a "monolayer" shall be provided further in this text.

Preferred but non-limitative aspects of the method according to the invention are as follows:

- the method further comprises the step of creation of at least one layer of ternary alloy in or on the initial barrier layer;
- the step of creation of said layer of ternary alloy comprises the deposit of a layer of a ternary alloy;
- the step of creation of said layer of ternary alloy comprises thermal treatment of atomic monolayers of first and second binary alloys deposited in i) and ii);
- the thermal treatment is carried out after at least some deposits of the second binary alloy:
 - at a surface temperature between 0°C and 300°C above to the temperature of creation of monolayers of first and second binary alloys;
 - under vacuum or ultra-high vacuum between 10^{-8} Torr and 10^{-1} Torr ;
 - under a gas mixture flow comprising ammoniac NH_3 or nitrogen molecule N_2 or hydrogen molecule H_2 at a pressure comprised between 10^{-8} Torr and the pressure of 1 kBar;
- in presence of a NH_3 , N_2 or H_2 plasma;
- the thermal treatment of atomic monolayers of first and second binary alloys deposited in i) and ii) is made after the step of creation of the initial barrier layer;
- the method further comprises the step of creation of a channel layer by deposit of a binary alloy of GaN, or AlN, or BN, or InN;
- the method further comprises the step of creation of a channel layer by deposit of a ternary alloy of AlGaN, or InGaN, or AlBN, or InBN, or InAlN;

- the method further comprises the step of creation of a channel layer by:

iv) deposit of an atomic monolayer of a third binary alloy;

5 v) deposit of an atomic monolayer of a fourth binary alloy;

repetition of steps iv) and v) if necessary until the required thickness is obtained;

- the step of creation of a channel layer further
10 comprises thermal treatment of atomic monolayers of third and fourth binary alloys deposited in iv) and v), the thermal treatment being carried out before some deposits of the fourth binary alloy:

- at a surface temperature between 0°C and 300°C above
15 to the temperature of creation of monolayers of third and fourth binary alloys;
- under vacuum or ultra-high vacuum between 10^{-8} Torr and 10^{-1} Torr ;
- under a gas mixture flow comprising ammoniac NH₃ or
20 nitrogen molecule N₂ or hydrogen molecule H₂ a pressure comprised between 10^{-8} Torr and the pressure of 1 kBar;

in presence of a NH₃, N₂ or H₂ plasma;

- the method further comprises the step of creation of a
25 buffer layer by deposit of a binary alloy of GaN, or AlN, or BN, or InN.

Presentation of the figures

Other characteristics and advantages of the invention will become clear after reading the following description which is given for purely illustrative and non-limitative purposes, and must be read with reference to the attached drawings among which:

- Figure 1 shows a sectional view of a semiconducting material based on a nitride of an III element on which an HEMT type transistor was made;
- 10 - Figure 2 is a sectional view of a semiconducting material based on a nitride of an III element;
- Figure 3 is a sectional view of an interface between a binary material and a ternary material of the semi-conducting material of the prior art;
- 15 - Figure 4 is a sectional view of a ternary material of the prior art;
- Figure 5a is a sectional view of a ternary material illustrating the alloy order in the [001] symmetric planes;
- 20 - Figure 5b is a sectional view of a ternary material of the prior art illustrating the alloy order in the [1-101] asymmetric planes;
- Figure 6a is a sectional view of binary and ternary material layers in the case of a ternary material
25 of the prior art;
- Figure 6b is a sectional view of binary and ternary material layers in the case of an ideal ternary material;

- Figure 6c is a sectional view of binary and ternary materials obtained using the method according to the invention;

- Figures 7a to 7g show sectional views of
5 different embodiments according to the invention;

- Figures 8a and 8b show sectional views of examples of pseudo-alloy ternary material obtained by the method according to the invention

- Figure 9 shows an example of semi-conducting
10 material according to the invention,

- Figure 10 shows an example of barrier layer according to the invention

- Figure 11 is a diagram illustrating the thickness of the barrier layer in function of the Al concentration
15 for different embodiments according to the present invention,

- Figures 12A to 12D illustrate the roughness of two embodiments of semi-conducting materials according to the present invention,

- Figures 12E to 12I illustrate different surface morphologies of AlGaIn/GaN HEMT structure according to the present invention for different Aluminium concentrations in the AlGaIn barrier (25nm thick),
20

- Figure 13 shows another example of semi-
25 conducting material according to the invention,

- Figure 14 shows two other embodiments according to the present invention.

Description of the invention

Therefore, one purpose of this invention is to provide a method capable of producing a semiconducting material based on an improved III-N, in other words a material that gives better properties of transistor structures made on it, in terms of charge density and reliability of the final transistor structure.

This is the purpose for which Applicant has studied some material parameters limiting these mobility, charge density and structure reliability properties.

These material parameters are roughness at interfaces, alloy fluctuations and alloy order.

Type 1 non-homogeneities: roughness at interfaces

The roughness at interfaces may be physical or chemical. The mobility of electrons in the GaN channel layer of a semiconducting material based on III-N is particularly sensitive to the chemical roughness.

The chemical roughness depends on the composition and occurs as soon as a ternary material (for example AlGa_N, InGa_N, InAl_N, AlBN, GaBN) is introduced into the structure.

Figure 3 shows an interface 9 between a GaN channel layer 7 and an Al_{0.3}Ga_{0.7}N barrier layer 8. The GaN channel layer 7 is located below the interface 9, and the Al_{0.3}Ga_{0.7}N barrier layer 8 is located above the interface 9.

It is seen that some atoms 11 of the GaN channel layer 7 located below the interface 9 are above said interface 9: therefore, there is a roughness phenomenon at the Al_{0.3}Ga_{0.7}N/GaN interface 9.

Type 2 non-homogeneities: alloy fluctuations

Figure 4 shows a non-homogenous distribution in a barrier layer of AlGaIn 30 of a III-N based semiconducting material.

5 "Gallium rich" areas 31 and "Aluminium rich" areas 32 are frequently created due to surface diffusion rates of Gallium and Aluminium precursors during the semiconducting material production method, because aggregates form and develop. This type of defect is qualified as an alloy
10 fluctuation.

Alloy fluctuations reduce the mobility of electrons and play an important role in the reliability of transistors made from the semiconducting material based on III-N.

15 In particular, these alloy fluctuations degrade the piezo-electric electron injection that becomes non-homogenous and causes a non-homogenous charge density in the channel of transistors produced on the semiconducting material.

20 Alloy fluctuations are a main source of failure of power transistors, since the current density in said transistors is not homogenous.

Type 3 non-homogeneities: the alloy order

25 The alloy order is a defect of the same type as the alloy fluctuation, but at atomic scale.

The alloy order is due to growth parameters and is the result of a partially ordered distribution of the constituent atomic elements of a ternary material.

For example, in the case of an AlGa_N barrier layer, "Aluminium rich" atomic planes can be observed alternating with "aluminium depleted" atomic planes.

The average composition of the alloy corresponds to
5 the target, with ordered fluctuations at atomic level.

The alloy order may appear in several crystalline directions. This alloy order may be induced by growth parameters and strain. In all cases, it is a "spontaneous" order that is not deliberately introduced into the
10 semiconducting material. Consequently, it is uncontrolled and non-homogenous.

Figure 5a shows the alloy order in the [1-101] asymmetric planes of an AlGa_N barrier layer, in other words in planes perpendicular to the [0001] growth axis.
15 "Aluminium rich" atomic planes 33 and "Aluminium depleted" atomic planes 34 can be seen.

The alloy order is formed in the [1-101] asymmetric planes when epitaxy production systems are used in which the supports are placed on a rotating plate. This is due to
20 the faster depletion of Aluminium and Gallium in the gas or molecular mix used in the method for manufacturing the semiconducting material (uncontrolled parasite reactions of precursors). Thus, the support will be exposed alternately to an "Aluminium rich" gas or molecular mix, then an
25 "Aluminium depleted" gas or molecular mix.

Figure 5b shows the alloy order in the [001] symmetric planes of an AlGa_N barrier layer. "Aluminium rich" atomic planes 35 and "Aluminium depleted" atomic planes 36 can be seen.

The alloy order in the [001] symmetry planes is due to non-homogenous strain distributions and differences in the stability of crystalline surfaces.

5 Effect of type 1, 2 and 3 non-homogeneities

Therefore, the three defect types mentioned above (roughness at interfaces, alloy fluctuations, alloy order) are related to the method used to make the semiconducting material and generate reliability problems for transistor
10 structures made on said semiconducting material.

As already demonstrated using the Ambacher et al. model, the charge density induced by polarisation is very dependent on the Aluminium concentration in the AlGaN barrier layer.

15 A local variation $\pm 0.2\%$ of the Aluminium concentration allows making the electronic density fluctuate by $2 \times 10^{12} \text{ cm}^{-2}$ or more.

As illustrated in Figure 6a, for the case of a classical AlGaN barrier layer 40, the direction and
20 intensity of the piezoelectric field 38 at the interface 39 between the barrier layer 40 and the channel layer 41 will locally depend on the distribution of Ga and Al atoms in the barrier layer 40, which will induce fluctuations in the electronic density at this interface 39.

25 Similarly, the power output by a transistor structure made on the semiconducting material comprising this standard AlGaN barrier layer will be distributed non-homogeneously.

As shown in Figure 6b, the average value of the
30 piezoelectric field 44 for an ideal barrier layer 42, is

equal to the local value of this field at any point on the interface 43 between the barrier layer 42 and the channel layer 45. Therefore, the electronic density is homogenous at the interface 43.

5 Applicant has thus demonstrated the importance of having a semiconducting material that includes a correctly ordered barrier layer in order to limit the three types of non-homogeneities mentioned above, and thus obtain better properties of transistor structures made on the
10 semiconducting material.

 In order to obtain a semiconducting material with a correctly ordered barrier layer, Applicant decided to replace the barrier layer made of a ternary alloy within III-N-based semiconducting materials according to prior
15 art, by a barrier layer made of a ternary pseudo-alloy.

 For the purposes of this invention, a ternary "pseudo-alloy" is an alloy composed of alternations of atomic monolayers of binary alloys.

 It will be understood, in the present invention, that
20 a "monolayer" of binary alloy is composed of one monatomic plane of III element (i.e. Ga, Al, In) and one monatomic plane of nitrogen (N). It will also be understood in the present invention that one "monatomic plane" corresponds to one step of atoms, which also corresponds to a half lattice
25 cell of the crystalline structure.

 Figure 7a illustrates a semiconducting material 50 according to a first embodiment of the invention.

 This semiconducting material 50 comprises a channel layer 51 on a support 52, and a barrier layer 53 made of a
30 ternary pseudo-alloy on the channel layer 51.

The support 52 is made of SiC. However, this support could be made of other materials such as Silicon, AlN, sapphire or GaN.

The channel layer 51 is a binary alloy of GaN.
5 However, another material could have been chosen for the channel layer 51 such as AlN, BN (boron nitride) or InN (Indium nitride).

This channel layer 51 is deposited on the support by a method known to those skilled in the art such as Molecular
10 Beam Epitaxy (MBE) or Metal-Organic Chemical Vapour Deposition (MOVD) method.

The barrier layer 53 is a ternary pseudo-alloy of AlGaN. This barrier layer 53 comprises binary alloy layers of GaN 54 and binary alloy layers of AlN 55. These GaN and
15 AlN layers are alternated and have constant thickness.

Each layer of first binary alloy made of GaN 54 (or each layer of second binary alloy made of AlN 55) is composed of one or several atomic monolayers of GaN (or AlN).

20 Those atomic monolayers of GaN and AlN are individually fitted in the semi-conducting material in order to obtain a barrier layer as homogeneous as possible.

Figure 12A to 12D illustrates the roughness of the semi-conducting materials according to the present
25 invention for different concentrations of Ga and Al in the barrier layer.

The number of atomic monolayers (denoted n_{GaN}) per layer of the first binary alloy made of GaN 54 can vary between 1 and 40, and preferably between 1 and 20, and even
30 more preferably between 2 and 10. Similarly, the number of

atomic monolayers (denoted n_{MLN}) per layer of the second binary alloy made of AlN 55 can vary between 1 and 40, and preferably between 1 and 20, and even more preferably between 2 and 10.

5 It shall be appreciated that existing processes such as the one disclosed by US6100542 indeed involve making layers with an alternation of very thin elementary layers - and in this respect these processes present some similarities with the alternation of monolayers mentioned
10 above. However, US6100542 addresses materials based on arsenides and not nitrides, and its alternation aims at maximizing the doping of the larger layer thus constituted with the elementary layers. US6100542 does not address the issue of homogeneity of the distribution of electrons.
15 Indeed, US6100542 concerns non piezoelectric structure. Man skilled in the art knows that alloy disorders in the layers of a non piezoelectric arsenide structure do not interfere with the homogeneity of the distribution of electrons. Hence, materials based on arsenide which comprise an
20 alternation of elementary layers do not address the issue of homogeneity of the distribution of electrons.

It shall also be appreciated that existing processes such as the one disclosed in WO02/093650 indeed involve making layers with an alternation of "monolayers" as
25 mentioned at page 7 third paragraph of WO02/093650.

However, the "monolayers" described in WO02/093650 are far from the definition of monolayer in the sense of the present invention. Indeed, the "monolayers" as described in WO02/093650 are in the range of 5 to 20 angstrom thick (see
30 WO02/093650 page 7 third paragraph), which is very thick

with respect to the monolayers of the present invention which are atomic monolayers.

WO02/093650 addresses the problem of increasing the electron mobility within the structure.

5 However, WO02/093650 does not address the issue of increasing the homogeneity of the electron distribution (particularly in the channel layer). Indeed WO02/093650 does not suggest monolayers as defined in the present invention (the "monolayer" as defined in WO02/093650 being
10 very thicker as the one of the present invention).

 Coming back to the invention, the production method known to those skilled in the art such as liquid phase epitaxy, or vapour phase epitaxy or molecular beam epitaxy is used to grow the barrier layer 53 on the channel layer
15 of GaN.

 The barrier layer 53 is created starting by depositing a layer of the first binary alloy of GaN 54 in which the number of atomic monolayers n_{GaN} is between 1 and 40, preferably between 1 and 20 and even more preferably
20 between 2 and 10, and the next step is to deposit a layer of the second binary alloy of AlN in which the number of atomic monolayers n_{AlN} is between 1 and 40, preferably between 1 and 20 and even more preferably between 2 and 10.

 The next step is to deposit layers of the first binary
25 alloy of GaN and layers of the second binary alloy of AlN until the required thickness of the barrier layer 53 is obtained, varying between 2 and 500 nm.

 In the embodiment shown in Figure 7a, the numbers of atomic monolayers n_{GaN} and n_{AlN} are equal. However, the

numbers of atomic monolayers n_{GaN} and n_{AlN} could be different.

Since the barrier layer 53 is composed of alternations of layers of GaN and AlN, the gas or molecular precursors of Gallium and of Aluminium (or Gallium and Aluminium) are not mixed during the production method and there is no mix depletion phenomenon.

Thus, alloy fluctuations are limited:

- at the nanometric and micrometric scales (type 1 non-homogeneities), and
- at the atomic scale (type 2 and 3 non-homogeneities).

Therefore the structure of the barrier layer 53 is perfectly ordered along the [0001] growth axis.

As illustrated in Figure 6c, this has the effect of:

- limiting the chemical roughness and consequently limiting the diffusion of electrons at the interface between the channel layer 91 and the barrier layer 92 (this barrier layer being composed of an alternation of AlN layers 93 and GaN layers 94),
- optimising the distribution of the piezoelectric field for which the average value is equal to the local value of the piezoelectric field 95 at all points on the interface 90.

Therefore, the injection of electrons by this field is optimised. Moreover, the distribution of electrons injected into the two-dimensional gas (2 DEG) is homogenous since the induced piezoelectric field is homogenous.

Consequently, this structure provides a means of optimising the mobility and the surface density of electrons located in the two-dimensional gas (2 DEG).

Figure 8a illustrates an example embodiment of a barrier layer according to this invention. In this example, a 20.5 nm thick barrier layer of AlGa_N containing 32.2% of aluminium was replaced by a barrier layer made of a ternary pseudo-alloy:

$$(\text{AlN } n_{\text{AlN}} = 2 / \text{GaN } n_{\text{GaN}} = 4)_{x=7}$$

10 where:

- n_{AlN} is the number of atomic monolayers of AlN,
- the thickness of an AlN monolayer is $e_{\text{AlN}} = 0.2485 \text{ nm}$,
- n_{GaN} is the number of atomic monolayers of GaN,
- 15 - the thickness of an GaN monolayer is $e_{\text{GaN}} = 0.2590 \text{ nm}$,
- X is the number of periods ($\text{AlN } n_{\text{AlN}} = 2 / \text{GaN } n_{\text{GaN}} = 4$),
- Y is the average composition of the barrier:
- 20 $Y = n_{\text{AlN}} / (n_{\text{GaN}} + n_{\text{AlN}}) = 32.2\%$,
- E is the equivalent thickness of the barrier:
- $E = X \times (n_{\text{AlN}} \times e_{\text{AlN}} + n_{\text{GaN}} \times e_{\text{GaN}}) = 20.1 \text{ nm}$.

Figure 8b illustrates another example embodiment of a barrier layer according to this invention. In this example, a barrier layer of AlGa_N containing 50.0% of aluminium was replaced by a barrier layer made of a ternary pseudo-alloy:

$$(\text{AlN } n_{\text{AlN}} = 1 / \text{GaN } n_{\text{GaN}} = 1)_{x=3}$$

Figure 7b illustrates a semiconducting material made according to a second embodiment of this invention.

In this second embodiment, a buffer layer 56 has been inserted between the channel layer 51 and the support 52.

The buffer layer 56 is a material chosen from among GaN and AlGaN. This buffer layer facilitates growth of the GaN channel layer. This buffer layer is deposited by bonding or by another known method to those skilled in the art such as an epitaxy method.

In the embodiment illustrated in figure 7c, the barrier layer 53 comprises GaN layers 54', 54'', 54''' without the same number of atomic monolayers n_{GaN} .

Layers 54', 54'', 54''' comprise eight, five and two atomic monolayers of GaN, respectively. These layers alternate with AlN layers 55' and 55'', the layer 55' being furthest from the support, and the layer 54''' being closest to the support.

In the illustration in Figure 7c, the number of atomic monolayers n_{GaN} per layer of GaN 54', 54'', 54''' decreases as the distance from the support 52 increases. However, it would be possible to have a barrier layer 53 in which the number of atomic monolayers increases as the distance from the support 52 increases.

Thus, the number of atomic monolayers n_{GaN} per GaN layer can vary along the barrier layer 53.

The same is true for the number of monolayers n_{AlN} per AlN layer that can also vary along the barrier layer 53.

In the barrier layer, the number of monolayers of GaN and AlN can vary independently as shown in figure 7c where the number of atomic monolayers n_{GaN} per layer of GaN 54', 54'', 54''' vary whereas the number of atomic monolayers n_{AlN} per layer of AlN 55' and 55'' do not vary.

The numbers of monolayers n_{GaN} and n_{AlN} can also vary simultaneously along the barrier layer. For example, the number of atomic monolayers n_{AlN} can vary so that it decreases (or increases) as the distance from the support increases, and the number of atomic monolayers n_{GaN} can vary so that it increases (or decreases) as the distance from the support increases.

Consequently, the number of atomic monolayers of each layer of binary alloy may vary between a first value on a back face of the barrier layer and a second value on a front face of the barrier layer, the back face being closer to the support than the front face.

Figure 7d illustrates a semiconducting material according to a fourth embodiment. This semiconducting material includes a support 52, a buffer layer 56, a channel layer 51 and a barrier layer 53.

In this embodiment, the buffer layer 56 is a ternary pseudo-alloy of AlGaN composed of alternating layers of binary alloy of GaN 57 and binary alloy of AlN 58.

The buffer layer 56 has the same characteristics as the ternary pseudo-alloy barrier layer (n_{GaN} and n_{AlN} between 1 and 40, preferably between 1 and 20, and even more preferably between 2 and 10 and possibly varying along the buffer layer, etc.).

In this embodiment, the buffer layer 56 comprises two GaN layers 57 alternating with two AlN layers 58.

Furthermore, the number of atomic monolayers n_{GaN} per GaN layer 57 varies along the buffer layer 56. The GaN layer 57 closest to the support comprises two atomic

monolayers while the GaN layer furthest from the support comprises four atomic monolayers.

The number of atomic monolayers n_{AlN} per AlN layer 58 can also vary along the buffer layer 56. The GaN layer 57 closest to the support comprises 6 atomic monolayers while the AlN layer furthest from the support comprises three atomic monolayers.

Thus, in the embodiment illustrated in Figure 7d, the numbers of atomic monolayers per layer of GaN and AlN vary along the buffer layer, the number of atomic monolayers n_{AlN} varying so that it decreases as the distance from the support increases, and the number of atomic monolayers n_{GaN} varies so that it increases as the distance from the support increases.

The reader will have understood that the numbers of atomic monolayers n_{AlN} and n_{GaN} may be fixed along the buffer layer as was the case for the barrier layer illustrated in Figure 7a.

This buffer layer can be obtained by a production method known to those skilled in the art such as an epitaxy method (molecular beam epitaxy, liquid phase epitaxy, vapour phase epitaxy).

In summary, the barrier layer (53) made of an AlGaIn ternary pseudo alloy may be denoted:

$$(AlNn_{\text{AlN}}/GaNn_{\text{GaN}})x$$

where:

- n_{AlN} is a number of atomic monolayers of an AlN layer where $1 \leq n_{\text{AlN}} \leq 40$, preferably $1 \leq n_{\text{AlN}} \leq 20$, more

preferably $2 \leq n_{\text{AlN}} \leq 10$) and where n_{AlN} can vary along the barrier layer.

- n_{GaN} is a number of atomic monolayers of a GaN layer where $1 \leq n_{\text{GaN}} \leq 40$, preferably $1 \leq n_{\text{GaN}} \leq 20$, more preferably $2 \leq n_{\text{GaN}} \leq 10$) and where n_{GaN} can vary along the barrier layer.

- X is the number of layers of GaN and AlN.

In order to further improve the electronic properties of the semiconducting materials based on III-N, the barrier layer may include one or several layers of ternary alloy in addition to the alternation of layers of binary alloys at the atomic scale.

Applicant has pointed out that the presence of a layer of ternary alloy in the barrier layer comprising the alternation of layers of binary alloys was able to improve the homogeneity of the piezoelectric field and to increase the mobility of charge carriers of the semi-conducting materials.

The creation of barrier layer 53 may include the same steps as described above.

It is thus possible to start by creating an initial barrier layer by deposit of a layer of a first binary alloy of GaN 54, deposit of a layer of a second binary alloy of AlN 55, and repetition of these deposits steps of layers of GaN and AlN until the required thickness is obtained for the barrier layer 53.

Furthermore, a step of creation of one or several layers of ternary alloy on or on the initial barrier layer is made.

The step of creation of layer(s) of ternary alloy varies according to the embodiment of the semi-conducting substrate.

In one embodiment illustrated in figure 7e, the
5 barrier layer 53 comprises a layer of ternary alloy 80 of AlGa_N and an alternation (at the atomic scale) of layers of a first binary alloy 54 of Ga_N and of a second binary alloy 55 of Al_N.

It will be understood that the atomic scale is the
10 scale of the angstrom.

Each layer of binary alloy of Ga_N (or Al_N) of the alternation comprises between 1 and 40 atomic monolayers of Ga_N (or Al_N), preferably between 1 and 20, and even more preferably between 2 and 10. In all cases, each layer of
15 binary alloy of Ga_N (or Al_N) of the alternation comprises at least one atomic monolayer of this binary alloy of Ga_N (or Al_N).

The alternation of layers of binary alloys 54, 55 of Ga_N and Al_N is located between the layer of the ternary alloy 80 of AlGa_N and the support 52. In other words, the
20 layer of the ternary alloy 80 of AlGa_N is on top of the alternation of layers of binary alloys of Ga_N and Al_N.

The presence of the layer of ternary alloy 80 on top of the alternation of layers of binary alloys 54, 55 of Ga_N and Al_N allows immediate compatibility with the technical
25 methods optimized for semi-conducting materials comprising a barrier layer made of a layer of ternary alloy of AlGa_N, especially regarding the making of ohmic contacts, while keeping the benefit of the optimal electronic injection
30 obtained thanks to the alternation at the atomic scale of

binary alloys 54, 55 of GaN and AlN in the barrier layer 53.

Indeed, the applicant has pointed out that the importance of having an ordered alloy in the barrier layer 53 decreases as the distance from the interface between the barrier layer and the channel layer 51 increases. In other words, a semi-conducting material having an alloy disorder in a layer located far from the interface between the channel layer 51 and the barrier layer 53 has a better mobility of the charge carriers and a piezoelectric polarization field more homogeneous than a semi-conducting material having an alloy disorder in a layer located closed to the interface between the channel layer 51 and the barrier layer 53

The step of creation of the layer of ternary alloy 80 of AlGa_N, allowing the semi-conducting material shown in figure 7e to be obtained, comprises the deposit of a classical layer of ternary alloy created by epitaxy.

It will be understood, in the present invention, that a "classical layer of ternary alloy" is a layer of ternary alloy created by epitaxy by making interact in a low residual pressure room (ultra-high vacuum, residual pressure comprised between 10^{-9} Torr and 10^{-14} Torr) atomic or molecular flows (obtained by evaporation of solid sources or by direct injection of gas precursors of GaN and AlN) on the substrate heated to an appropriate temperature for the epitaxial growth.

In another embodiment shown in figure 7f, the barrier layer 53 comprises a plurality of layers of ternary alloy 70 of AlGa_N. Those layers of ternary alloy 70 of AlGa_N are

located in the alternation of layers of binary alloys 54, 55 of GaN and AlN.

The layers of ternary alloy 70 of AlGa_N interbedded in the alternation of layers of binary alloys 54, 55 of GaN and AlN are obtained by interdiffusion of the III elements
5 of the layers of binary alloys 54, 55 of GaN and AlN.

Figure 10 is a sectional view, at the atomic scale, of the barrier layer from the embodiment illustrated in figure 7f. Each layer of binary alloy of GaN (or AlN) comprises
10 two atomic monolayers. Each layer of ternary alloy of AlGa_N comprises one atomic monolayer of ternary alloy.

The presence of layers of ternary alloy 70 between the layers of binary alloys 54, 55 allows avoiding the violent variations of composition in the barrier layer 53. This
15 improves the homogeneity of the local piezoelectric polarisation field. This homogenisation of the polarisation field allows decreasing the charge density fluctuations at the interface between the channel layer 51 and the barrier layer 53.

20 The creation of the plurality of layers of ternary alloy 70 illustrated in figure 7f comprises a thermal treatment after having created at least one alternation of layers of binary alloys 54, 55 of GaN and AlN deposited for the creation of the barrier layer 53.

25 The thermal treatment can be realised at the end of the step of creation of the barrier layer 53 (that is to say after the successive deposit steps of the layers of the first binary alloy 54 of GaN and the second binary alloy of AlN).

This treatment can also be realized during the steps of creating the barrier layer. In that case, the thermal treatment is carried out before some deposit steps of the second binary alloy.

5 For example, one can begin to deposit the first binary alloy (GaN). Then, one can deposit the second binary alloy (AlN). Then, one can carry out the thermal treatment which allows better inter-diffusion of the III elements of the layers of binary alloys 54, 55 of GaN and AlN. The
10 diffusion, very local, can take place on a typical distance of 1 to 5 material monolayers.

The thermal treatment is carried out after at least some binary alloy deposits. Typical conditions for this treatment are:

- 15 - at a surface temperature between 0°C and 300°C above to the temperature of creation of monolayers of first and second binary alloys;
- under vacuum or ultra-high vacuum between 10^{-8} Torr and 10^{-1} Torr ;
- 20 - under a gas mixture flow comprising ammoniac NH₃ or nitrogen molecule N₂ or hydrogen molecule H₂ a pressure comprised between 10^{-8} Torr and the pressure of 1 kBar;
- in presence of a NH₃, N₂ or H₂ plasma.

A layer of ternary alloy 70 of AlGa_{0.5}N is then obtained,
25 located between the layers of the first and second binary alloys of GaN and AlN. This layer of ternary alloy comprises between 1 and 5 monolayers of ternary alloy.

If the barrier layer thickness does not correspond to the required thickness, a deposit of a layer of GaN is made
30 and a deposit of a layer of AlN is made. Then, the thermal

treatment is carried out, and so on until the thickness corresponds to the required thickness.

The reader will appreciate that it can be chosen not to carry out the thermal treatment systematically after
5 each deposit of a layer of the second binary alloy.

For example, the thermal treatment can be made once on two times. That is to say the thermal treatment is carried out after two deposits of a layer of a binary alloy have been made.

10 The thermal treatment may also be carried out only once at the end of the creation step of the initial barrier layer, that is to say once the required barrier layer thickness is obtained.

Moreover, before carrying out the thermal treatment,
15 it is possible to deposit an additional layer of AlN or SiN in order to stabilize the surface of the barrier layer 53 during the thermal treatment.

In figure 7g, a semi-conducting material according to another embodiment of the present invention is shown. In
20 this embodiment, the semi-conducting material comprises the same elements as the embodiment illustrated in figure 7. Those same elements are the alternation of layer of binary alloys 54, 55 of GaN and AlN, and the plurality of layers of the ternary alloy 70 located in the alternation.

25 Moreover, the embodiment illustrated in figure 7g comprises a classical layer of ternary alloy on top of the alternation. This allows gathering the advantages of the embodiments illustrated in figures 7e and 7f.

The man skilled in the art will appreciate that it is
30 possible to realize a semi-conducting material comprising a

channel layer or a buffer layer comprising the same elements (layers alternation of binary alloys, etc.) than those described for the barrier layer. Having a channel layer or a buffer layer made of ternary pseudo-alloy allows
5 increasing the homogeneity of the distribution of the electrons in the semi-conducting material.

Figure 9 shows an example of semi-conducting material realization according to the present invention. In this example, the semi-conductor comprises:

- 10 - a Si (silicon) substrate 52,
- a buffer layer 56 made of a $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}$ alloy,
- a channel layer 51 made of a $\text{In}_{0.25}\text{Ga}_{0.75}\text{N}$ ternary pseudo-alloy of a thickness of 155 Angstroms,
- an alternation of layer of binary alloys 54, 55
15 made of ternary pseudo-alloy $\text{Al}_{0.32}\text{Ga}_{0.68}\text{N}$ of a thickness of 184 Angstroms,
- a layer of a classical ternary alloy 80 of $\text{Al}_{0.4}\text{Ga}_{0.6}\text{N}$ of a thickness of 50 Angstroms,
- a layer of binary alloy 190 of GaN of a thickness
20 of 20 Angstroms,
- a layer of binary alloy 100 of AlN of a thickness of 30 Angstroms.

In the different embodiments illustrated in figures 7a to 7g, the channel layer is made of binary alloy of GaN. In
25 other embodiments, the channel layer is a ternary pseudo-alloy of AlGa_xN, or InGa_xN, or Al_xBN, or In_xBN, or InAlN.

In these other embodiments, the channel layer is created using a similar method to the one described for the creation of the barrier layer, and the binary alloys for

making the ternary pseudo-alloy are chosen from among AlN, GaN, BN, and InN.

When the channel layer is made of a ternary pseudo-alloy, it comprises the same features as the ternary
5 pseudo-alloy barrier layer (number of atomic monolayers per layer of binary alloy comprised between 1 and 40, preferably between 1 and 20, and more preferably between 2 and 10, this number being able to vary along the thickness of the channel layer). By having a channel layer made of
10 ternary pseudo-alloy, the homogeneity of the semi-conducting material (and particularly the distribution of electrons) is increased.

The surface morphology of AlGaN/GaN HEMT structure is generally affected by Al concentration in the barrier.

15 The semi-conducting material according to the invention allows increasing the aluminium concentration in the barrier layer (or channel layer, or buffer layer) as illustrated in figure 11.

Indeed, by decreasing the roughness at the interface
20 between the channel layer and the barrier layer, it is possible to increase the concentration of Al in the layer.

In fact, the perturbations (homogeneity of the electronic density ...) in a layer are principally due to the Al atoms. Hence, for a given roughness, it is possible with
25 the present invention to increase the concentration of aluminium.

OK data points of figure 11 correspond to structures according to the present invention which are grown on Si
30 111 substrates for different thicknesses and Aluminium concentrations measured by XRD.

As shown in figure 11, thick barrier layers are achievable (up to 41nm for 23% Aluminium), but most results correspond to thin barrier layers.

Typical thicknesses ranging between 20nm and 27nm have
5 shown best results after device fabrications.

Below 25 nm, Aluminium concentration in the 28%-30% range is a standard specification leading to optimised ohmic contacts.

For higher Al concentrations (32% and more), barrier
10 thickness must be decreased down to 15-20nm.

Cross Hatch data points of figure 11 correspond to cross-hatched structures according to the present invention for different thicknesses and Aluminium concentrations measured by XRD.

15 In this case, relaxation of the AlGa_N barrier occurs, leading to micro-cracks on the surface.

This strain effect appears when Aluminium concentration is too high in regards with barrier thickness.

The trend is given by curve 500. Applicant recommends
20 specifying barrier layers thickness/Al% below this curve 500.

PSP data points correspond to pseudomorphic structures according to the present invention with strained Ga_N channel on Al_{0.1}Ga_{0.9}N buffer layer.

25 As shown in figure 11, it is possible, with such pseudomorphic structures, to reach concentrations of 40% in Aluminium even for thick barriers (26nm).

Figures 12E to 12I illustrate the surface morphology of different structures according to the present invention
30 with various Aluminium concentrations in the AlGa_N barrier.

Figure 12E shows a structure according to the present invention having an Aluminium concentration of 20% in the AlGa_N barrier of a thickness equal to 25nm.

Figure 12F shows a structure according to the present invention having an Aluminium concentration of 25% in the AlGa_N barrier of a thickness equal to 25nm.

Figure 12G shows a structure according to the present invention having an Aluminium concentration of 32% in the AlGa_N barrier of a thickness equal to 25nm.

Figure 12H shows a structure according to the present invention having an Aluminium concentration of 40% in the AlGa_N barrier of a thickness equal to 25nm.

Figure 12I shows a structure according to the present invention having an Aluminium concentration of 39% in the AlGa_N barrier of a thickness equal to 26nm.

As is shown on figures 12E to 12I, no differences are observed on the surface morphology for every layers.

In the different embodiments illustrated in figures 7a to 7g, the barrier layer is a ternary pseudo-alloy of AlGa_N. In other embodiments, the barrier layer is a ternary pseudo-alloy of InGa_N (indium gallium nitride), or AlBN (aluminium boron nitride), or InBN (indium boron nitride, or InAlN (indium aluminium nitride). In these other embodiments, the first and second binary alloys making the ternary pseudo-alloy are chosen from among AlN, GaN, BN, and InN.

Figure 13 shows another embodiment according to the present invention.

This other embodiment comprises:

- a substrate 600 having a thickness of 500 nm,

- an AlGa_N template layer 610 having a thickness of 1500 nm which comprises 10% of Aluminium in concentration,
- a GaN channel layer 620 having a thickness of 15 nm,
- a barrier layer 630 having a thickness of 11 nm which
5 comprises 50% of Aluminium in concentration,
- an AlGa_N Schottky layer 640 having a thickness of 4 nm which comprises 25% of Aluminium in concentration, and
- a GaN cap layer 650 having a thickness of 2 nm.

The barrier layer of the semi-conducting material
10 illustrated in figure 13 comprises alternations of one monolayer of AlN (one monatomic plane of Al and one monatomic plane of N) and one monolayer of GaN (one monatomic plane of Ga and one monatomic plane of N).

The present invention presents some advantages thank
15 to the use of monolayers, which allows obtaining ordered ternary pseudo-alloy, as AlGa_N layer having a concentration of 50% of Aluminium (Al - N - Ga - N).

Figure 14 shows some advantages of the present
invention compared to the process and device described in
20 W002/093650.

In figure 14:

- A represents an AlN lattice cell (Al - N - $\tilde{\text{Al}}$ - N),
- B represents a GaN lattice cell (Ga - N - Ga - N),
- C represents an AlGa_N lattice cell (Al - N - Ga - N).

25 As can be observed with the alternation C - A - C - B... according to the present invention and illustrated on the top of figure 14, the present invention allows smoothing of the forbidden band diagram 730:

- the energy diagram is smoothed (E_g is the energie of the forbidden band of the alloys: $E_g(\text{GaN})=3.4\text{eV}$, $E_g(\text{AlN}) = 6.2 \text{ eV}$, $E_g(\text{AlGaN } 50\%) = 4.8\text{eV}$,
- the strain, in the structure presents a better
5 distribution which allows to obtain more reliable transistor structures.

On the contrary, the process and device described in WO02/093650 does not allow smoothing of the forbidden band diagram 730.

10 Indeed, the process described in WO02/093650 does not allow obtaining an AlGa_xN lattice cell C (Al - N - Ga - N) (since the "monolayers" as defined in WO02/093650 are thick). Hence, the process described in WO02/093650 only allows obtaining alternations A - B - A - B... as illustrated
15 on top of figure 14.

Embodiment 710 and 720 are two examples of semi-conducting material according to the present invention which comprise C layers.

Although some examples of embodiments of the present
20 invention were described in detail above, those skilled in the art will easily understand that many modifications could be made without physically going outside the scope of the new information and the advantages described herein. Consequently, all modifications of this type will be
25 included in the scope of this invention as defined in the attached claims.

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CLAIMS

1. Semi-conducting substrate (60) based on elements in columns III and V in the periodic table, to be used for example for manufacturing of HEMT of HEMT type transistor structures, comprising a support (52), a channel layer (51) on the support and a barrier layer (53) on the channel layer, wherein the barrier layer (53) is composed of an alternation, at the atomic scale, of layers of first and second III-V binary semi-conducting alloys (54, 55) and of layers of III-V semi-conducting ternary alloy; each layer of III-V semi-conducting ternary alloy being located between a layer of the first binary alloy and a layer of the second binary alloy of the alternation.
2. Semi-conducting substrate according to claim 1, wherein the channel layer comprises an alternation, at the atomic scale, of layers of third and fourth III-V binary semi-conducting alloys.
3. Semi-conducting substrate according to claim 1 or 2, wherein the semi-conducting substrate (60) further includes a buffer layer (56) between the support (52) and the channel layer (51), the buffer layer (56) comprising an alternation, at the atomic scale, of layers of fifth and sixth III-V binary semi-conducting alloys.
4. Semi-conducting substrate according to claim 1, 2 or 3, wherein the number of atomic monolayers in each binary alloy of the alternation of the barrier layer or of the

channel layer or of the buffer layer is comprised between 1 and 20.

5. Semi-conducting substrate according to claim 1 or 2 or 3, wherein the number of atomic monolayers in each binary alloy of the alternation of the barrier layer or of the channel layer or of the buffer layer varies between a first value on a back face of the barrier layer or of the channel layer or of the buffer layer, and a second value on a front face of the barrier layer or of the channel layer or of the buffer layer, the back face being closer to the support (52) than the front face.
6. Semi-conducting substrate according to claim 5, wherein the first and second values are comprised between 1 and 20.
7. Semi-conducting substrate according to one of the preceding claims, wherein the first, second, third, fourth, fifth and sixth binary alloys are chosen from among AlN, GaN, BN, and InN.
8. Semi-conducting substrate according to claim 1, wherein the alternation, at the atomic scale, of layers of first and second III-V semi-conducting binary alloys is located between the support and said layer of III-V semi-conducting ternary alloy.
9. Semi-conducting substrate according to claim 1, wherein the barrier layer further includes a layer of the III-V semi-conducting ternary alloy on the alternation, at the atomic scale, of layers of first and second III-V semi-conducting binary alloys.

10. Semi-conducting substrate according to claim 2, wherein the channel layer further comprises a plurality of layers of III-V semi-conducting ternary alloy, each layer of III-V semi-conducting ternary alloy being located between a layer of the third binary alloy and a layer of the fourth binary alloy of the alternation.
11. Semi-conducting substrate according to one of claims 8 to 10, wherein the number of atomic monolayers in each layer of the ternary alloy located between two layers of the binary alloys is comprised between 1 and 5.
12. Semi-conducting substrate according to claim 1 or 3, wherein the channel layer is made of a layer of ternary alloy of AlGa_N, or InGa_N, or AlBN, or InBN, or InAlN.
13. Semi-conducting substrate according to claim 1 or 3, wherein the channel layer is made of a layer of binary alloy of Ga_N, or Al_N, or BN, or In_N.
14. Semi-conducting substrate according to claim 1 or 2, wherein the semi-conducting substrate (60) further comprises a buffer layer (56) between the support (52) and the channel layer (51), the buffer layer being made of a layer of binary alloy of Ga_N, or Al_N, or BN, or In_N.
15. Semi-conducting substrate according to claim 1 or 2, wherein the semi-conducting substrate (60) further comprises a buffer layer (56) between the support (52) and the channel layer (51), the buffer layer being made of a layer of ternary alloy of AlGa_N, or InGa_N, or AlBN, or InBN, or InAlN.

16. Semi-conducting substrate according to one of the preceding claims, wherein the support (52) is made of a material chosen from among Si, SiC, AlN, Sapphire, and GaN.

17. Semi-conducting substrate according to one of the preceding claims, wherein the thickness of the barrier layer (53) is comprised between 2nm and 500 nm.

18. Method for preparation of a semi-conducting substrate {60} comprising a support (52), a channel layer (51) on the support and a barrier layer (53) on the channel layer,

wherein the methods comprises the following step (no order being imposed) :

b. creation of an initial barrier layer by:

vi) deposit of at least one atomic monolayer of a first binary alloy;

vii) deposit of at least one atomic monolayer of a second binary alloy;

viii) repetition of steps vi) and vii) if necessary until the required thickness is obtained;

c. creation of at least one layer of ternary alloy in or on the initial barrier layer by;

ix) thermal treatment of atomic monolayers of first and second binary alloys deposited in vi) and vii)

19. Method according to claim 18, wherein the thermal treatment is carried out after at least some deposits of the second binary alloy: - at a surface temperature between 0°C and 300°C above to the temperature of creation of monolayers of first and second binary alloys; under vacuum, or ultra-high vacuum, between 10⁻⁸ Torr and 10⁻¹ Torr ; - under a gas mixture flow comprising ammoniac NH₃ or nitrogen molecule N₂ or hydrogen molecule H₂ a pressure comprised between 10⁻⁸ Torr and the pressure of 1 kBar; in presence of a NH₃, N₂ or H₂ plasma.
20. Method according to claim 18 or 19 , wherein the thermal treatment of atomic monolayers of first and second binary alloys deposited in i) and ii) is made after the step of creation of the initial barrier layer.
21. Method according to one of claims 18 to 20 , wherein the method further comprises the step of creation of a channel layer by deposit of a binary alloy of GaN, or AlN, or BN, or InN.
22. Method according to one of claims 18 to 20, wherein the method further comprises the step of creation of a channel layer by deposit of a ternary alloy of AlGa_xN_{1-x}, or InGa_xN_{1-x}, or AlBN, or InBN, or InAlN.
23. Method according to one of claims 18 to 20, wherein the method further comprises the step of creation of a

channel layer by: ix) deposit of an atomic monolayer of a third binary alloy; x) deposit of an atomic monolayer of a fourth binary alloy; xi) repetition of steps iv) and v) if necessary until the required thickness is obtained.

24. Method according to claim 23, wherein the step of creation of a channel layer further comprises thermal treatment of atomic monolayers of third and fourth binary alloys deposited in iv) and v) , the thermal treatment being carried out before some deposits of the fourth binary alloy: - at a surface temperature between 0°C and 300°C above to the temperature of creation of monolayers of third and fourth binary alloys; under vacuum or ultra-high vacuum between 10⁻⁸ Torr and 10⁻¹ Torr ; - under a gas mixture flow comprising ammoniac NH₃ or nitrogen molecule N₂ or hydrogen molecule H₂ a pressure comprised between 10⁻⁸ Torr and the pressure of 1 kBar; in presence of a NH₃, N₂ or H₂ plasma. 30. Method according to one of claims 20 to 29, wherein the method further comprises the step of creation of a buffer layer by deposit of a binary alloy of GaN, or AlN, or BH, or InN.