FORMATION OF METAL SILICIDE LAYER OVER COPPER INTERCONNECT FOR RELIABILITY ENHANCEMENT

Background of Invention

1) Field of the Invention

The present invention relates to copper (Cu) and/or Cu alloy metallization in semiconductor devices. The present invention is applicable to manufacturing high speed integrated circuits having submicron design features and high conductivity interconnect structures.

2) Description of the Prior Art

Typically, Cu interconnects are fabricated using damascene processing methods. In these structures, the top surface of the Cu damascene line is capped with a thin dielectric layer, e.g. Si_3N_4, SiC, etc, while the bottom surface and two sidewalls are sealed with a metal liner, e.g. TiN, Ta, TaN, etc. Although the fast diffusion paths in Cu interconnect can vary depending on the fabrication process and materials used, all investigators have reported that the electromigration lifetime of Cu transport at interfaces, especially the Cu/dielectric interface. Even though, this interface allows fast diffusion,

interjecting a thin conducting layer on the surface of Cu line shows to reduce Cu interface mass transport and enhances Cu electromigration (EM) lifetime.

The importance of overcoming the various deficiencies noted above is evidenced by the extensive technological development directed to the subject, as documented by the relevant patent and technical literature. The closest and apparently more relevant technical developments in the patent literature can be gleaned by considering the following.

US6777811: - Harada - Semiconductor device and its fabrication method - Semiconductor device has copper silicide layer formed selectively on copper wiring above which titanium nitride film is deposited inside a hole formed in silicon oxide and silicon nitride films.

US6181013- Liu, Chung-Shi - Method for selective growth of Cu3Ge or Cu5Si for passivation of damascene copper structures and device manufactured thereby- Thin film electronic device for use in ultra large scale integrated applications includes a passivation layer overlying an exposed surface of a damascene copper conductor.

US5893752: - Inventor: Zhang, Jiming; Austin, TX - Process for forming a semiconductor device - Manufacture of a semiconductor device with metal interconnects

United States Patent 6,660,634 Ngo, et al. December 9, 2003 - Method of forming reliable capped copper interconnects.

United States Patent 5,447,887 Filipiak , et al. September 5, 1995 - Method for capping copper in semiconductor devices.

United States Patent 6,674,167 Ahn, et al. January 6, 2004 - Multilevel copper interconnect with double passivation – forms a silicide layer around the cu interconnects.

United States Patent 5,510,295 Cabral, Jr. , et al. shows a process to make metal silicide.

Summary of the Invention

The embodiments of the present invention provides a structure and a method of manufacturing a copper interconnect with an overlying sputtered metal silicide which is characterized as follows.

An example embodiment comprises:

forming a dielectric layer over a semiconductor structure;

forming an interconnect opening in said dielectric layer;

forming a copper layer at least filling said interconnect opening;

planarizing said copper layer to form a copper interconnect in said interconnect opening; said copper interconnect has a top surface below the top surface of the surrounding dielectric layer;

forming metal silicide layer over said copper interconnect using a sputter process;

planarizing said metal silicide layer to form a metal silicide cap.

In an aspect, the metal silicide layer is formed using a sputter process at a temperature between 20 and 180 degrees C.

The above and below advantages and features are of representative embodiments only, and are not exhaustive and/or exclusive. They are presented only to assist in understanding the invention. It should be understood that they are not representative of all the inventions defined by the claims, to be considered limitations on the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages may be mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of

the claimed invention have not been discussed herein. However, no inference should be drawn regarding those discussed herein relative to those not discussed herein other than for purposes of space and reducing repetition. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

Brief Description of the Drawings

The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figures 1 through 5 are cross sectional views for illustrating a method for manufacturing a sputtered metal silicide layer on a copper interconnect according to an example embodiment of the present invention.

Detailed Description of the Example Embodiments

I. Example embodiment of a silicide layer over a copper interconnect

An example embodiment is shown in figures 1 to 5 for a method of fabrication of a low temperature sputtered metal silicide layer over a copper interconnect.

A. form a conductive layer and capping layer over a semiconductor structure

Referring to figure 1, we form a conductive layer 14 over a semiconductor structure 10. The semiconductor structure can comprise a substrate having conductive and insulating layers there over. The conductive layer 14 can be a metal layer, such as a copper layer. The substrate can be a semiconductor substrate such as a silicon wafer. The substrate can be other substrates used in electronics' manufacturing.

Next, we form a capping layer 16 over the conductive layer 16.

The capping layer can be comprised dielectric materials and more preferably of SiN, SiC(O), SiC(N), and combination of SiC(O) and SiC(N).

B. form interconnect opening in dielectric layer

Next, we form a dielectric layer 20 over the barrier layer 16 and the conductive layer 14.

The dielectric layer 20 can be comprised of dielectric materials and more preferably TEOS or low K material; and has a thickness between 2000 and 6000 angstroms and more preferably a thickness between 3000 and 5000 Angstroms.

C. interconnect opening

Then we form an interconnect opening 22 in the dielectric layer 20.

The interconnect opening 22 can have a single or dual damascene shape.

For example, for a dual damascene opening 22, the trench (upper) opening 22A can have an open dimension between 0.05 and 0.8 microns and more preferably between 0.1 and 0.6 microns and the via opening (lower) 22B can have an open dimension between 0.05 and 0.6 μm and more preferably between 0.1 and 0.3 μm.

D. form a copper layer

Referring to figure 2, we form a copper layer at least filling the interconnect opening 22.

In an example process, the copper layer can be formed by the following steps. A pore sealant can be formed selectively over the dielectric layer 20 in the interconnect opening 22. The pore sealant is comprised of any dielectric material and more preferably of SiN, Parylene-N or Poly(p-xylyene).

Next we form a barrier layer 24 over the dielectric layer 20.

The barrier layer 24 can be comprised of TiN or TiSiN, Ta, TaN or a combination of Ta/TaN and can have a thickness between 50 and 500 angstroms and more preferably 150 and 200 angstroms.

We form a Cu seed layer over the barrier layer 24. The Cu seed layer is preferably a PVD Cu layer with a thickness between 200 and 1000 angstroms and more preferably between 300 and 600 angstroms.

Then we can form a Cu layer 28 by an electroplating process (such as ECP® System process by AMC research INC., USA) over the seed layer thus at least filling the interconnect opening.

The copper layer 28 can be formed by a electroplating or electroless process and is most preferably formed by an electroplating process.

E. copper interconnect

As shown in figure 3, we planarize the copper layer 28 to form a copper interconnect 30 in the interconnect opening 22. The planarization process can be a chemical-mechanical polish (CMP) or Electrochemical Mechanical Planarization (ECMP) process.

The step of planarizing the copper layer 28 removes the copper layer over the top surface of the dielectric layer 20 outside of the interconnect opening 22 and removes the barrier metal layer 24 outside of the interconnect opening 22. We preferably purposely over polish the copper interconnect 28 to a level below the top surface of the dielectric layer outside of the interconnect opening 22 to create a depression 32. This over polishing causes dishing. Preferably we over polish the interconnect 28 to form the depression 32 that has a top level between 100 and 300 angstroms and more preferably between 100 and 200 angstroms below the top surface of the dielectric layer 20.

F. Metal Silicide layer by low temperature sputtering process

Referring to figure 4, in a key step, we form metal layer or metal silicide layer 40 over the copper interconnect using a sputtering process.

Preferably we treat the Cu 30 surface before we form the metal silicide layer 40. Preferably, after the Cu CMP, we expose the copper surface to air to form a Copper oxide layer on the top surface of the Cu. It is preferably to subject the Cu surface to a NH_3 or H_2 containing plasma treatment for 5 to 25 seconds and more preferably 10 to 20 seconds.

The metal silicide layer 40 can be comprised of a metal silicide such as WSi (tungsten silicide), CoSi (cobalt silicide) , NiSi (nickel silicide), CuSi (copper silicide) and is most preferably comprised of NiSi or CuSi. The sputter target is an alloyed metal silicide. The metal silicide sputter process is preferably performed at a temperature between 20 and 180 C.

Tungsten Silicide

An example metal silicide sputter process is as follows:

- sputter target preferably is comprised substantially of a silicon and tungsten with a Si/W atomic ratio of between 2.7 and 2.9. (e.g., Si/W atomic ratio of 2.8 +/- 0.1). Where Si/W is the atomic ratio of Si to tungsten.
- DC power for sputtering is between 1000 to 3000 W,
- Ar gas as sputtering gas
- pressure less than 10 mtorr.
- temperature between 20 and 180 C
- Sputtering in a PVD chamber equipped with heating pedestal set at temp between about 20 C and 180 C,
- Depending on the application typically sputtered silicide is for blanket deposition then is not need to bias power to improve step coverage of the deposited film.

The metal silicide layer 40 is preferably comprised of substantially of silicon and tungsten and preferably has a Si/W atomic ratio of between 2.7 and 2.9 (Si/W atomic ratio of 2.8 +/- 0.1). In other words, Si/W is the atomic ratio of Si to tungsten.

Copper Silicide

Another example is a copper silicide (CuSi) sputter process is as follows:

- sputter target preferably comprised substantially of a silicon and Cu with a Si/Cu atomic ratio of between 2.7 and 2.9. (e.g., Si/Cu atomic ratio of 2.8 +/- 0.1). Where Si/Cu is the atomic ratio of Si to tungsten.
- DC power for sputtering is between 1000 to 3000 W,

- Ar gas as sputtering gas
- pressure less than 10 mtorr.
- temperature between 20 and 180 C
- Sputtering in a PVD chamber equipped with heating pedestal set at temp between about 20 C and 180 C,

Depending on the application typically sputtered silicide is for blanket deposition then is not need to bias power to improve step coverage of the deposited film.

The metal silicide layer 40 also is preferably comprised of substantially of silicon and copper (copper silicide) and preferably has a Si/Cu atomic ratio of between 2.7 and 2.9 (Si/Cu atomic ratio of 2.8 +/- 0.1). In other words, Si/Cu is the atomic ratio of Si to Cu.

The metal silicide layer 40 can have a thickness between 500 and 800 angstroms.

G. Optional - annealing the metal silicide layer

In an optional step, we can anneal the metal silicide layer 40.

H. planarizing the metal silicide layer

Referring to figure 5, we planarize the metal silicide layer 40 to form a metal silicide cap 41. The metal silicide cap preferably has a thickness between 100 and 200 angstroms.

Next, we can form a dielectric capping layer 55 over the metal silicide cap 41.

I. cap layer

Referring to figure 5, we form a cap layer 55 over the metal silicide cap 41 and dielectric layer 20. The cap layer 50 can be comprised of dielectric materials and more preferably of SiN, SiC(O), Si(N), and combination of SiC(O) and SiC(N).

J. example embodiment – Sputter metal silicide process

In the embodiment's process, metal silicide (e.g. CuSi, CoSi, NiSi, etc) is deposited on Cu by physical sputtering of sintering target at lower temperature preferably between 20 C and 180 degrees C. In contrast, it is common to form CuSi by reactive method such as forming a silicon layer on a metal layer an perform an anneal at between 300 and 450 C. The reactive process is at a much higher temperature which is not favorable for Cu process. High temperatures such as this can cause via pull out that can lead to void formation between the via bottom and the underlying metal. Thus yield can significantly decrease. The embodiment's low temperature sputter metal silicide cap process can improve yields by reducing temperature related defects (e..g, via pull out, voids, etc).

K. non-limiting example embodiments

In the above description numerous specific details are set forth such as flow rates, pressure settings, thicknesses, etc., in order to provide a more thorough understanding of the present invention. Those skilled in the art will realize that power settings, residence times, gas flow rates are equipment specific and will vary from one brand of equipment to another. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these details. In other instances, well known process have not been described in detail in order to not unnecessarily obscure the present invention.

Unless explicitly stated otherwise, each numerical value and range should be interpreted as being approximate as if the word about or approximately preceded the value of the value or range.

Given the variety of embodiments of the present invention just described, the above description and illustrations show not be taken as limiting the scope of the present invention defined by the claims.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. It is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A method of fabrication of a sputtered metal silicide layer over a copper interconnect; comprising the steps of :

providing a dielectric layer over a semiconductor structure; providing an interconnect opening in said dielectric layer; providing a copper interconnect in said interconnect opening;

forming metal silicide layer over said copper interconnect using a sputter process.

2. The method of claim 1 which further includes planarizing said metal silicide layer to form a metal silicide cap.

3. The method of claim 1 wherein the metal silicide layer is formed using a sputter process at a temperature between 20 and 180 degrees C.

4. The method of claim 1 which further includes planarizing said metal silicide layer to form a metal silicide cap; said metal silicide cap has a thickness between 100 and 200 angstroms; said metal silicide layer is comprised of a material selected from the group consisting of: WSi, CoSi, NiSi, and CuSi.

5. The method of claim 1 which further includes planarizing said metal silicide layer to form a metal silicide cap; said metal silicide cap has a thickness between 100 and 200 angstroms; said metal silicide layer is comprised of CuSi.

6. A method of fabrication of a sputtered metal silicide cap over a copper interconnect; comprising the steps of :

forming a dielectric layer over a semiconductor structure;

forming an interconnect opening in said dielectric layer;

forming a copper layer at least filling said interconnect opening;

removing said copper layer over the dielectric layer to form a copper interconnect in said interconnect opening; said copper interconnect has a top surface below the top surface of the surrounding dielectric layer;

forming metal silicide layer over said copper interconnect using a sputter process;

planarizing said metal silicide layer to form a metal silicide cap.

7. The method of claim 6 wherein said dielectric layer is comprised of TEOS or a low K material and has a thickness between 2000 and 6000 angstroms; said interconnect opening has a dual damascene shape.

8. The method of claim 6 wherein the step of forming the copper layer comprises:

forming a pore sealant selectively over the dielectric layer in the interconnect opening; the pore sealant is comprised of SiN, Parylene-N or Poly(p-xylyene);

forming a barrier layer over the dielectric layer; said barrier layer comprised of a material from the group consisting of TiN or TiSiN, Ta, and TaN and has a thickness between 150 and 300 angstroms;

forming a Cu seed layer over said barrier layer; the Cu seed layer is a PVD Cu layer with a thickness between 300 and 600 angstroms;

forming said copper layer by an electroplating process over said seed layer.

9. The method of claim 6 wherein the step of removing the copper layer comprises planarizing said copper layer to remove said copper layer over the top surface of said dielectric layer outside of the interconnect opening and remove a barrier metal layer outside of the interconnect opening, and planarizing the copper interconnect to a level between 100 and 200 angstroms below the top surface of said dielectric layer outside of the interconnect opening.

10. The method of claim 6 wherein the top surface of said copper interconnect is below the top surface of said dielectric layer a distance between about 100 and 200 angstroms.

11. The method of claim 6 wherein the metal silicide layer is formed using a sputter process at a temperature between 20 and 180 degrees C.

12. The method of claim 6 wherein said metal silicide layer is comprised of a material selected from the group consisting of: WSi, CoSi, NiSi, and CuSi.

13. The method of claim 6 wherein said metal silicide layer has a thickness between 500 and 800 angstroms.

14. The method of claim 6 wherein the metal silicide layer is form using a sputtering process comprises:

a target comprised substantially of metal and Si a Si/Metal atomic ratio of between 2.7 and 2.9, a DC power for sputtering is between 1000 to 3000 W;

Ar gas as sputtering gas;

a pressure less than 10 mtorr.;

a temperature between 20 and 180 degrees C.

15. The method of claim 6 wherein said metal silicide cap has a thickness between 100 and 200 angstroms.

16. The method of claim 6 wherein the metal silicide layer is formed using a sputter process at a temperature between 20 and 180 degree C; said metal silicide layer is comprised substantially of copper silicide.

17. A method of fabrication of a sputtered metal silicide layer over a copper interconnect; comprising the steps of :

forming a conductive layer over a semiconductor structure;

forming a capping layer over said conductive layer;

forming a dielectric layer over said capping layer and said conductive layer;

forming an interconnect opening in said dielectric layer; said interconnect opening has a dual damascene shape.

forming a copper layer at least filling said interconnect opening;

(1) said copper layer is formed by an electroplating or electroless process;

planarizing said copper layer to form a copper interconnect in said interconnect opening; said copper interconnect has a top surface between about 100 and 300 angstroms below the top surface of the surrounding dielectric layer;

forming a metal silicide layer over said copper interconnect using a sputter process;

(1) the metal silicide layer is formed using a sputter process at a temperature between 20 and 180 degree C;

(2) said metal silicide layer is comprised of a material selected from the group consisting of: WSi, CoSi, NiSi, and CuSi;

planarizing said metal silicide layer to form a metal silicide cap.

18. The method of claim 17 which further includes forming a cap layer over the metal silicide cap and dielectric layer; the cap layer is comprised of a material selected from the group consisting of: dielectric materials, SiN, SiC(O), SiC(N).

19. The method of claim 17 wherein The step of forming the copper layer comprises:

forming a pore sealant selectively over the dielectric layer in the interconnect opening; the pore sealant is comprised of SiN, Parylene-N or Poly(p-xylyene);

forming a barrier layer over the dielectric layer; said barrier layer comprised of a material from the group consisting of TiN, TiSiN, Ta, or TaN; and has a thickness between 150 and 200 angstroms;

forming a Cu seed layer over said barrier layer; the Cu seed layer is a PVD Cu layer with a thickness between 50 and 500 angstroms;

forming said copper layer by an electroplating process over said Cu seed layer.

20. The method of claim 17 wherein the metal silicide layer is formed using a sputtering process comprising: a target comprised substantially of metal and Si with a Si/W atomic ratio of between 2.7 and 2.9; a DC power for sputtering is between 1000 to 3000 W;

Ar gas as sputtering gas;

a pressure less than 10 mtorr.;

a temperature between 20 and 180 degrees C.

21. The method of claim 17 wherein the metal silicide layer comprised substantially of copper silicide and is formed using a sputtering process comprising: a target comprised substantially of copper and Si with a Si/Cu atomic ratio of between 2.7 and 2.9; a DC power for sputtering is between 1000 to 3000 W;
Ar gas as sputtering gas;
a pressure less than 10 mtorr.;
a temperature between 20 and 180 degrees C.

22. The method of claim 17 wherein said metal silicide cap has a thickness between 100 and 200 angstroms.