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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Improvements in Planar Semiconductor Devices

We, GENERAL ELECTRIC COMPANY, a corporation organised and existing under the laws of the State of New York, United States of America, of 1 River Road, Schenectady 12305, State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to planar semiconductor devices which includes a body of semiconductive material having a substantially planar surface and an insulating oxide layer disposed over at least a part of that surface.

Planar passivated devices and integrated circuits are of particular importance in the general field of semiconductors, principally because of their extremely small size and substantially lower cost. Simultaneous operations on a single wafer produce one thousand or more devices thus distributing the expense of the process and minimizing the cost per device. It is accordingly of interest to increase the quality of planar devices so that these advantages catn be realized in circuits for which the performance requirements are high.

Planar devices generally comprise a body of semiconductive material, such as silicon or germanium, having a substantially planar surface, and an insulating oxide layer over the planar surface. The devices may include a metal contact over the insulating layer as in the case of varactors or capacitors, or a junction between regions of varying conductivity in the semiconductive material as in the case of diodes or conventional transistors, or various combinations of these, as in field effect transistors. Conventionally, the insulating layer used is an oxide of silicon because, on silicon wafers, it can readily be produced by baking the silicon in oxygen, it is an effective diffusion mask for certain impurities and it serves to provide a degree of electrical and chemical isolation of the surface. Also, because it is produced by driving oxygen into unexposed silicon, the oxide-silicon interface is completely clean, thus avoiding the problems caused by depositing a material on the semiconductor.

Planar semiconductive devices including such oxide insulating layers have been subject to several problems which limit the performance characteristics obtainable, necessitate the use of great care in the handling of the devices and contribute substantially to the cost of such devices. A particularly severe example of this is the instability of planar devices under high temperature which arises, despite the supposed insulating effect of the oxide layer, from contamination by various impurities such as aluminum, alkali metals and water vapor. Also, it has been found that application of a positive voltage to an aluminum contact overlying silicon oxide - coated semiconductor bodies causes deterioration of the oxide, perhaps due to the reduction of SiO_2 to SiO by the aluminum electrodes, and a short circuit occurs. Finally, the relatively low insulating ability of silicon dioxide due to its low dielectric strength reduces the breakdown voltage of the devices.

The present invention seeks to improve the stability of planar semiconductive devices of the kind which comprise a body of semiconductive material having a substantially planar surface and an oxide insulating layer contiguous with at least a part of that surface. The semiconductive devices of this invention are characterized by the provision of a layer of silicon nitride contiguous with at least a part of the oxide insulating layer.

The semiconductive devices of this invention are found to possess enhanced stability in comparison with similar devices which do not include the silicon nitride layer. Apparently, the silicon nitride prevents the introduction of impurities such as alkali metal ions and water

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vapor which are believed to have been responsible for the substantial instabilities found in devices coated only with an oxide. For example, the alkali ions may be introduced into the oxide during the evaporation of electrodes; these ions are then believed to drift through the oxide causing shifting fields which in turn shift the operating characteristics of the device. Water vapor may enter into the oxide from the atmosphere and also has a deteriorating effect thereon. It has also been found that aluminum electrodes overlying the oxide tend to produce a conductive path through the oxide if left under a positive bias for a sufficient length of time. In devices having a coating of silicon nitride interposed between the electrodes and the oxide layer, this effect has been found to be eliminated. Also the breakdown voltage of nitride-coated devices is increased substantially compared to devices having only a silicon oxide coating, apparently due to the higher dielectric strength of silicon nitride as compared to the conventional silicon dioxide. An additional advantage of this invention is that, due to the impermeability of the silicon nitride coating, the expense of encapsulating the device, which constitutes a substantial portion of the total cost, may be avoided in some situations. In conventional devices, encapsulation is required since otherwise the oxide layer may be destroyed by ambient impurities such as water vapor. The nitride coatings of the present invention have been found to be impervious to such impurities and therefore in some instances the devices need not be encapsulated. In addition to the large cost advantage, this also reduces size and weight of the device.

The present invention is particularly applicable to silicon semiconductive devices since only in silicon can the oxide layer be produced by direct growth into a virgin crystal lattice, thus enabling one to continue the advantages of a clean oxide-silicon interface and, at the same time, to achieve those described herein for the nitride-oxide combination. However, it is to be understood that the semiconductive body of the devices of this invention may be formed from other semiconductive materials, e.g. germanium or gallium arsenide, with the oxide layer being formed of an oxide of silicon, for example silicon dioxide deposited by sputtering, or from other oxides.

In forming the semiconductive devices of this invention, it is preferred to deposit a silicon nitride layer which is thinner than the oxide insulating layer.

In the particular case of junction devices, in which the junctions and regions of varying conductivity emerge at the substantially planar surface of the semiconductor, the oxide layer used is relatively thick and serves as a "passivating" layer. This effect includes electrical insulation from overlying electrodes, chemical isolation of the semiconductor from atmospheric impurities and avoidance of breakdown due to the formation of channels around the junction in the covering material. In the case of such devices, it is generally preferred that the oxide layer be in the range of from 0.1 to 1 micron thick although it may lie beyond this range in some cases. It has been found that the silicon nitride coating of the present invention need only be on the order of a few hundred Angstrom units thick to accomplish the above-described advantages. In general, the nitride coating should range in thickness from 50 to 500 Angstrom units although thicker coatings may be applied.

In embodiments wherein a metallic electrode is disposed over the silicon nitride layer and an electric field is applied between it and the underlying semiconductor, it is preferred to use oxide layers ranging in thickness from 100 to 3,000 Angstrom units with the silicon nitride thickness again within the range of 50 to 500 Angstrom units.

The preferred method of making devices in accordance with this invention includes forming the oxide insulating layer on a semiconductive wafer, masking and etching photolithographically to produce openings and introduction of the desired impurity. This may be done by direct diffusion or by predeposition and diffusion. To accomplish the nitriding step after any oxide coating step, a suitable system for depositing silicon nitride may be used, for example, a furnace containing an atmosphere of SiH_4 and ammonia is satisfactory. It has been found that a coating of silicon nitride approximately 300 Angstrom units thick may be produced by maintaining the wafer at a temperature of 1000°C. for about 1 minute in such an atmosphere.

It has been found that the chemicals used to etch the oxide are also suitable for etching silicon nitride, although the times involved are somewhat longer. For example, an appropriate aperture can be etched in a layer of oxide 10,000 Angstrom units thick by an HF solution in about 1 minute while the etching of 300 Angstrom units of silicon nitride in the same solution requires approximately 2 minutes.

It is another advantage of this invention that the semiconductive devices retain the manufacturing advantages of the conventional oxide-semiconductive devices. Thus, in some cases, the oxide forms a better mask during introduction of impurities than other coatings do. Also, in the case of silicon, the oxide is usually produced by direct growth into the silicon, thus providing a clean oxide-silicon interface. This fact also permits control to be established over the impurity concentration since, if an incorrect amount of the impurity is predeposited, the growth rate of an oxide during diffusion may be used to compensate. Finally, in present photolithographic pro-

cesses, an oxide coating is preferred because a thick oxide, required for passivation, etches more readily than the photoresist layer. Other thick coatings are difficult to etch and the photo-resist mask may be inadvertently removed. Furthermore, the finished products retain the advantage of the oxide-semiconductive devices in that the oxide-semiconductor interface maintains a given surface potential in the semiconductor while other insulators allow carrier leakage and drift of the surface potential. The term "planar" is used in this Specification in accord with the terminology used in the art, to refer to semiconductive devices and circuits prepared by diffusion of impurities into or epitaxial deposit of thin layers on to one or both sides of a semiconductive wafer. Similarly, such wafers are stated to have "substantially planar" surfaces since the minor variations introduced by epitaxy or by conversion to an oxide and removal of same in selected regions actually produce a variation of only a few microns in a device having a width of 1 or 2 millimeters and a depth in the order of 1/2 millimeter and are thus not significant.

The invention, together with a more detailed description of some important advantages thereof, will be described further with reference to the accompanying drawings, in which:

Figure 1 is a schematic view in vertical cross section of a device constructed in accord with the present invention;

Figure 2 is a schematic view in vertical cross section of another device according to the present invention;

Figure 3 is a schematic view in vertical cross section of an alternative device according to this invention; and

Figure 4 is a schematic view in vertical cross section of a preferred embodiment of the present invention.

In Figure 1 a transistor *1* embodying the present invention is illustrated. The device comprises a body 2 of silicon containing three regions of different conductivity. As used throughout this specification, the reference to regions of different conductivity is intended to apply to differences in numerical level and/or type of conductivity. The transistor of Figure 1 may, for example, comprise a phosphorous-doped n-type collector 3, a boron-doped p-type base 4 and a phosphorous-doped n-type emitter 5.

In the conventional planar process, such a device is produced by providing the phosphorous-doped body 2 with an oxide coating on a planar surface 6, diffusing boron through an opening made in the oxide reoxiding the opening and diffusing phosphorous through a smaller opening within the area of original opening.

In accord with the present invention, a coating of silicon nitride, Si_3N_4, is provided after one or more of the oxide coatings has been produced, the number of nitride coatings depending on the requirements of the particular device. For example, in a transistor, it may be sufficient to provide a nitride coating only after the first oxide coating so as to cover the collector-base junction. Since this junction is between two lightly doped regions, it is subject to breakdown at low voltage. The nitride coating of this invention increases the breakdown voltage by a factor of two or more. The single nitride is sufficient if the oxide produced in later steps is sufficiently stable for the intended use. In other devices, it may be desirable to provide nitride coatings over some or all of the oxide coatings or only over the last oxide coating.

In the transistor of Figure 1, for convenience of illustration, the silicon nitride has been applied only after the first oxide coating. Thus, the passivation structure comprises an oxide layer 7 covered by a silicon nitride layer 8. In the central region of the device, these layers have been removed by photolithographic techniques for the diffusion of the impurity which produces region 4 and junction 9. Either during or after the introduction of the impurity, another oxide coating 10 is produced in the silicon. An opening is then produced photolithographically in the oxide 10 and region 5 is produced by diffusion of an impurity to junction 11. This may be accompanied or followed by production of another oxide layer 12 over region 5. Finally holes are produced in the layers and electrons 13, 14, 15 are provided by evaporation of a metal, usually aluminum, into the holes and onto surface areas to provide lands broad enough for the attachment of wire electrodes.

As previously noted, the breakdown voltage of collector-base junctions formed with the overlying silicon nitride coating has been found to be increased by a factor of two or more over similar junctions covered with an oxide coating but without the silicon nitride. Other advantages obtained from the improved passivation structure include improved stability and avoidance of the effect of electrodes on the oxide.

In Figure 2, a transistor is illustrated in which the improvements and advantages gained by the use of the present invention are provided over the entire surface of the device by producing a nitride on each of the respective oxide coatings during preparation of the device. The device is similar to that of Figure 1 and corresponding elements are designated by corresponding numbers. The additional nitride coatings, identified as elements 16 and 17, are respectively deposited on the oxide layers 10 and 12. This is accomplished by depositing silicon nitride on the surface of the wafer after each oxide is produced and prior to

etching the opening in the respective oxides for the next process.

Figure 3 illustrates, as an alternative embodiment of this invention, a capacitor, which may, for example, be used in many applications as a varactor, comprising a semiconductor body 20 and a metal layer 21 separated by insulating material. In accord with this invention, the conventional oxide layer 22 is covered by a layer 23 of silicon nitride. In the case of capacitors and other devices in which a field is applied across the insulating layer, the thickness of the oxide is substantially less than that used for passivation of junction devices, being on the order of a few hundred to 1000 Angstrom units rather than several thousand as in passivation.

In previous devices of this kind, the difficulties of contamination of the oxide by ions and the subsequent drift thereof has interfered severely with stable operation of the devices, particularly since the oxides are thin and since the operation of the devices is based on the effect of a field across the oxide. Therefore, these ions cause especially severe difficulties. This is further magnified by the fact that the metallic contact is of relatively broad area and the number of ions which may enter the oxide is increased. Also, the deterioration of silicon dioxide in the presence of metals, for example aluminum, and the resultant short circuit through the oxide is hastened by the broad area contact and by the shallow depth of the oxide.

Provision of the additional coating of silicon nitride in accordance with this invention has been found to overcome these difficulties and results in devices which are substantially more stable and less subject to deterioration than previous devices. Alkali ions present during the evaporation of the contact cannot pass through the nitride layer and are thus prevented from changing the operating characteristics of the device. The aluminum of the contact cannot chemically react with the oxide since the is separated therefrom and therefore the short circuit through the oxide does not develop.

A comparison of capacitor devices prepared from similar wafers, coated with identical oxides has shown that in the the devices coated with silicon nitride the drift of the threshold voltage at which a significant rate of change of capacitance with applied voltage occurs is reduced to less than 1 volt when held at temperature up to 300°C for 10 hours or more as compared to a drift of 25 volts for the devices without the nitride, after 1 hour at 280°C. The number of short circuits through the insulating layer when the metal contact is positively biased has been found to be greatly reduced when coated with silicon nitride. Finnitride permits the device to be used without the expense, size and weight of encapsulation ally, as previously noted, the provision of the since ambient impurities such as water vapor which destroy the conventional oxide do not penetrate the nitride. Again, it is noted that the present invention results in an improvement over the presently known oxide devices which permits the advantages previously noted, such as the clean interface, the improved masking of some impurities, and the diffusion control ability to be retained while overcoming the noted disadvantages.

Figure 4 illustrates a field effect transistor prepared in accordance with the present invention. The device comprises a body of silicon 24 of predetermined conductivity having therein two separate regions 25 and 26 of opposite conductivity type. Overlying the planar surface 27 of body 24, there is provided the conventional oxide layer 28 and, in accord with the present invention, a layer 29 of silicon nitride. An aluminum gate electrode 30 is also provided and contacts 31 are made to the various regions of the device. The oxide layer 28 is relatively thick for passivation except in the central region of the device between the two opposite conductivity regions 25 and 26. In the conventional operation of such devices, a field is applied across the oxide in this central region to control the width, and therefore the amount of conduction, through a channel between the two regions. The oxide layer conventionally used in such devices is on the order of several hundred to more than 1000 Angstrom units in thickness.

In accordance with this invention, a layer on the order of a few hundred Angstrom units of nitride overlies the oxide which, in the region of thick oxide, functions as previously described in connection with the transistors of Figures 1 and 2 to enhance the passivating effect of the oxide. In the central region above conduction channel the nitride functions in a manner similar to that described with relation to the capacitor shown in Figure 3; that is, it insulates the oxide from the aluminum electrode 30, prevents introduction of ions which might interfere with the applied field and it increases the breakdown voltage of the insulating structure.

In tests conducted on devices constructed in accordance with this invention, it has been found that the nitride placed over the oxide in the region above the channel is preferably less than the thickness of the oxide. Again, the present invention results in the provision of a device which embodies the advantages of the conventional oxide while overcoming the previously encountered disadvantages thereof.

It is noted that, in the case of devices such as the field effect transistor which combine the structure of the junction devices with that of the capacitor devices the present invention is particularly advantageous in that, where the conventional oxide overlying the junction must be relatively thin to allow the field applied to

have the desired effect so that it permits the possibility of voltage breakdown, the higher dielectric strength of the nitride layer of the present invention increases the breakdown voltage without substantially increasing the thickness of the layer.

WHAT WE CLAIM IS:—

1. A planar semiconductive device of improved stability comprising a body of semiconductive material having a substantially planar surface, an oxide insulating layer contiguous with at least a part of said surface, and a layer of silicon nitride contiguous with at least a part of the oxide insulating layer.

2. A semiconductive device according to Claim 1, wherein the semiconductive body is formed of silicon, germanium or gallium arsenide.

3. A semiconductive device according to Claim 1 or Claim 2, wherein the oxide insulating layer is formed of an oxide of silicon.

4. A semiconductive device according to any preceding claim, wherein the oxide insulating layer is thicker than the silicon nitride layer.

5. A semiconductive device according to Claim 4, wherein the silicon nitride layer is between 50 and 500 Angstrom units thick.

6. A field effect planar semiconductive device of improved stability comprising a semiconductive body of silicon or germanium having a substantially planar surface; the semiconductive body including a first region of one conductivity and a second region of different conductivity forming a junction with said first region; said first region, said second region and said junction being disposed to emerge from said body in said surface; an insulating layer comprising an oxide of silicon contiguous with at least a part of said surface and covering said junction; a layer of silicon nitride contiguous with at least a part of the silicon oxide insulating layer; a metallic electrode contiguous with a predetermined area of the silicon nitride layer and juxtaposed with an area of said surface, the silicon nitride and silicon oxide layers interposed between said electrode and said surface being sufficiently thin that application of an electric field between said body and said electrode affects the conductivity of a surface-adjacent volume of said body; and means electrically connected to said electrode and to said first and second regions for connecting said device in a circuit.

7. A planar semiconductive device of improved stability substantially as hereinbefore described with reference to Figure 1, Figure 2, Figure 3 or Figure 4 of the accompanying drawings.

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