

**THIN PACKAGING OF MULTI-CHIP MODULES
WITH ENHANCED THERMAL/POWER MANAGEMENT**

Abstract

A novel packaging of semiconductor elements, such as MCM tiles, with a variety of
5 printed circuit or wired boards (PWB), the packages occupying a small size, at least
in the vertical direction, relative to prior art OMPAC devices. The MCM tile
includes an interconnection substrate with peripheral metallizations and at least one
chip or integrated circuit (IC) mounted on the substrate by solder reflow or
conductive adhesive technology. The PWB which may be a single level or a
10 multilevel, is provided with an aperture for accommodation of at least one chip
therein. Depending on the type of interconnection between the substrate and the
PWB, the aperture may be larger than the substrate of the MCM tile for wire
bonding interconnection or smaller than the substrate for solder reflow or conductive
adhesive interconnection. In the wire bonding case, the MCM tile is positioned
15 within the aperture resting on the surface of the PWB or of a structural member or of
a heat sink which encloses one end of the aperture. The other end of the aperture
may be open or enclosed by a structural member, a heat sink, another PWB or a
mother board. For solder reflow or conductive adhesive interconnection, the
substrate which is larger than the aperture is positioned so that its ends overlap areas
20 of the PWB adjacent the aperture and the chips and/or substrate are positioned within
the aperture. The interconnections are enclosed in a compliable encapsulating
material, such as silica gel.

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