CLAIMS

WHAT IS CLAIMED IS:

1. A memory system, comprising:

a memory device; and

a controller coupled to the memory device and configured to perform operations comprising:

determining, based on a plurality of commands received by the memory system during a first period of time, that a condition is met; and

reducing a frequency or a voltage applied to one or more processors of the controller in response to determining that the condition is met.

2. The memory system according to claim 1, wherein the plurality of commands comprise at least one of sequential write commands or sequential read commands.

3. The memory system according to claim 1, wherein the operations further comprise:

determining that a second period of time has elapsed since the frequency or the voltage applied to the one or more processors of the controller was reduced last time; and

wherein reducing the frequency or the voltage applied to the one or more processors of the controller comprises:

reducing the frequency or the voltage applied to the one or more processors of the controller in response to determining that the condition is met and the second period of time has elapsed since the frequency or the voltage applied to the one or more processors of the controller was reduced last time.

4. The memory system according to claim 1, wherein reducing the frequency or the voltage applied to the one or more processors of the controller comprises reducing the frequency applied to the one or more processors of the controller followed by reducing the voltage applied to the one or more processors of the controller.

5. The memory system according to claim 1, wherein the first period of time is immediately preceding a time instant when the frequency or the voltage applied to the one or more processors of the controller is reduced.

6. The memory system according to claim 1, wherein the memory system is in a sequential write mode, a sequential read mode, or an idle mode.

7. The memory system according to claim 1, wherein before reducing the frequency or the voltage applied to the one or more processors of the controller, the operations further comprise:

in response to determining that the condition is met:

completing all current tasks of the one or more processors; and

synchronizing each of the one or more processors to a common designated state.

8. The memory system according to claim 1, wherein after reducing the frequency or the voltage applied to the one or more processors of the controller, the operations further comprise:

performing new tasks on the one or more processors.

9. The memory system according to claim 1, wherein reducing the frequency applied to the one or more processors comprises reducing the frequency applied to the one or more processors using a phase-locked loop (PLL) register in the controller.

10. The memory system according to claim 1, wherein the one or more processors comprise a main processor and one or more secondary processors, the memory system further comprises a power management integrated circuit (PMIC) coupled to the controller, and wherein reducing the voltage applied to the one or more processors comprises:

determining, by the main processor, one or more commands based on a plurality of parameters monitored by the one or more processors; and

sending, by the main processor, the one or more commands to the PMIC to reduce the voltage applied to the one or more processors.

11. The memory system according to claim 1, wherein before reducing the frequency or the voltage applied to the one or more processors of the controller, the operations further comprise:

determining that the memory system is not in garbage collection mode; and

wherein reducing the frequency or the voltage applied to the one or more processors of the controller comprises:

reducing the frequency or the voltage applied to the one or more processors of the controller in response to determining that the condition is met and the memory system is not in garbage collection.

12. The memory system according to claim 1, wherein the condition comprises that a quantity of the plurality of commands received by the memory system during the first period of time is more than a threshold, a ratio of the threshold to the first period of time is larger than or equal to 32000, and the first period of time is longer than or equal to one second.

13. A method, comprising:

determining, by a controller of a memory system and based on a plurality of commands received by the memory system during a first period of time, that a condition is met; and

reducing, by the controller, a frequency or a voltage applied to one or more processors of the controller in response to determining that the condition is met.

14. The method according to claim 13, wherein the plurality of commands comprise at least one of sequential write commands or sequential read commands.

15. The method according to claim 13, further comprising:

determining that a second period of time has elapsed since the frequency or the voltage applied to the one or more processors of the controller was reduced last time; and

wherein reducing the frequency or the voltage applied to the one or more processors of the controller comprises:

reducing the frequency or the voltage applied to the one or more processors of the controller in response to determining that the condition is met and the second period of time has

elapsed since the frequency or the voltage applied to the one or more processors of the controller was reduced last time.

16. The method according to claim 13, wherein reducing the frequency or the voltage applied to the one or more processors of the controller comprises reducing the frequency applied to the one or more processors of the controller followed by reducing the voltage applied to the one or more processors of the controller.

17. The method according to claim 13, wherein before reducing the frequency or the voltage applied to the one or more processors of the controller, the method further comprises:

in response to determining that the condition is met:

completing all current tasks of the one or more processors; and

synchronizing each of the one or more processors to a common designated state.

18. The method according to claim 13, wherein the one or more processors comprise a main processor and one or more secondary processors, the memory system further comprises a power management integrated circuit (PMIC) coupled to the controller, and wherein reducing the voltage applied to the one or more processors comprises:

determining, by the main processor, one or more commands based on a plurality of parameters monitored by the one or more processors; and

sending, by the main processor, the one or more commands to the PMIC to reduce the voltage applied to the one or more processors.

19. The method according to claim 13, wherein before reducing the frequency or the voltage applied to the one or more processors of the controller, the method further comprises:

determining that the memory system is not in garbage collection mode; and

wherein reducing the frequency or the voltage applied to the one or more processors of the controller comprises:

reducing the frequency or the voltage applied to the one or more processors of the controller in response to determining that the condition is met and the memory system is not in garbage collection.

20. A controller of a memory system, wherein the controller is configured to perform operations comprising:

determining, by the controller and based on a plurality of commands received by the memory system during a first period of time, that a condition is met; and

reducing, by the controller, a frequency or a voltage applied to one or more processors of the controller in response to determining that the condition is met.