

SYNC DETECT CIRCUIT

ABSTRACT OF THE DISCLOSURE

A sync detect circuit is comprised of two serial data registers (40) and (42), each for storing a single word. A plurality of current sources in current source banks (44) and (46) are operable to convert the bits in the stored sync word to a differential current domain. Depending upon the logic state, the currents are added on two lines (50) and (52). When the differential current falls below a predetermined limit, a frame sync signal is generated to latch the next and following words into a data latch (34). These are then transferred out to a system upon the generation of a system data clock.

Figure 1