What is Claimed is:

1. A memory cell, comprising:

a first electrode having sidewalls angled less than 90 degrees in relation to a bottom surface of the first electrode;

a second electrode, including an electrode contact portion of the second electrode, having sidewalls angled less than 90 degrees in relation to the bottom surface of the first electrode, wherein the second electrode is over the first electrode; and

a storage element between the first electrode and the electrode contact portion of the second electrode.

2. The memory cell of claim 1, wherein an electrode contact portion of the second electrode has sidewalls angled less than 90 degrees in relation to the bottom surface of the first electrode.

3. The memory cell of claim 1, wherein the first electrode has a trapezoidal cross-sectional area and sidewalls that are selected from the group consisting of straight, concave, or convex.

4. The memory cell of claim 3, wherein a top surface of the trapezoidal cross-sectional area of the first electrode is an electrode contact portion of the first electrode and is in contact with the storage element.

5. The memory cell of any one of claims 1-4, wherein the first electrode has a triangular cross-sectional area and sidewalls that are selected from the group consisting of straight, concave, or convex.

6. The memory cell of any one of claims 1-4, wherein the storage element includes a resistance variable material and an access device.

7. The memory cell of any one of claims 1-4, wherein the sidewalls of the electrode contact converge toward the storage element.

8. The memory cell of claim 7, wherein an active region of the memory cell is between an apex of the first electrode and an apex of the electrode contact portion of the second electrode.

9. A memory cell, comprising:

a resistance variable material formed on a blunted peak of a first electrode having non-vertical sidewalls;

a first dielectric material formed on the resistance variable material and having a valley formed therein; and

a contact portion of a second electrode formed in the valley such that the contact has non-vertical sidewalls defined by the valley.

10. The memory cell of claim 9, wherein a remaining portion of the second electrode is formed over the contact portion of a second electrode within the valley such that the remaining portion of the second electrode has angled sidewalls defined by the valley.

11. The memory cell of claim 9, wherein the first electrode is a bottom electrode and a second dielectric material is formed in a valley with angled sidewalls formed between the bottom electrode and an adjacent bottom electrode.

12. The memory cell of any one of claims 9-11, wherein the first electrode is a bottom electrode conductor line.

13. The memory cell of claim 12, wherein the second electrode is a top electrode conductor line non-parallel with the bottom electrode conductor line.

14. A memory cell, comprising:

a resistance variable material formed on a peak of a first electrode having angled sidewalls such that the resistance variable material includes a peak and angled sidewalls;

a first dielectric material formed on the resistance variable material and having a valley formed therein; and

a contact portion of a second electrode formed in the valley such that the contact portion of the second electrode has angled sidewalls defined by the valley.

15. The memory cell of claim 14, wherein a remaining portion of the second electrode is formed on the contact within the valley such that the remaining portion of the second electrode has angled sidewalls defined by the valley.

16. The memory cell of claim 14, wherein the contact portion of the second electrode is formed on the peak of the resistance variable material and overlaps the sidewalls of the resistance variable material.

17. The memory cell of any one of claims 14-16, wherein a surface area of contact between the contact portion of the second electrode and the resistance variable material is defined by the sidewalls of the resistance variable material.

18. The memory cell of any one of claims 14-16, wherein the angled sidewalls of the contact portion of the second electrode are angled about 10 degrees to about 80 degrees in relation to a bottom surface of the first dielectric material.

19. A memory cell, comprising:

a first electrode having a saddle region;

a resistance variable material formed in the saddle region and having a portion in contact with the first electrode; and

a second electrode having a portion in contact with the resistance variable material.

20. The memory cell of claim 19, wherein an interfacial area of the portion of the resistance variable material in contact with the saddle region of the first electrode is greater than an area of an areal footprint beneath the saddle region.

21. The memory cell of claim 19, wherein a surface area of the portion of the resistance variable material in contact with the second electrode is greater than a surface area of a surface of the first electrode beneath the saddle region.

22. The memory cell of any one of claims 19-21, wherein a bottom surface of the second electrode is positioned below a top surface of the first electrode.

23. The memory cell of any one of claims 19-21, wherein the first and second electrodes are oriented non-parallel to each other.

24. The memory cell of any one of claims 19-21, wherein the first and second electrodes are surrounded by a dielectric material.

25. The memory cell of any one of claims 19-21, wherein the memory cell is a resistive random access memory (RRAM) cell.

26. An array of memory cells, comprising:

a first number of electrodes, each having sidewalls angled less than 90 degrees in relation to bottom surfaces of the first number of electrodes;

a second number of electrodes, each including an electrode contact portion of the first electrode, having sidewalls angled less than 90 degrees in relation to the bottom surfaces of the first number of electrodes, wherein the second number of electrodes are over the first number of electrodes; and

a number of storage elements between the first number of electrodes and the electrode contact portions of the second number of electrodes.

27. The array of claim 26, wherein each of the first number of electrodes are separated from each other by a number of portions of a first dielectric material.

28. The array of claim 26, wherein each of the second number of electrodes are separated from each other by a number of portions of a second dielectric material.

29. The array of any one of claims 26-28, wherein the array of memory cells are configured in a cross-point memory cell array.

30. An array of memory cells, comprising:

a number of saddle regions formed in a number of portions of a first contact material, wherein each of the number of portions of the first contact material are separated by a first dielectric material;

a resistance variable storage element formed in each of the number of saddle regions; and

a number of portions of a second contact material formed over the resistance variable storage element in each of the number of saddle regions.

31. The array of claim 30, wherein the number of portions of a second contact material are separated by a second dielectric material.

32. The array of claim 31, wherein the number of portions of a first contact material and the number of portions of the second contact material are oriented non-parallel to each other.

33. The array of any one of claims 30-32, wherein the array of memory cells are configured in a cross-point memory cell array.

34. The array of any one of claims 30-32, wherein the resistance variable storage element includes a resistance variable storage element and an access device.

What is Claimed is:

1. A memory cell, comprising:

a first electrode having sidewalls angled less than 90 degrees in relation to a bottom surface of the first electrode;

a second electrode, including an electrode contact portion of the second electrode, having sidewalls angled less than 90 degrees in relation to the bottom surface of the first electrode, wherein the second electrode is over the first electrode and is formed on a first dielectric material having sidewalls angled less than 90 degrees in relation to the bottom surface of the first electrode and wherein an angled sidewall of the second electrode and an angled sidewall of the first dielectric material are adjacent to each other; and

a storage element between the first electrode and the electrode contact portion of the second electrode, wherein the first dielectric material is formed on a top surface of the storage element.

2. The memory cell of claim 1, wherein an electrode contact portion of the second electrode has sidewalls angled less than 90 degrees in relation to the bottom surface of the first electrode.

3. The memory cell of claim 1, wherein the first electrode has a trapezoidal cross-sectional area and sidewalls that are selected from the group consisting of straight, concave, or convex.

4. The memory cell of claim 3, wherein a top surface of the trapezoidal cross-sectional area of the first electrode is an electrode contact portion of the first electrode and is in contact with the storage element.

5. The memory cell of claim 1, wherein the first electrode has a triangular cross-sectional area and sidewalls that are selected from the group consisting of straight, concave, or convex sidewalls.

6. The memory cell of claim 1, wherein the storage element includes a resistance variable material and a select device.

7. The memory cell of claim 1, wherein the sidewalls of the electrode contact portion converge toward the storage element.

8. The memory cell of claim 7, wherein an active region of the memory cell is between an apex of the first electrode and an apex of the electrode contact portion of the second electrode.

9. A memory cell, comprising:

a resistance variable material formed on a blunted peak of a first electrode having non-vertical sidewalls;

a first dielectric material formed on a top surface of the resistance variable material and having a valley formed therein; and

a contact portion of a second electrode formed in the valley such that the contact portion has non-vertical sidewalls defined by the valley.

10. The memory cell of claim 9, wherein a remaining portion of the second electrode is formed over the contact portion of a second electrode within the valley such that the remaining portion of the second electrode has angled sidewalls defined by the valley.

11. The memory cell of claim 9, wherein the first electrode is a bottom electrode and a second dielectric material with angled sidewalls is formed in a valley between the bottom electrode and an adjacent bottom electrode.

12. The memory cell of claim 9, wherein the first electrode is a bottom electrode conductor line.

13. A memory cell, comprising:

a first electrode having a saddle region;

a resistance variable material formed in the saddle region and having a portion in contact with the first electrode; and

a second electrode having a portion in contact with the resistance variable material.

14. The memory cell of claim 13, wherein an interfacial area of the portion of the resistance variable material in contact with the saddle region of the first electrode is greater than an area that is beneath the saddle region and equal to the width of the first electrode multiplied by the width of the second electrode.

15. The memory cell of claim 13, wherein a surface area of the portion of the resistance variable material in contact with the second electrode is greater than a surface area of a surface of the first electrode beneath the saddle region.

16. The memory cell of claim 13, wherein a bottom surface of the second electrode is positioned below a top surface of the first electrode.

17. The memory cell of claim 13, wherein the first electrode and the second electrode are surrounded by a dielectric material.

18. The memory cell of claim 13, wherein the memory cell is a resistive random access memory (RRAM) cell.

19. An array of memory cells, comprising:

a first number of electrodes each having sidewalls angled less than 90 degrees in relation to bottom surfaces of the first number of electrodes;

a second number of electrodes, each including an electrode contact portion, having sidewalls angled less than 90 degrees in relation to the bottom surfaces of the first number of electrodes, wherein the second number of electrodes are over the first number of electrodes and are formed on a number of dielectric material portions each having sidewalls angled less than 90 degrees in relation to the bottom surface of the first number of electrodes and wherein an angled sidewall of each of the second number of electrodes and an angled sidewall of each of the first dielectric material portions are adjacent to each other; and

a number of storage elements between the first number of electrodes and the electrode contact portions of the second number of electrodes, wherein the number dielectric material portions are formed on a top surface of the number of storage elements.

20. The array of claim 19, wherein each of the first number of electrodes are separated from each other by a number of portions of a first dielectric material.

21. The array of claim 19, wherein each of the second number of electrodes are separated from each other by a number of portions of a second dielectric material.

22. The array of claim 19, wherein the array of memory cells are configured in a cross-point memory cell array.

23. An array of memory cells, comprising:

a number of saddle regions formed in a number of portions of a first contact material, wherein each of the number of portions of the first contact material are separated by a first dielectric material;

a resistance variable storage element formed in each of the number of saddle regions; and

a number of portions of a second contact material formed over the resistance variable storage element in each of the number of saddle regions.

24. The array of claim 23, wherein the number of portions of a second contact material are separated by a second dielectric material.

25. The array of claim 23, wherein the number of portions of a first contact material and the number of portions of the second contact material are oriented non-parallel to each other.

26. The array of claim 23, wherein the array of memory cells are configured in a cross-point memory cell array.

27. The array of claim 23, wherein the resistance variable storage element includes a resistance variable storage element and a select device.