Claims

What is claimed:

1. A semiconductor device, comprising:

a first ~~semiconductor die~~ conductive layer;

a vertical interconnect structure disposed ~~outside the first semiconductor die~~ over the first conductive layer;

a no-flow insulating material disposed around the vertical interconnect structure and the first conductive layer;

a first semiconductor die embedded within the no-flow insulating material over the first conductive layer, wherein the no-flow insulating material, first semiconductor die, and vertical interconnect structure includes a planar surface and the first conductive layer is partially embedded in the no-flow insulating material to cover a side surface of the first conductive layer;

a first interconnect structure formed over the planar surface, the first interconnect structure including a second conductive layer formed in direct contact with the vertical interconnect structure and a surface of the no-flow insulating material and extending over the surface of the no-flow insulating material outside a contact interface between the first interconnect structure and the vertical interconnect structure;

a second semiconductor die disposed over the first interconnect structure and directly overlying the first semiconductor die, wherein the second semiconductor die is a duplicate of the first semiconductor die; and

a second interconnect structure formed over and contacting the first conductive layer opposite the first interconnect structure.

~~a conductive layer electrically connecting the first semiconductor die to the vertical interconnect structure;~~

~~an insulating material disposed around the first semiconductor die and vertical interconnect structure with the insulating material, first semiconductor die, and vertical interconnect structure having a planar surface;~~

~~a first interconnect structure formed over the planar surface; and~~

~~a second interconnect structure formed over the conductive layer and insulating material opposite the first interconnect structure.~~

~~2. The semiconductor device of claim 1, wherein the insulating material includes a no-flow underfill material or encapsulant.~~

~~3~~2. The semiconductor device of claim 1, wherein the first interconnect structure or second interconnect structure includes an integrated passive device.

~~4~~3. The semiconductor device of claim 1, further including a plurality of stacked semiconductor devices ~~electrically connected through the first interconnect structure, second interconnect structure, and vertical interconnect structure.~~

~~5. The semiconductor device of claim 1, further including a second semiconductor die mounted over the first interconnect structure and electrically connected to the first semiconductor die through the first interconnect structure, vertical interconnect structure, and conductive layer~~.

~~6~~4. The semiconductor device of claim 1, wherein the vertical interconnect structure includes a bump.

~~7. A semiconductor device, comprising:~~

~~a first semiconductor die;~~

~~a vertical interconnect structure;~~

~~a conductive layer electrically connecting the first semiconductor die to the vertical interconnect structure;~~

~~an insulating material disposed around the first semiconductor die and vertical interconnect structure with the insulating material, first semiconductor die, and vertical interconnect structure having a planar surface; and~~

~~a first interconnect structure formed over the planar surface.~~

~~8. The semiconductor device of claim 7, further including a second interconnect structure formed over the conductive layer and insulating material opposite the first interconnect structure.~~

~~9. The semiconductor device of claim 8, further including a plurality of stacked semiconductor devices electrically connected through the first interconnect structure, second interconnect structure, and vertical interconnect structure.~~

10. The semiconductor device of claim 8, further including a second semiconductor die mounted over the first interconnect structure and electrically connected to the first semiconductor die through the first interconnect structure, vertical interconnect structure, and conductive layer.

11. The semiconductor device of claim 8, wherein the first interconnect structure or second interconnect structure includes an integrated passive device.

12. The semiconductor device of claim 7, wherein the insulating material includes a no-flow underfill material or encapsulant.

13. The semiconductor device of claim 7, wherein the vertical interconnect structure includes a bump.

14. A semiconductor device, comprising:
a vertical interconnect structure;
an insulating material disposed around the vertical interconnect structure;
a first semiconductor die disposed into the insulating material such that the insulating material, first semiconductor die, and vertical interconnect structure have a planar surface; and
a first interconnect structure formed over the planar surface.

15. The semiconductor device of claim 14, further including a conductive layer electrically connecting the first semiconductor die to the vertical interconnect structure.

~~16. The semiconductor device of claim 14, further including a second interconnect structure formed over the insulating material opposite the first interconnect structure.~~

~~17. The semiconductor device of claim 16, further including a plurality of stacked semiconductor devices electrically connected through the first interconnect structure, second interconnect structure, and vertical interconnect structure.~~

~~18. The semiconductor device of claim 16, further including a second semiconductor die mounted over the first interconnect structure and electrically connected to the first semiconductor die through the first interconnect structure, vertical interconnect structure, and conductive layer.~~

~~19. The semiconductor device of claim 14, wherein the insulating material includes a no-flow underfill material or encapsulant.~~

~~20. The semiconductor device of claim 14, wherein the vertical interconnect structure includes a bump.~~

~~21. A semiconductor device, comprising:~~

~~a first semiconductor die;~~

~~a vertical interconnect structure; and~~

~~an insulating material disposed around the first semiconductor die and vertical interconnect structure with the insulating material, first semiconductor die, and vertical interconnect structure having a planar surface.~~

~~22. The semiconductor device of claim 21, further including a conductive layer electrically connecting the first semiconductor die to the vertical interconnect structure.~~

~~23. The semiconductor device of claim 21, further including:~~

~~a first interconnect structure formed over the planar surface; and~~

~~a second interconnect structure formed over the conductive layer and insulating material opposite the first interconnect structure.~~

~~24. The semiconductor device of claim 21, wherein the insulating material includes a no flow underfill material or encapsulant.~~

~~25. The semiconductor device of claim 21, wherein the vertical interconnect structure includes a bump.~~

5. The semiconductor device of claim 1, wherein the first interconnect structure or second interconnect structure includes an insulating layer.