

Apparatus and method for non-destructive data storage and retrieval

The present invention concerns a data storage apparatus with means for storing and retrieving data in respective write and read operations, wherein data are stored in a non-volatile manner as polarization states in ferroelectric or electret memory cells, wherein the memory cells are provided in a passive matrix-addressable array, wherein the memory cells can be individually addressed electrically for write and read operations, the addressing of the memory cell taking place via crossing electrodes of a respectively first and second electrode sets, wherein each electrode set comprises parallel stripe-like electrodes such that the electrodes of the first set substantially are oriented orthogonally to the electrodes of the second set; a method for performing a non-destructive readout in the apparatus according to claim 1; and a method for poling pairs of piezoelectric storage cells for write operations in the apparatus according to claim 1.

Memory devices based on ferroelectric or electret polymer material have many advantages, like small cell footprint, stacking of memory layers, adaptability to reel-to-reel production/inkjet based production, low temperature processing, low cost, etc. Typically, data are read from the memory by so-called destructive readout, where reversal of polarization during the read operation makes it necessary to write back the information for further storage in the memory. A destructive read mode of this kind is undesirable for many applications; for instance, the number of fatigue cycles related to read is the doubled. The latter may represent a problem, since ferroelectric or electret based memories only can withstand a finite number of write cycles. Furthermore, having to switch the polymer film twice means that the power consumption is increased, as is the complexity of the required circuitry enabling such write back.

The destructive read itself is a rather slow process (typically hundreds of nanoseconds to several microseconds, subject to applied field). This implies that with destructive read the polymer memory is not suitable for a number of major applications, such as replacing fast cache SRAM memory. Finally, when cells are reduced in size, the reduced signal strength may make it difficult to implement polymer memory in state of the art designs, or use at all with ultra-dense lithography ($< 0.15 \text{ } \mu\text{m}$).

It is well-known that many ferroelectric and electret materials, including both the well-known PVDF (polyvinylidene-difluoride) and the copolymer PVDF-TrFE (poly(vinylidene difluoride- trifluoroethylene)) have piezoelectric properties. In that connection there can be referred to Sessler and Gerhard-Multhaupt (editors) Electrets, Vol. 1 and Vol. 2, Chapt. 5, 8, 11 and 12 (3rd ed., Laplacian Press (1998)).

In European patent application EP-A2-0166 938 (Eiling & al.) which has a priority date of 1 June 1984, there is disclosed a write and read method in combination with the data storage device based on a ferroelectric polymer memory layer, with the aim of increasing storage density and reducing access time. To this end data are stored in memory cells formed by a single domain in the polymer memory material of polymer. These domains are coded by being permanently polarized by an applied electric field and coded in accordance with the direction of the field, i.e. with a positive or negative polarization in the memory layer. For reading the data this application discloses the use of pyroelectric or piezoelectric activation of the polarized domains. This activation is envisaged to take place over the suitably arranged electrode means in a matrix-addressable memory cell array in a ferroelectric memory material, preferably e.g. poly(vinylidene difluoride-trifluoroethylene) (PVDF-TrFE), such that activation of a memory cell would take place either pyroelectrically or piezoelectrically, respectively by means of an applied heating current pulse or by applied pressure or tension.

Employing matrix-addressing, the proposed write and read methods according to EP-A2-0168 938 moreover would allow a parallel write/read. An attainable storage density of 10^8 bit/cm² is stated. It is indicated that the access time for a pyroelectric read would be of the order 10^{-9} s. No indication is given for attainable access times for readout based on piezoelectric effects. Furthermore there is no indication in this application of the attainable performance in the small-signal range, neither with regard to access speed, applicable voltage levels, frequencies, detection reliability and noise immunity. However, since it is envisaged that non-destructive readout methods for memories based on ferroelectric polymers may operate in the small-signal range, particularly attainable signal/noise ratios and detection levels will be of major concern.

Hence it is a major object of the present invention to provide a data-storage apparatus allowing non-destructive read operations based on piezoelectric effects that can be obtained in a ferroelectric or electret memory material.

5 It is also a major object of the present invention to provide a very fast non-destructive readout method based on piezoelectric effects and with much improved signal/noise ratio as compared with prior art.

The above objects as well as further features and advantages are achieved with a data storage apparatus according to the present invention which is characterized in that the first set of electrodes comprises a plurality of
10 parallel trenches extending horizontally with an orthogonal orientation to the electrodes and vertically downwards from a top surface thereof for a distance less than the thickness of the electrodes and having a substantially rectangular profile, that at least a ferroelectric or electret memory material is provided in the trenches and covering the sidewalls thereof, that the second
15 set of electrodes is provided as a dual set of electrodes, each comprising parallel twin electrodes provided in said trenches and parallel therewith and without mutual contact with the electrodes of said first set, that the ferroelectric material is provided in at least a portion of the volume of the trenches not occupied by the electrodes, said ferroelectric or electret material
20 being a soft or elastic ferroelectric or electret material with piezoelectric properties and in addition providing electrical insulation between the electrodes of the second set and the electrodes of the first set, whereby the twin electrodes of the second set under a suitably applied force can be displaced laterally in the soft ferroelectric or electret material with
25 piezoelectric properties such that a piezoelectric effect is generated therein, and that said soft ferroelectric or electret material with piezoelectric properties in the volumes between the twin electrodes of the second set and the electrodes of the first set forms subcells of the memory cells in said trenches, said subcells capable of being poled for a write operation by
30 applying an electric field between respective twin electrodes and crossing electrodes of the first set, such that the memory cells are polarized to store at least one of two or more logical values in the form of a set of polarization states in said subcells and can be read non-destructively by applying voltage potential between the twin electrodes, and/or between at least one of the
35 latter and at least one of proximal electrodes of the first electrode set, and over the ferroelectric or electret material of the subcells which are subjected

to tensile and/or compressive stresses enabling the detection of parameters deriving from the polarization states thereof by means of piezoelectric effects in response to strains thus induced in said subcells, whereby the logic state of the subcells of a memory cell can be found and the logical value or values stored in a memory cell containing the subcells can be determined.

The above objects as well as further features and advantages are also achieved with a method which is characterized by the readout of data being performed by subjecting the subcells of the memory cells selected for read operations to tensile and/or compressive force and concurrent detection of phase and/or polarity and/or magnitude of piezoelectrically generated voltage or current from said subcells in response to strains resulting from the application of said tensile and/or compressive force.

Finally, the above objects as well as further features and advantages are achieved with a method for poling pairs of piezoelectric memory cells for a write/read operation in the apparatus according to the invention and with the poling method characterized by poling each cell of the pair in one of two poling directions oriented orthogonally relative to the twin electrodes opposing each cell of the pair, whereby all four possible permutations of the poling directions can be realized in the two cells of the pair.

Further features and advantages of the present invention shall be apparent from the appended dependent claims.

The invention shall now be discussed in more detail in terms of various preferred exemplary embodiments and with reference to the appended drawing figures, of which

figs. 1a and 1b show respectively a plan view and cross section thereof taken along line the A-A in fig. 1a of a portion of a memory cell array in a first preferred embodiment of the apparatus according to the present invention,

figs. 2a and 2b correspondingly a schematic variant of the embodiment in figs. 1a and 1b,

fig. 3 schematically shows a plan view of a passive matrix arrangement according to the preferred embodiment in fig. 1,

figs. 4 a-d show the steps of a poling sequence in a write operation on a portion of the memory array in the apparatus according to the present invention,

5 figs. 5a,c and 5b,d respectively plan views and cross sections taken along the lines A-A in figs. 5a and 5b, and schematically illustrating the principle for performing a readout in the apparatus according to the present invention and in accordance with an embodiment of a method according to the present invention,

10 figs. 6a and 6b respectively a plan view and a cross section thereof, taken along the line A-A of the former, of a portion of a second preferred embodiment of the apparatus according to the present invention,

15 figs. 7a-d the poling of memory cells for a write operation in the embodiment of the apparatus as rendered in figs. 6a and 6b, figs. 7a and 7c being a plan view and figs. 7c and 7d respective corresponding matrix arrangements thereof, and

figs. 8a,c and 8b,d respectively plan views and cross sections thereof taken along the lines A-A of fig. 8a and 8c, illustrating a method for data readout in the embodiment in figs. 6a and 6b according to the present invention, and based on a poling sequence as shown in figs. 7a-d.

20 The general background of the present invention shall now be briefly mentioned, with a more comprehensive discussion of the various preferred embodiments of the apparatus and methods according to the invention to follow further below.

25 Basically the present invention permits information content in ferroelectric or electret memory cells to be read out non-destructively, by employing the piezoelectric effect in ferroelectric or electret materials to generate a physical driving force on individual memory cells, and to detect the polarization (logic-state)-dependent piezoelectric voltage response from those cells. Generic architectures are described, whereby piezoelectric driver and
30 memory cells can be laid out densely in a passive matrix addressable array. These architectures involve polarization of ferroelectric or electret material in a lateral direction, i.e. parallel to the supporting substrate and combine micromechanical structures, resonant or non-resonant, that are compatible

with layered stacking of multiple memory structures, to provide high volumetric data storage densities.

Various preferred embodiments shall now be discussed. It is to be understood that drawing figures aim at illustrating the essential and basic layout of the structural parts of the inventive apparatus, and the general principles behind the inventive method for reading data therefrom. Moreover, for simplicity's sake the memory material shall in the following be termed ferroelectric, although it could also be an electret material. – Actually ferroelectric materials can properly be regarded as a subclass of electret materials.

Fig. 1a shows a plan view of portion of an array of memory cells according to one preferred embodiment of the present invention, while fig. 1b shows a cross section thereof taken along the line A-A. The location of a single memory cell 1 is roughly indicated by a stitched outline. The array of electrodes $a_n, a_{n+1}, a_{n+2}, \dots$, crosses a dual set of electrodes b_m and c_m which are embedded in an insulating, mechanically soft and elastic material 2 filling a trench 3 formed in the electrodes a_n , as best can be seen in fig. 1b. The material 2 in the trench 3 is preferably a ferroelectric polymer, which can be poled in an electric field of strength exceeding its coercive field. Once poled, the ferroelectric polymer retains its polarization, the direction and strength of which represents a logic value in a non-volatile memory cell arrangement formed by the matrix of intersecting, embedded electrodes as shown partly in fig. 1a. At each crossing between an electrode a_n and a twin electrode set b_m and c_m , three piezoelectrically active subcells of a memory cell 1 can be defined, indicated by α_{n1} , α_{n2} and β_n in fig. 1b. Subcells α_{n1} and α_{n2} correspond to the volume of ferroelectric polymer subjected to strong electric fields when a voltage is applied between the common electrode a_n and electrodes b_m and c_m , respectively. While these subcells are small, the cell β_n corresponds to the elongated volume of ferroelectric polymer between electrodes b_m and c_m that is subjected to a strong electric field when a voltage is applied between the latter two. Poling endows the ferroelectric polymer with a piezoelectric response, which in the configuration shown in figs. 1a, 1b causes the twin electrodes b_m, c_m , to move laterally in the trench 3 (i.e. in the direction of the electrode a_n), the exact direction and magnitude of the motion being dependent on the poling direction in the ferroelectric material 2 and the direction and strength of the electric field in the subcells α_{n1} , α_{n2} and β_n .

Fig. 2a shows a plan view of a variant of the basic design in figs. 1a and 1b, where the bottom of the trench 3 is filled with a support material 4 different from the ferroelectric material 2 inside the subcells α_{n1} , α_{n2} and β_n . This is seen to advantage in fig. 2b, which shows a cross section taken along the line A-A in fig. 2a. The memory cell 1 is as before indicated by the stitched outline. By appropriate selection of the support material 4 in the bottom of the trench 3, the mechanical response of the electrodes b_m and c_m can be optimized for given applications. It does not need to be ferroelectric or piezoelectric and can be chosen from a wide range of materials. Thus, it may be soft and elastic, providing small restraint on lateral motion of the electrodes b_m and c_m . In certain cases, its mechanical dissipation properties may be selected so as to influence the mechanical motion characteristics of the electrodes b_m , c_m . An example of this is adjustment of energy dissipation for achieving a desired mechanical Q value during resonant excitation of subcells α_{n1} , α_{n2} , β_n . To obtain specific mechanical characteristics, the bottom layer material 4 may or may not be bonded to the overlaying ferroelectric material 2 of the subcells α_{n1} , α_{n2} , β_n and/or the electrodes b_m , c_m .

Fig. 3 shows schematically a cross-point passive matrix arrangement representing a preferred embodiment according to the present invention. Only the electrode layout is rendered. A memory cell 1 corresponding to the one shown in figs. 1b and 2b is shown within a stitched outline. This addressing arrangement differs from the traditional passive matrix addressing schemes of prior art in that the "vertical" electrodes now are the parallel twin electrodes b_m and c_m ($1 \leq m \leq M$), where M is the number of memory cells 1 along each horizontal electrode a_n ($1 \leq n \leq N$), where N is the number of memory cells 1 along each vertical electrode set b_m , c_m . As is apparent, data can be stored at $M \times N$ crossing points in the matrix by appropriately poling the ferroelectric material 2 in the memory cells defined at each crossing point. According to the present invention, the data-carrying subcells of a memory cell 1 are of the type α_{n1} and α_{n2} , while the macroscopic subcells β_n are used for reading out the stored data (cf. below). As can be seen from figs. 1b and 2b, subcells α_{n1} and α_{n2} can each be poled such that the polarization points either from the sidewall of the trench 3 towards one of the twin electrodes b_m or c_m , or in the opposite direction. This shall in principle provide four different combinations of poling arrangements and would allow

a permutation of the polarization direction on the subcells α_{n1} , α_{n2} . However, when a passive matrix addressing arrangement is used to pole a ferroelectric in the matrix crossing points, it is well known in prior art matrix addressing with single electrodes in both horizontal and vertical directions that the voltages that are applied to the crossing lines during poling (writing) of individual memory cells must be chosen with care, to avoid disturbing non-selected cells at other crossing points in the matrix. In this connection one may refer to, e.g. Norwegian Patent application No. 20003508, and references contained therein. A closer study shows that the disturbance of non-addressed cells can be minimized by coordinated application of voltages on all matrix electrodes. One solution is shown in fig. 3, exposing non-selected cells to a maximum of $1/3$ of the voltage V_p employed to pole selected cells during the writing cycle.

Figs. 4a-4d show the first steps in a poling sequence amounting to activation and write operations for a portion of the memory matrix comprising five memory cells 1, each of these occupying a corresponding location to the one indicated in either fig. 1a or fig. 2a, but not specifically shown here. First, the subcell β_n is poled to prepare it to function as a driver cell during subsequent readout of data (cf. below). This is achieved as shown in fig. 4a by applying a voltage V_p between electrodes b_m and c_m . This voltage is chosen to create an electric field in the ferroelectric that exceeds the coercive field, causing the ferroelectric to polarize in the direction shown by arrows in the figure. All crossing electrodes $a_n, \dots$ are shown to be maintained at $V_p/2$, leading to little or no polarization response in all subcells α due to the strongly nonlinear hysteresis characteristics of the ferroelectric. This voltage may be chosen otherwise, or the electrodes $a_n, \dots$ may be allowed to float, since the polarization states in the subcells α shall subsequently be set during the writing operation. Fig. 4b shows how subcells α_{n1} and α_{n2} on electrode a_n are poled for a write operation to encode a polarization state which in this case is taken to represent one bit of information, e.g. a logic "1". As can be seen, the voltages that are applied cause the polarization to be directed symmetrically from the twin electrodes b_m, c_m and outwards towards the sidewalls of the trench 3, while the voltages on all the other subcells α along the twin electrodes remains below $V_p/3$, i.e. below the polarization switching threshold. Fig. 4c shows the encoding of a logic state "0" on electrode a_{n+1} . As can be seen, the polarization in cells α_{n1} and α_{n2} for electrode a_{n+1} is

reversed compared to the case for electrode a_n . The set of voltages applied to the electrodes in the matrix are in this case as shown locally in fig. 4c, and for the complete matrix as shown in fig. 3. In fig. 3 are also shown the set of voltages (in parentheses) that would be used to write a "1" bit into the memory cell 1 at a_{n+1} , (b_m , c_m), indicated by the stitched circle. Further writing to the matrix proceeds in analogous fashion, cf. fig. 4d. It may be noted that the multibit coding apparently possible by permuting the polarization directions in cells α_{n1} and α_{n2} as mentioned above, has not been invoked here. Closer scrutiny shows that this shall entail voltages between b_m and c_m exceeding $V_p/3$ during the writing cycle as shown. In this regard see, however, the discussion of another preferred embodiment of the present invention, below).

Figs. 5a-5d show how data can be read out from the matrix. Figs. 5a and 5c show a plan view of the memory matrix at two different time instants, figs. 5b and 5d the respective cross sections thereof taken along the lines A-A. The approximate location of a memory cell 1 is as before indicated by the stitched outline. The twin electrodes b_m and c_m act as an exciter unit which causes the subcells α_{n1} , α_{n2} for all electrodes along the length of the twin electrodes to be subjected to compression/dilation along the local poling direction in the ferroelectric material. As well-known in the literature, a piezoelectric response is elicited from the subcells α_{n1} , α_{n2} with a polarity that is dependent upon the poling direction. In figs. 5a and 5b are shown the positions of the twin electrodes b_m , c_m at two instants representing extrema in a vibration cycle. In fig. 5a the twin electrodes b_m , c_m are far apart, and all cells α_{n1} and α_{n2} along the length of the twin electrodes b_m , c_m are compressed laterally. In fig. 5b, corresponding to a later point in time, the twin electrodes b_m , c_m have moved to reduce the gap between them, stretching the cells α_{n1} and α_{n2} on either side. Via the piezoelectric effect which acts cooperatively between cells α_{n1} and α_{n2} at each electrode a_n , voltages are generated between each electrode a_n and a suitable reference (e.g. the average or median potential on electrodes b_m and c_m). The phase or instantaneous polarity of these voltages can then be uniquely linked to the logic state in each memory cell 1 represented by the crossing point between an electrode a_n and the twin electrodes b_m , c_m . Several distinct readout schemes can be based on this basic vibration scheme, as exemplified immediately below.

Example 1: Resonant excitation

Depending on materials, dimensions and selected geometries, the vibratory motion indicated in figs. 5 may be resonantly excited. As can be easily ascertained based on relevant choices of material, the free vibration frequencies of structures as shown in figs. 5 with micrometer-sized cell widths shall be quite high, i.e. in the hundreds of kHz to hundreds of MHz region. Depending on the Q value achieved, readout can be performed with low voltage excitation on the twin electrodes b_m , c_m , minimizing pick-up and crosstalk in the readout signals. Finally, one notes that the readout scheme in fig. 5 provides opportunities for large-scale parallelism and correspondingly high data output rates.

Example 2: Ring-down detection

Providing a sufficiently high mechanical Q value is achieved, the vibrations shown shall persist for a time after the electrical excitation of the twin electrodes b_m , c_m has been turned off, permitting read-out free from disturbing excitation voltages.

Example 3: Impulse detection

Instead of exciting the twin electrodes b_m , c_m with a sinusoidal or other periodic voltage, a single step or delta pulse may be applied, causing compression or dilation of the α_{n1} and α_{n2} cells. An analogy is piezoelectric spark generators. This provides a very fast means of readout, since the transit time of a compressional sound wave across the subcells α_{n1} and α_{n2} is in the sub-nanosecond regime in typical memory structures.

Figs. 6a and 6b illustrate respectively in plan view and in cross section taken along line A-A in fig. 6a a memory device structure which is quite similar in many respects to those shown in figs. 1 and 2, but where the twin electrodes b_m , c_m are excited in a different way during readout of data. Correspondingly, there are certain physical differences in the overall structure, and in the encoding (writing) and reading of data. The volume or gap β_n between the twin electrodes b_m , c_m is now filled with a material which in addition to being electrically insulating and non-piezoelectric adheres well to both of the twin electrodes, keeping them at a fixed distance from each other. Poling of the subcells α_{n1} and α_{n2} of a memory cell 1 at each electrode a_n , a_{n+1} , a_{n+2} , ... proceeds as shown in figs.7, in analogy with the coordinated voltage

protocols mentioned below with reference to figs. 7 in connection with figs. 3 and 4.

Figs. 7a-7d show how subcells α_{n1} and α_{n2} of a memory cell 1 can be poled with mutually opposite poling directions relative to the opposing twin electrode. The plan view of fig. 7a and the corresponding matrix arrangement in fig. 7b show the poling of subcell α_{n1} in a memory cell 1 indicated by the stitched outline, while similarly figs. 7c and 7d show the poling of a subcell α_{n2} in the same arrangement. Since there is no longer any need for or danger of polarizing any ferroelectric material in the volume β_n , this is now possible, even in a passive matrix and with non-selected subcells not being exposed to disturb voltages exceeding $v_p/3$. Thus, in principle all 4 permutations of poling alternatives in the two cells α_{n1} and α_{n2} can be realized.

Figs. 8a-8d show readout of data from a memory cell 1 in the arrangement as shown in figs. 6 and 7. Figs. 8a and 8c show a portion of the apparatus according to the invention the memory in plan view, while figs. 8b and 8d show the respective cross sections thereof taken along the lines A-A of figs. 8a and 8c. Again the location of a memory cell 1 with subcells $\alpha_n, \dots, \beta_n$ is indicated by a stitched outline. As shown, subcells $\alpha_n - \alpha_{n+5}$ adjoining the electrodes $a_n - a_{n+5}$ have been poled such that when a voltage is applied between these electrodes and the twin electrodes b_m, c_m , a net force is exerted upon the twin electrodes b_m, c_m , pulling/pushing them to one side. Applying a sinusoidal voltage causes a right-left vibration of the twin electrodes b_m, c_m as a unit, as shown in figs. 8a and 8b at two points in time. Clearly, the number and positions of driver units such as those on electrodes a_n and a_{n+5} can be selected in each specific case, to achieve adequate overall excitation of the twin electrodes b_m, c_m without sacrificing too much memory capacity. In fig. 8a the memory cells 1 on electrodes a_{n+2}, a_{n+3} and a_{n+4} are encoded with data that yield a response $+V, -V$ and $0 V$, respectively, at that point in the excitation cycle. The voltages are generated piezoelectrically, and the discussion on different modes of excitation connection with fig. 5 above also applies here. One notes that the option of multibit encoding in the present case to a certain extent mitigates the disadvantage of using α_{n1} and α_{n2} cells for excitation purposes.

Not shown in the above-referred figures is how a layer of insulating material may be applied to seal and protect the memory cells and ancillary circuitry.

In practice, the material on top of the moving parts of the overall device must be selected and applied so as to avoid unduly damping or inhibiting the motion. In addition, an electrically conducting layer may be applied on top of the insulating layer, to provide electrical shielding against noise and pick-up.

5 In cases where it is desired to build stacked structures on top of the first layer as described here, it may be required to include planarizing procedures and materials between layers in a stack, etc. This is considered obvious to persons skilled in the art, and shall not be discussed further here.

10 As is apparent from the above, the present invention provides new opportunities for building densely arrayed piezoelectric microstructures that are essentially planar and compatible with multilayer stacking. The micromechanical motion takes place in a well-defined volume with precisely controlled materials and dimensions. A novel passive matrix architecture with dual electrodes provides a number of different ways of constructing
15 memory cells, as well as writing data thereto, retrieving data therefrom and once more writing new data thereto. Extensions and variants of those exhibited here as the herein above-disclosed preferred embodiments would be obvious to persons skilled in the art, and shall be claimed as included in the present patent application.

20 The present invention provides a passive matrix-addressable array of memory cells which in its overall aspects already is known from the prior art devices, wherein a layer of memory material, e.g. of ferroelectric polymer, is sandwiched between a first electrode layer with parallel strip-like electrodes and a second layer of parallel strip-like electrodes, but oriented orthogonally
25 to the electrodes of the first set, whereby any memory cell in the array can be uniquely addressed for a write/read operation. A very high storage density can be obtained in the prior art devices as the device thickness may be a fraction of a micrometer and the electrodes provided in a dense arrangement and with an obtainable memory cell pitch approaching the line width or
30 minimum feature size that can be provided by the resolution presently offered by photolithographic and etching techniques used for patterning the electrodes. The memory layer is of course laid down as a global and continuous layer in the device and needs no patterning. The implication of a memory cell size and the memory cell pitch that may approach the minimum
35 feature size as obtainable with present photomicro lithographic and etching

techniques, offers the possibility of an area storage density of about 25 bit/ μm^2 or even more, with one bit per memory cell.

In the present invention the trench 3 must in order to accommodate the twin electrodes *b*, *c* provided therein and patterned with the conventional
5 technologies, have a width at least twice that of a minimum feature size as provided by available design rules. As in the case of the prior art, however, the electrodes in the present invention all can be provided in a so-called dense arrangement, see for instance PCT/NO02/00414, and the distance
10 between the parallel neighbour trenches which are oriented orthogonally to the electrodes *a* can in practice be made very small, as it is envisaged that also the trenches 3 can be provided in a dense arrangement. This would, however, still imply that the area storage density in the apparatus according to the invention would be less than one half of that achievable with prior art memory devices with dense electrode arrangements, but one should then also
15 bear in mind that the thickness of the memory matrix in present invention shall be equal to the thickness of the electrodes *a*. In other words, all functional parts of the apparatus of the present invention is contained within the electrode layer that constitutes the electrodes *a*, and this contrasts with prior art sandwich structures where the memory matrix consists of three
20 consecutive stacked layers, as mentioned above. This offers the possibility of the apparatus according to the present invention providing an improved volumetric storage density, i.e. the number of memory cells or bits stored per volume unit would be comparable to that of the prior art technologies and could be further improved by resorting to multibit coding, if that is
25 implemented in present invention. It should also be noted that the apparatus according to the present invention, i.e. the memory matrix, could be used to form a volumetric data storage apparatus similar to the volumetric devices known in the prior art, by stacking the inventive memory matrices on the top of each other, as the displacements or motions of the electrodes *b*, *c* take
30 place laterally, i.e. in a horizontal direction, and the stress vectors in the memory material have the same direction. Thus no vertical up-down movements occur and memory matrices of the stack are not detrimentally disturbed by the piezoelectric activation of the memory cell of a particular memory matrix or device in the stack. – The general concept of stacking is
35 well-known in prior art technology and shall hence not be further discussed here.

In addition of course, the present invention achieves the added benefit that the reliance of piezoelectric properties of the ferroelectric memory material shall provide for a shorter access time and a significantly improved signal/noise ratio as compared with the prior art ferroelectric or electret matrix memories based on ferroelectric or electret polymer materials. These
5 may as noted above be the presently most preferred material, viz. poly(vinylidenedifluoride-trifluoroethylene), but need not be limited thereto or to copolymers of the same family. Other candidate materials displaying both ferroelectric and piezoelectric properties have been contemplated by the
10 applicant and include odd nylons, vinylidene-cyanide copolymers, polyurea, and polymers containing polynitride or imide groups.

CLAIMS

1. A data storage apparatus with means for storing and retrieving data in respective write and read operations, wherein data are stored in a non-volatile manner as polarization states in ferroelectric memory cells, wherein the
5 memory cells are provided in a passive matrix-addressable array, wherein the memory cells can be individually addressed electrically for write and read operations, the addressing of the memory cell taking place via crossing electrodes of a respectively first and second electrode sets, wherein each electrode set comprises parallel stripe-like electrodes such that the electrodes
10 of the first set substantially are oriented orthogonally to the electrodes of the second set,
characterized in that the first set of electrodes (*a*) comprises a plurality of parallel trenches (3) extending horizontally with an orthogonal orientation to the electrodes (*a*) and vertically downwards from a top surface thereof for a
15 distance less than the thickness of the electrodes (*a*) and having a substantially rectangular profile, that at least a ferroelectric or electret memory material (2) is provided in the trenches (3) and covering the sidewalls thereof, that the second set of electrodes is provided as a dual set of electrodes, each comprising parallel twin electrodes (*b*, *c*) provided in said
20 trenches (3) and parallel therewith and without mutual contact with the electrodes (*a*) of said first set, that the ferroelectric material (2) is provided in at least a portion of the volume of the trenches (3) not occupied by the electrodes (*b*, *c*), said ferroelectric or electret material being a soft or elastic ferroelectric or electret material with piezoelectric properties and in addition
25 providing electrical insulation between the electrodes (*b*, *c*) of the second set and the electrodes (*a*) of the first set, whereby the twin electrodes (*b*, *c*) of the second set under a suitably applied force can be displaced laterally in the soft ferroelectric or electret material (2) with piezoelectric properties such that a piezoelectric effect is generated therein, and that said soft ferroelectric
30 or electret material with piezoelectric properties in the volumes between the twin electrodes (*b*, *c*) of the second set and the electrodes (*a*) of the first set forms subcells (α_1 , α_2) of the memory cells (1) in said trenches (3), said subcells (α_1, α_2) capable of being poled for a write operation by applying an electric field between respective twin electrodes (*b*; *c*) and crossing
35 electrodes (*a*) of the first set, such that the memory cells (1) are polarized to store at least one of two or more logical values in the form of a set of

polarization states in said subcells (α_1, α_2) and can be read non-destructively by applying a voltage potential between the twin electrodes (b, c), and/or between at least one of the latter and at least one of proximal electrodes (a) of the first electrode set, and over ferroelectric or electret material of the subcells (α_1, α_2) which are subjected to tensile and/or compressive stresses enabling the detection of parameters deriving from the polarization states thereof by means of piezoelectric effects in response to strains thus induced in said subcells, whereby the logic state of the subcells (α_1, α_2) of a memory cell (1) can be found and the logical value or values stored in a memory cell (1) containing the subcells (α_1, α_2) can be determined.

2. An apparatus according to claim 1, characterized in that said soft ferroelectric or electret material (2) is a ferroelectric polymer.

3. An apparatus according to claim 1, characterized in that ferroelectric or electret material (2) and said twin electrodes (b, c) are supported by a layer on non-ferroelectric or non-electret material (4) located at bottom surface of the trench (3).

4. An apparatus according to claim 1, characterized in that the bottom layer (4) can be bonded or not bonded to other materials and structures in said trench (3) and optionally selected as an elastomer.

5. An apparatus according to claim 4, characterized in that a gap (β) between said twin electrodes (b, c) is filled with a ferroelectric or electret material (2).

6. An apparatus according to claim 4, characterized in that the gap (β) between said twin electrodes (b, c) is filled with a non-piezoelectric material (5) bonded to both.

7. Apparatus according to claim 4, characterized in that said twin electrodes (b, c) form a mechanically resonant structure, with said twin electrodes oscillating relative to each other with the gap (β) between them opening/closing.

8. An apparatus according to claim 1, characterized in that said twin electrodes (b, c) form a mechanically resonant

structure, with said twin electrodes oscillating sideways in the trench (3), the distance between them remaining constant.

9. Apparatus according to claim 1,
characterized in that one or more mechanically and/or electrically insulating
5 layers are provided over the top surface of the electrodes (*a*, *b*, *c*) and the memory cells (1).

10. A non-destructive readout method in a data storage apparatus
according to claim 1,
characterized by the readout of data being performed by subjecting the
10 subcells (α_1 , α_2) of the memory cells (1) selected for read operations to tensile and/or compressive force and concurrent detection of phase and/or polarity and/or magnitude of piezoelectrically generated voltage or current from said subcells (α_1 , α_2) in response to strains resulting from the application of said tensile and/or compressive force.

11. A method according to claim 10,
characterized by said tensile and/or compressive force being transmitted by
the motion of electrodes (*b*, *c*) that are part of the physical structure defining
a given memory cell (1).

12. A method according to claim 11,
20 characterized by said motion being parallel to the surface on which said array of memory cells (1) is supported.

13. A method according to claim 11,
characterized by said tensile and/or compressive force being generated by the
application of electric fields to poled ferroelectric or electret material
25 proximate to said electrodes (*b*, *c*).

14. A method according to claim 13,
characterized by said ferroelectric or electret material (2) being a polymer.

15. A method according to claim 14,
characterized by said ferroelectric or electret polymer (2) being the same
30 material as used in subcells (α_1 , α_2).

16. A method according to any of the claims 10,
characterized by said tensile and/or compressive force varying cyclically in
time.

17. A method according to claim 16,
characterized by detection of a thereby piezoelectrically generated voltage or
current being performed with coherent averaging or lock-in technique.

5 18. A method according to claim 10,
characterized by said tensile and/or compressive force being a single step
pulse.

19. A method according to claim 10,
characterized by said tensile and/or compressive force being a delta pulse or
burst of such pulses.

10 20. A method according to claim 11,
characterized by said electrodes (b , c) acting upon two or more memory cells
(1) simultaneously.

15 21. A method for poling pairs of subcells (α_1 , α_2) in memory cells (1) for
write operations in a data storage apparatus according to claim 1,
characterized by poling each cell (α_1 , α_2) of the pair in one of two poling
directions oriented orthogonally relative to the twin electrodes (b , c)
opposing each cell (α_1 , α_2) of the pair, whereby all four possible
permutations of the poling directions can be realized in the two cells (α_1 , α_2)
of the pair.