

PERSONAL COMPUTER WITH PROCESSOR RESET CONTROL

ABSTRACT

This invention relates to personal computers, and more particularly to personal computers in which capability is provided for continuance of processing through an occurrence of a RESET signal while avoiding systems failures. The personal computer system has a high speed local processor data bus; an input/output data bus; a resettable microprocessor coupled directly to the local processor bus; and a bus interface controller coupled directly to the local processor bus and directly to the input/output data bus for providing communications between the local processor bus and input/output data bus. The bus interface controller provides for arbitration among devices directly coupled to the input/output data bus for access to the input/output data bus and to the local processor bus and for arbitration among the input/output data bus and the microprocessor for access to the local processor bus. The bus interface controller further recognizes receipt of a reset signal intended to initiate a reset of the microprocessor and defers delivery of a reset signal to until the bus interface controller has barred access to the local processor bus and input/output bus by any of the devices potentially requesting such access.