ABSTRACT

A PILLAR PROCESS FOR COPPER INTERCONNECT SCHEME

A method for forming reliable inter-level metal interconnections in semiconductor integrated circuits is described where pillars are formed to connect between different metal layers. A first conductive layer is deposited overlying a substrate containing devices, junctions and other structures formed in previous process steps covered by an insulating layer. A conductive etch stop layer is deposited overlying the first conductive layer and then patterned to form a mask for the first conductive layer. This is followed by a deposition of via metal layer overlying the entire surface. A hard mask layer is deposited and patterned to form the mask where via pillars are to be formed. Subsequent anisotropic etching forms pillars in the via metal layer and openings in the first conductive layer. An inter-metal dielectric (IMD) layer is deposited covering and filling both the openings in the first conductive layer and in between the via pillars. The surface is then planarized. The IMD and hard mask layers are patterned and etched forming openings to the via pillars and single damascene trenches where second conductive layer lines will lie. These lines are formed by depositing the second conductive material overlying the IMD and filling the trenches followed by planarization to remove conductive material not in the trenches. Etching metal to form conductive pillars is more effective than etching small, deep via holes. The problems associated with etching via holes though the IMD and filling the holes are eliminated providing a reliable interlevel conductor connection. In addition, problems of varying IMD etch rates in areas of dense via population are not encountered. This process allows the use of copper interconnection reducing both interconnection resistance and electromigration.

Figure 5