

METHOD AND APPARATUS FOR INTERRUPT COMMUNICATION IN A PACKET-SWITCHED
COMPUTER SYSTEM

Abstract of the Disclosure

1 An apparatus and method for handling interrupt requests from any of a plurality of inter-
rupters to any of a plurality of interrupt handlers. Each interrupt handler includes an interrupt
input request queue for holding a plurality of incoming interrupt requests. A system controller is
5 connected to the interrupters and the interrupt handlers, and includes an input queue coupled to
each interrupter for receiving a plurality of interrupt requests. The system controller includes a
processor and a memory storing instructions for controlling its operation. The system controller
also includes an output queue coupled to each interrupt handler (which in many cases will also be
10 interrupters), and a counter for monitoring the current number, at any given time, of interrupt
requests pending in each of the interrupt input queues in the interrupt handlers. When an interrupt
request is sent from an interrupter, the system controller determines a target for the request, which
may be by a target ID in the request or may be based upon a predetermined method to ensure even
15 distribution of interrupt requests among all or a subset of the interrupt handlers. The system con-
troller determines whether the target interrupt handler's input queue is full, and if not then it
passes on the interrupt request and sends a positive acknowledgment to the interrupter. If the
queue is full, then a negative acknowledgment is sent, and the interrupter then waits a random
20 period of time and sends the interrupt request again. The target interrupt handler may thus accept
multiple interrupt requests and process them in order without negative acknowledgments.

(Figure 1)