

# PATENT SPECIFICATION

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## (54) INTEGRATED CIRCUIT ARRANGEMENT

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

- 10 The invention relates to a circuit arrangement comprising an electrical information input, logic gates and a conductor for supplying power to said gates, and control means for adjusting the current in said  
 15 conductor between a first value and a stand-by value in response to a control signal.

- Patent Specification 1,257,009 discloses control of a memory circuit, notably a  
 20 bistable trigger stage, between a stand-by state of low dissipation, i.e. low current consumption, and a state of high dissipation, i.e. high current consumption, when writing or reading is required to take place.  
 25 In this both fast reading and writing and low dissipation in the stand-by state can be achieved, the latter enabling lightweight batteries to be incorporated in apparatus with battery supply and excessively high temperatures to be avoided in  
 30 apparatus which is supplied from the mains.

- If information has not only to be stored but also to be processed, similar considerations apply.

- The present invention provides a circuit arrangement, comprising an integrated circuit having an electrical information input, logic gates, a conductor or conductors for  
 40 supplying power to said logic gates, and a clock for controlling said logic gates, the arrangement including control means for adjusting the current in said conductor or conductors between a first value and a  
 45 stand-by value in response to a control

signal, means being provided for adjusting the output frequency of the clock between one value and another together with the adjustment of the current in a said supply conductor between the first value and the  
 50 standby value.

When the current has its first value it may thus be arranged that operations on the information can be performed very quickly, whereas when the current has its  
 55 (lower) stand-by value such high speed operation may not be possible. (If the current were completely switched off so as to save energy rather than just reduced to its stand-by value, information might  
 60 be lost).

The stand-by current value can be arranged to occur in various situations. Thus it may be arranged to occur on occasions when the required processing  
 65 capacity of the arrangement is low or zero. As a result it may be arranged that the processing of the information is not significantly delayed, whilst a substantial amount of energy is saved. Another possibility occurs if power for the arrangement is normally derived from the mains and an emergency supply source, for example a battery, is also provided. The control signal can then be arranged to have  
 75 different values depending on whether or not the mains supply is adequate, in the latter case the battery being made to supply the stand-by current by means of the control means. In all cases the clock output frequency will vary with the current variations in the supply conductor and it can thus be automatically adapted, for example, to the achievable information processing speed in the remainder of the integrated circuit.

If desired, means may be provided for blocking the clock output when the current in the supply conductor or conductors has the stand-by value the effective value  
 90

of the output frequency of the clock then being zero. It may thus be arranged that no information is processed at the stand-by current value, but only at the first value.

5 A detector such as a simple differentiating element may be provided for changes in current in said conductor or conductors to said stand-by value, the output of said detector being coupled to means for blocking the clock output. This detector may respond to changes in said current directly, to changes in said control signal or in any other quantity, or to the attainment of a given amount of charge. It can effect the blocking of the clock output for a fixed period of time or for the period during which the stand-by value is maintained. The adjustment of the clock output frequency to zero in the standby state can facilitate the use of components with larger tolerances; a clock frequency which is substantially constant when present can be very advantageous in this respect.

Preferably a said conductor is connected to a bias current input of a current injector for said gates, and preferably also to a bias current input of a current injector for a gate which is included in the frequency-determining part of said clock. A "current injector" is to be understood to mean a multilayer structure comprising at least three successive layers, which are separated from each other by rectifying junctions, including a first (injecting) layer, which is provided with a bias current input and is separated from the circuit element to be supplied with current by at least one rectifying junction, an adjoining (intermediate) second layer of semiconductor material which is also provided with a bias current input so that connection of a bias current source between the bias current inputs in such a sense as to forward bias the junction between the injecting and intermediate layers will cause charge carriers to be injected into the intermediate layer by the injecting layer, so causing collection of charge carriers by a subsequent (collecting) layer of said successive layers of the current injector via a rectifying junction which said collecting layer forms with an adjacent layer of the current injector, a zone of the circuit element to be supplied with current belonging to said collecting layer.

A structure of this kind has become known as "integrated injection logic", and is described in Patent Specifications 1,398,862/3/4/5/6/7/8. It can have a simple construction and can be substantially devoid of adjusting resistors. A large number of gates can be supplied with current by identical current injectors, with the result that the injected currents and hence the switching times can be made accurately

the same. The control means for such an arrangement can often consist of a single resistor in parallel with a transistor.

An embodiment of the invention will be described by way of example, with reference to the accompanying diagrammatic drawing in which Figure 1 is a diagram of a pocket calculator; Figure 2 is a section through a semiconductor structure constructed according to the integrated injection logic principle; Figures 3 and 4 show examples of gates constructed by integrated injection logic; and Figure 5 is a block diagram of a clock constructed by integrated injection logic.

Figure 1 is a block diagram of a pocket calculator (being an example of apparatus in which an integrated circuit is provided comprising information inputs, logic gates, a clock for controlling the gates, and an associated power supply). The arithmetical operations taking place in the calculator may be completely standard and will not be described here-in. The calculator comprises a housing (not shown), a keyboard KB, a display unit DP, control means SW, an amplifier A, and an energy source POW which comprises, for example, an exchangeable battery. The calculator also includes a detector DT, a decoder DC and an arithmetic unit ARI, which are constructed as one or more integrated circuits.

The energy source POW includes a switch which is not shown. If this switch is in the "on" position the display unit DP is actuated; this unit may comprise six positions at which a number can be displayed by means of liquid crystal material. The control means SW, and hence the decoder DC and the arithmetic unit ARI, are initially controlled so that DC and ARI consume only a stand-by current which reaches them via the lines 1 and 3, respectively. As a result, the processing speed is substantially limited in the two components DC and ARI. When a key of the key-board KB is depressed, however, the decoder DC receives a signal therefrom via a multiple cable, and the depression is also signalled by the detector DT. This signal is applied via amplifier A as a first signal to control means SW, with the result that decoder DC and arithmetic unit ARI consume a higher current which reaches them via the lines 2 and 4, respectively. Consequently, the achievable decoding and calculating speeds are then high. The information fed in by the key is decoded; if the key is a digit key the information is stored in a register in the arithmetic unit ARI and is displayed on the display unit DP; if it is a function key the calculation is performed and the result thereof is stored in a register and

displayed. The first signal may be supplied to the control means SW by the amplifier A for example, 0.5 second. The time for which this signal is applied may be arranged to be the maximum time required for an arithmetical operation. As an alternative however, the application of the first signal to the control means may be terminated by a signal from the arithmetic unit ARI itself, which signal may be triggered by a change in the display. For example, it may be that the depression of each key results eventually in a change in the number displayed, or because the result of the calculation is displayed. When this occurs the current is reduced to the stand-by value.

In practice the power consumption of the display unit DP may be 3 mA as long as the switch is in position "on". The entire remainder of the circuit may consume 20 mA in its high-current state and 2mA in its stand-by current state. During normal calculation at the most one arithmetic operation may be started every ten seconds and may last less than  $\frac{1}{10}$  second on the average. It will be seen therefore that the additional current consumption in excess of the stand-by value will then be negligible, even if the time for which each high-current state lasts is fixed at 0.5 second.

The depression of a key can be detected directly, for example by causing the depression to be signalled by an interrogation unit (not shown). As an alternative the receipt of information by decoder DC when in the stand-by current range can be detected. As a further alternative the information may be arranged to arrive as a flow of bits from a conductor in such a form that each signal is preceded by a "1"-pulse of very long duration. This "1"-pulse will change the current pattern in the circuit, which can be detected by a current detector. The detector output signal can be fed to amplifier A. If amplifier A is included in a positive feedback loop and the loop amplification exceeds 1, the amplifier A will become saturated and cause the control means to control the current to the higher value. If desired it may be arranged that depression of not all the keys give rise to the higher current value. If a digit key or an "erase" key, or a decimal point key is depressed, not much activity is required of the calculator. This also applies, but to a lesser extent, to adding and subtracting. On the other hand an extensive calculating program is required for multiplication, division, root extraction and the like. Thus it may be arranged that the current is set to the higher value only in response to depression of certain keys.

If desired the control means may be arranged to control the current to three

or more discrete values.

The arithmetic unit ARI includes a clock Cl which synchronizes the operations of the remainder of the unit, which clock has the same power supply, and the output frequency of which varies with the current supply thereto. As a result, the clock frequency is automatically adapted to the processing speed which can be achieved in the remainder of the unit. An example of such a clock and its use will be described hereinafter.

The elements DT, DC, ARI A and SW may be in combined integrated form. As an alternative, however, a plurality of chips can be used, even for those elements which are shown as one unit. The arrangement may also comprise non-integrated elements such as output amplifiers, switches and the like.

Figure 2 is a sectional view through a semiconductor structure intended to operate according to the integrated injection logic (I<sup>2</sup>L) principle. The structure consists of six layers which are manufactured by techniques which are conventional in integrated circuit technology. Five of these layers are provided with connectors which are denoted by heavy lines. Layer 1 is of p-type semiconductor material, is connected to a supply source, and constitutes an injecting layer. Layer 3 is of n-type semiconductor material and is connected to ground. This layer constitutes an intermediate layer into which charge carriers are injected by the injecting layer. This hole current is dependent on the supply voltage applied to the layer 1 (and also on the physical conditions such as the impurity concentration in the material and the temperature). Layer 6 is of n-type semiconductor material of a higher n-concentration than layer 3. This thicker layer acts as a mechanical reinforcement. Layer 2 is of p-type semiconductor material and constitutes a collecting layer for the holes injected into layer 3 by layer 1. The assembly of the layers 1, 3 and 2 constitutes a three-layer current injector, and has a so called lateral structure: the three layers are arranged beside each other. If layer 2 is allowed to float it will become positively charged and will also inject a hole current into layer 3, which current will increase as the forward potential of layer 2 increases. Layer 1 and layer 2 are deposited together, so that their physical properties are substantially the same. Because they are also arranged close together, their temperatures are also the same. On the one hand, the combination of layer 1 and layer 3 can be considered as a current source having a high internal resistance (current substantially constant). On the other hand, the

current which actually flows in the direction  $1 \rightarrow 3 \rightarrow 2$  depends on the potential of layer 2. If this potential is high, this current is small, whereas if the potential of layer 2 is low, the current in the direction  $1 \rightarrow 3 \rightarrow 2$  is large.

Layers 4 and 5 are of n-type semiconductor material and constitute two collectors of a multi-collector npn transistor which is formed by the layers 3 - 2 - 4 (5). If the potential of layer 2 is high, so that the current in the direction  $2 \rightarrow 3$  is large (current in the direction  $1 \rightarrow 3 \rightarrow 2$  small), this transistor is conducting and current can be conducted through the layers 4 and/or 5. On the other hand, if the potential of layer 2 is made low by draining current from it via an external circuit (current in the direction  $1 \rightarrow 3 \rightarrow 2$  large) the multi-collector transistor will be cut off. Thus a current-controlled current logic (I<sup>2</sup>L) arises. It will be noted that the current injector structure should not be considered as a pnp-transistor, because only the currents therein are of importance and not the voltages.

Two logic states can be defined:

- a) no current drained externally from 2, in which case currents flow in the directions  $1 \rightarrow 3$  and  $4(5) \rightarrow 2 \rightarrow 3$
- b) current drained externally from 2, in which case current flows in the direction  $1 \rightarrow 3 \rightarrow 2$  only.

A current drain can be arbitrarily defined as a logic "1".

This example of integrated injection logic is only one of many which are possible. Many others are described in the said Patent Specifications 1,398,862/3/4/5/6/7/8. For example, the current injector (layers 1 - 3 - 2) can be constructed as a vertical structure, and the multi-collector transistor (layers 3 - 2 - 4/5) as a lateral structure.

Figure 3 shows a gate which is constructed in integrated injection logic i.e. the same gate as that shown in Figure 2, but now represented symbolically. Transistor T1 is composed of the layers 3, 2 and 4/5 of Figure 2, and current source S1, having a supply connection K0, is composed of the layers 1 and 3 of Figure 2. Terminal K1 constitutes a signal input and the collectors of transistor T1 form signal outputs. The transistor can have two logic states:

- a) Current is taken from terminal K1 by an external circuit, in which case the paths between the emitter and the collector electrodes of transistor T1 are effectively open circuit,
- b) no current is taken from K1, in which case the paths between the emitter and the collector electrodes of transistor T1 conduct.

If the current-carrying property of an

external connection between K1 and earth, and of the internal collector-emitter paths of T1 are defined as logic "1", the circuit of Figure 3 constitutes a logic NOT-gate having two outputs.

Figure 4 shows a circuit comprising three transistors T1, T2, T3, corresponding to transistor T1 of Figure 3, and three signal terminals K1, K2, K3. Connected to the bases of these transistors are current sources S1, S2, S3 respectively each of which always supplies the same current, the construction of each source being identical to that shown at 1, 3 in Figure 2.

If the output current of S1 is taken from terminal K1 by an external connection (logic 1), transistor T1 is not conducting. Similarly, if the corresponding current is taken from terminal K2, transistor T2 is not conducting. If the output current of current source S3 passes to ground via the emitter electrode of transistor T3 (rather than through the collector-emitter path of transistor T1 or T2, terminal K3 is connected to earth in a conducting manner through the collector-emitter of transistor T3. This occurs only if current is taken externally from both K1 and K2, because otherwise the current from S3 will be taken by the collector-emitter paths of T1 or T2. If the current-carrying state of a connection is defined as logic "1", the arrangement of Figure 4 is therefore a logic AND-gate. Similarly, if the galvanic connection between the collector electrodes of the transistors T1 and T2 and the base-electrode of transistor T3 is taken as the circuit output the circuit becomes a logic NAND-gate. If the output signal of a gate has to be fed to more than one location, a different collector electrode of the corresponding transistor should preferably be used for each. Otherwise different collector currents might occur in different gates with the result that different switching times might occur. However, it may be that this phenomenon can be used to good advantage in certain circuits.

Figure 5 is a block diagram of the clock C1 of Figure 1. This is constructed from integrated injection logic elements and consists of an odd number (in this case 5) of logic gates T5 . . . T9 each corresponding to Figure 3. The base electrode of each gate (denoted by a circle) is connected to a collector electrode of a preceding gate. The circuit is astable and the gate switch each time after the same delay. A symmetrical output signal thus appears on terminal K4.

If this clock is included in a circuit the remainder of which (for example the remainder of ARI in Figure 1) is constructed from similar integrated injection logic elements (same temperature and composition)

and is fed from the same supply voltage, the clock frequency can be made to automatically adapt to voltage and temperature variations. In certain circumstances it may be necessary to stop the clock, for example by means of an additional blocking gate in the loop containing T5 . . . T9 or in the output line connected to terminal K4. These blocking gates can be unblocked when the supply current is sufficiently large, or when it is sufficiently constant. A special detector of known construction can be added to the circuit of Figure 1 for this purpose. Furthermore, it can be arranged that any bistable and polystable elements such as counters incorporated in the circuit are reset to a starting position when the clock is stopped, to predetermine the starting condition thereof when the supply of clock pulses is restored.

An arrangement according to the invention may also be used, for example, in portable "key-to-tape" equipment, space satellites processing digital signals, sealed error-correction devices in submarine data transport cables, and other devices in which dissipation reduction and energy savings are desirable.

WHAT WE CLAIM IS:—

1. A circuit arrangement, comprising an integrated circuit having an electrical information input, logic gates, a conductor or conductors for supplying power to said logic gates, and a clock for controlling said logic gates, the arrangement including control means for adjusting the current in said conductor or conductors between a first value and a stand-by value in response to a control signal, means being provided

for adjusting the output frequency of the clock between one value and another together with the adjustment of the current in a said supply conductor between the first value and the stand-by value.

2. An arrangement as claimed in Claim 1, wherein the clock is constructed so that its frequency will vary with variations in supply current thereto, a said conductor being connected to a current supply input of said clock.

3. An arrangement as claimed in Claim 1 or Claim 2, wherein the other value of the output frequency of the clock is zero.

4. An arrangement as claimed in Claim 3, including a detector for changes of current in said conductor or conductors to said stand-by value, the output of said detector being coupled to means for blocking the clock output.

5. An arrangement as claimed in any preceding Claim, wherein a said conductor is connected to an input of a current injector (as herein defined) for said gates.

6. An arrangement as claimed in Claim 5, wherein said conductor is connected to an input of a current injector (as herein defined) for a gate which is included in the frequency determining part of said clock.

7. A circuit arrangement as claimed in Claim 1, substantially as herein described with reference to the accompanying diagrammatic drawings.

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