

ABSTRACT

A semiconductor device includes a substrate including an active region defined by a device isolation layer. A word line structure is in a trench formed in an upper portion of the substrate. The word line structure includes a gate insulation pattern covering an inner surface of the trench. A gate electrode pattern is on the gate insulation pattern. A first work function pattern is between the gate insulation pattern and the gate electrode pattern. A second work function pattern is on the first work function pattern and extends along a side surface of the gate electrode pattern. The first work function pattern has a top surface at a level below that of a bottom surface of the gate electrode pattern. The first work function pattern has a work function greater than that of the second work function pattern.

FIG. 2