Claims

What is claimed is:

1. A miniature passive structure for electrostatic discharge protection and input/output matching for a high frequency integrated circuit, the structure comprising:

a transmission line for providing at least one electrostatic discharge path; and

a capacitor with a first end connected to the transmission line and a second end connected to ground;

wherein the transmission line comprises at least one of a high impedance loaded transmission line or an unloaded transmission line.

2. The miniature passive structure of claim 1,

wherein the transmission line comprises a length of about 1/4 wavelength.

3. The miniature passive structure of claim 1 or 2, further comprising:

an input signal trace, wherein the transmission line is DC connected to the input signal trace at a first end and DC connected to the capacitor at a second end.

4. The miniature passive structure of claim 1 or 2, further comprising:

an input signal trace, wherein the transmission line is DC connected to the input signal trace at a first end and AC coupled or DC connected to a supply rail at a second end.

~~5. The miniature passive structure of any one of claims 1 to 4,~~

~~wherein the transmission line comprises at least one of a high impedance loaded transmission line or an unloaded transmission line.~~

~~6. The miniature passive structure of any one of claims 1 to 4,~~

~~wherein the transmission line comprises a high impedance transmission line;~~

~~wherein the high impedance transmission line comprises at least one of (i) a coplanar waveguide, (ii) a conductor backed coplanar waveguide, (iii) coax transmission lines, (iv) a microstrip line, or (v) a stripline.~~

~~7. A miniature passive structure for electrostatic discharge protection and input/output matching for a high frequency integrated circuit, the structure comprising:~~

~~an inductor for providing at least one electrostatic discharge path; and~~

~~a capacitor with a first end connected to the inductor and a second end connected to ground.~~

~~8. The miniature passive structure of claim 7,~~

~~wherein the inductor comprises at least one of a single ended inductor, a multilayer stacked inductor, a differential symmetrical inductor or an inductor proposed by IC foundry.~~

~~9. The miniature passive structure of claim 7 or 8, further comprising:~~

~~an input signal trace, wherein the inductor is DC connected to the input signal trace at a first end and DC connected to the capacitor at a second end.~~

~~10. The miniature passive structure of claim 7 or 8, further comprising:~~

~~an input signal trace, wherein the inductor is DC connected to the input signal trace at a first end and AC coupled or DC connected to a supply rail at a second end.~~

5~~11~~. A high frequency electrostatic discharge protection network for integrated circuits comprising:

a high frequency signal carrying transmission line; and

one or more miniature passive structures, each of the one or more miniature passive structures comprising:

a transmission line for providing a corresponding at least one electrostatic discharge path; and

a capacitor with a first end connected to the transmission line and a second end connected to ground;

wherein the integrated circuits are based on an integrated circuit technology selected from the group consisting of CMOS, GaAs, SiGe, and InP; and

wherein the transmission line comprises at least one of a high impedance loaded transmission line or an unloaded transmission line.

612. The high frequency electrostatic discharge protection network of claim 511,

wherein the high frequency electrostatic discharge protection network is coupled to core circuits of the integrated circuits by capacitive coupling selected from the group consisting of capacitor coupling and coupled transmission line coupling for one or more of protection of the core circuits and DC bias of the core circuits.

713. The high frequency electrostatic discharge protection network of claim 511 or 612,

wherein the high frequency electrostatic discharge protection network is coupled to core circuits of the integrated circuits by direct connection for protection of the core circuits.

814. The high frequency electrostatic discharge protection network of any one of claims 511 to 713,

wherein a differential configuration of the high frequency electrostatic discharge protection network provides electrostatic discharge protection for differential input/output ports.

9~~15~~. The high frequency electrostatic discharge protection network of any one of claims 5~~11~~ to 8~~14~~, further comprising:

a plurality of electrostatic discharge paths wherein cascading of the high frequency electrostatic discharge protection network distributes electrostatic discharge current into multiple ones of the plurality of electrostatic discharge paths.

10~~6~~. The high frequency electrostatic discharge protection network of any one of claims 5~~11~~ to 9~~15~~,

wherein the high frequency electrostatic discharge protection network acts as an element in an input/output matching network.

~~17. A high frequency electrostatic discharge protection network for integrated circuits comprising:~~

~~a high frequency signal carrying transmission line; and~~

~~one or more miniature passive structures, each of the one or more miniature passive structures comprising:~~

~~an inductor for providing a corresponding at least one electrostatic discharge path; and~~

~~a capacitor with a first end connected to the inductor and a second end connected to ground;~~

~~wherein the integrated circuits are based on an integrated circuit technology selected from the group consisting of CMOS, GaAs, SiGe, and InP.~~

~~18. The high frequency electrostatic discharge protection network of claim 17, wherein the high frequency electrostatic discharge protection network is coupled to core circuits of the integrated circuits by capacitive coupling selected from the group consisting of capacitor coupling and coupled transmission line coupling for one or more of protection of the core circuits and DC bias of the core circuits.~~

~~19. The high frequency electrostatic discharge protection network of claim 17 or 18, wherein the high frequency electrostatic discharge protection network is coupled to core circuits of the integrated circuits by direct connection for protection of the core circuits.~~

~~20. The high frequency electrostatic discharge protection network of any one of claims 17 to 19, wherein a differential configuration of the high frequency electrostatic discharge protection network provides electrostatic discharge protection for differential input/output ports.~~

~~21. The high frequency electrostatic discharge protection network of any one of claims 17 to 20, further comprising: a plurality of electrostatic discharge paths wherein cascading of the high frequency electrostatic discharge protection network distributes electrostatic~~

~~discharge current into multiple ones of the plurality of electrostatic discharge paths.~~

~~22. The high frequency electrostatic discharge protection network of any one of claims 17 to 21,~~

~~wherein the high frequency electrostatic discharge protection network acts as an element in an input/output matching network.~~

11~~23~~. A high frequency electrostatic discharge protection scheme for integrated circuits comprising:

power supply rails;

a supply clamp, providing transient clamping of the electrical potential difference between the power supply rails; and

a high frequency electrostatic discharge protection network comprising:

a transmission line for providing at least one electrostatic discharge path; and

a capacitor with a first end connected to the transmission line and a second end connected to ground,~~.~~

wherein the transmission line comprises at least one of a high impedance loaded transmission line or an unloaded transmission line.

12~~24~~. The high frequency electrostatic discharge protection scheme of claim 11~~23~~, further comprising an input/output (I/O) pin, and wherein the power supply rails comprise a positive power supply rail and a negative power supply rail, and

wherein the high frequency electrostatic discharge protection scheme provides electrostatic discharge stress for the integrated circuits, the electrostatic discharge stress selected from the group consisting of (a) positive electrostatic discharge stress at the I/O pin with reference to the negative power supply rail, (b) negative electrostatic discharge stress at the I/O pin with reference to the negative power supply rail, (c) positive electrostatic discharge stress at the I/O pin with reference to the positive power supply rail, (d) negative electrostatic discharge stress at the I/O pin with reference to the positive power supply rail, (e) positive electrostatic discharge stress at the positive power supply rail with reference to the negative power supply rail, and (f) negative electrostatic discharge stress at the positive power supply rail with reference to the negative power supply rail.

~~25. A high frequency electrostatic discharge protection scheme for integrated circuits comprising:~~

~~power supply rails;~~

~~a supply clamp, providing transient clamping of the electrical potential difference between the power supply rails; and~~

~~a high frequency electrostatic discharge protection network comprising:~~

~~an inductor for providing at least one electrostatic discharge path; and~~

~~a capacitor with a first end connected to the inductor and a second end connected to ground.~~

~~26. The high frequency electrostatic discharge protection scheme of claim 25,~~

further comprising an input/output (I/O) pin, and wherein the power supply rails comprise a positive power supply rail and a negative power supply rail, and wherein the high frequency electrostatic discharge protection scheme provides electrostatic discharge stress for the integrated circuits, the electrostatic discharge stress selected from the group consisting of (a) positive electrostatic discharge stress at the I/O pin with reference to the negative power supply rail, (b) negative electrostatic discharge stress at the I/O pin with reference to the negative power supply rail, (c) positive electrostatic discharge stress at the I/O pin with reference to the positive power supply rail, (d) negative electrostatic discharge stress at the I/O pin with reference to the positive power supply rail, (e) positive electrostatic discharge stress at the positive power supply rail with reference to the negative power supply rail, and (f) negative electrostatic discharge stress at the positive power supply rail with reference to the negative power supply rail.