1. A pixel acquisition circuit of an optical flow sensor, comprising:

a photodetection unit operative to output a first electrical signal responding to the incident light intensity in real time;

a signal detection unit with its input terminal coupled with the output terminal of the photodetection unit, and operative to output a first trigger signal when detecting that the first electrical signal meets predetermined trigger conditions;

an OR logic unit with its input terminal coupled with both the output terminal of the signal detection unit and a global trigger signal line of the optical flow sensor, and operative to output an acquisition instruction signal when receiving the first trigger signal or a global trigger signal from the global trigger signal line;

an acquisition control unit with its input terminal coupled with the output terminal of the OR logic unit, and operative to output and keep an activation signal when receiving the acquisition instruction signal;

a sample and hold unit with its first input terminal coupled with the output terminal of the photodetection unit, its second input terminal coupled with a time signal line, and its third input terminal coupled with the output terminal of the acquisition control unit, and operative to receive the activation signal, and sample and buffer the first electrical signal and/or time signal at the moment of the receiving of the activation signal; and

a signal output unit being coupled with both the acquisition control unit and the sample and hold unit, and operative to buffer and output the activation signal and the first electrical signal and/or time signal most recently sampled by the sample and hold unit.

2. The pixel acquisition circuit as claimed in claim 1, wherein, said acquisition control unit is connected with a reset signal line, and operative to revoke said activation signal when receiving a reset signal from the reset signal line.

3. The pixel acquisition circuit as claimed in claim 1, wherein, said time signal line is operative to transmit a periodic signal waveform to said sample and hold unit;

the time signal sampled by said sample and hold unit is the amplitude signal of that periodic signal waveform at the present acquisition instant in time.

4. The pixel acquisition circuit as claimed in claim 1, wherein, said photodetection unit comprises:

a photodiode (PD_1) with its anode grounded;

a first transistor (T_1) with its source connected with the cathode of the photodiode (PD_1) and its drain and gate connected to the power supply (VDD).

5. The pixel acquisition circuit as claimed in claim 1, wherein, said photodetection

unit comprises:

a photodiode (PD_1) with its anode grounded;

a first transistor (T_1) with its source connected with the cathode of the photodiode (PD_1) and its drain connected with the power supply (VDD);

a first amplifier (A_1) connected between the cathode of the photodiode (PD_1) and the gate of the first transistor (T_1).

6. The pixel acquisition circuit as claimed in claim 1, wherein, said photodetection unit comprises:

a photodiode (PD_1) with its anode grounded;

N transistors connected in series, wherein, $N \geq 2$, the source of the 1st transistor is connected with the cathode of the photodiode (PD_1), the drain of the Nth transistor is connected to the power supply (VDD), each transistor has its gate and drain connected together, and the source of each of the 2nd to the Nth transistors is connected to the drain of the previous transistor.

7. The pixel acquisition circuit as claimed in claim 1, wherein, said photodetection unit comprises:

a photodiode (PD_1) with its anode grounded;

N transistors connected in series, wherein, $N \geq 2$, the source of the 1st transistor is connected with the cathode of the photodiode (PD_1), the drain of the Nth transistor is connected to the power supply (VDD), the source of each of the 2nd to the Nth transistors is connected to the drain of the previous transistor, and each of the 2nd to the Nth transistors has its gate and drain connected together;

a first amplifier (A_1) connected between the cathode of the photodiode (PD_1) and the gate of the 1st transistor.

8. The pixel acquisition circuit as claimed in claim 1, wherein, said signal detection unit comprises:

a signal processing module operative to perform a high-pass filtering process on said first electrical signal in order to obtain a corresponding second electrical signal;

a threshold comparison module operative to output said first trigger signal when determining that the second electrical signal is greater than a first threshold or less than a second threshold.

9. The pixel acquisition circuit as claimed in claim 1, wherein, said signal detection unit comprises:

a signal processing module operative to perform an amplification process and a

high-pass filtering process on said first electrical signal in order to obtain a corresponding second electrical signal;

a threshold comparison module operative to output said first trigger signal when determining that the second electrical signal is greater than a first threshold or less than a second threshold.

10. The pixel acquisition circuit as claimed in claim 9, wherein, said signal processing module comprises:

a second amplifier (A_2) with its positive input electrode connected to the output terminal of said photodetection unit and its negative input electrode connected with a first resistor (R_1) which acts as a pull-down resistor, with a second resistor (R_2) connected between its output terminal and negative input electrode, and operative to perform said amplification process on the first electrical signal output by said photodetection unit;

a high-pass filter connected to that second amplifier (A_2), and operative to filter out the signal component below a frequency threshold in the amplified first electrical signal, so as to output said second electrical signal.

11. The pixel acquisition circuit as claimed in claim 9, wherein, said signal processing module comprises:

a first capacitor (C_1) with its first terminal connected with the output terminal of said photodetection unit;

a second amplifier (A_2) with its positive input electrode connected to a fixed potential and its negative input electrode connected with the second terminal of the first capacitor (C_1);

a second capacitor (C_2), a third resistor (R_3), and a first switch (K_1) all connected in parallel across the negative input electrode and output terminal of the second amplifier (A_2),

wherein, while said reset signal line holds the reset signal, the first switch (K_1) is closed.

12. The pixel acquisition circuit as claimed in claim 11, wherein, said third resistor is an adjustable resistor.

13. The pixel acquisition circuit as claimed in claim 9, wherein, said signal processing module comprises:

a second amplifier (A_2) with its positive input electrode connected with the output terminal of said photodetection unit;

a first capacitor (C_1) with its first terminal connected with the negative input

electrode of the second amplifier (A_2) and its second terminal connected to a fixed potential;

a first switch (K_1) connected between the first terminal of the first capacitor (C_1) and the output terminal of said photodetection unit; and

a high-pass filter connected to that second amplifier (A_2), and operative to filter out the signal component below a predetermined frequency threshold in the amplified first electrical signal, so as to generate said second electrical signal,

wherein, while said reset signal line holds the reset signal, the first switch (K_1) is switched on.

14. The pixel acquisition circuit as claimed in claim 9, wherein, said signal processing module comprises:

a first capacitor (C_1) with its first terminal connected with the output terminal of said photodetection unit;

a current replicator (P_1) with its first terminal connected with the second terminal of the first capacitor (C_1);

a second amplifier (A_2) with its input positive electrode connected to a fixed potential and its input negative electrode connected with the second terminal of the current replicator (P_1);

a second capacitor (C_2), a first switch (K_1), and a third resistor (R_3) all connected in parallel between the negative input electrode and output terminal of the second amplifier (A_2),

wherein, while said reset signal line holds the reset signal, the first switch (K_1) is switched on.

15. The pixel acquisition circuit as claimed in claim 8, wherein, said threshold comparison module comprises:

a first voltage comparator (VC_1) with its inverting input terminal connected with the signal line providing said first threshold and its non-inverting input terminal connected to the output terminal of said signal processing module.

16. An optical flow sensor, comprising:

a pixel acquisition circuit array comprising a plurality of pixel acquisition circuits as claimed in claim 15;

a waveform generator operative to output a periodic signal waveform to the time signal line coupled with each of the pixel acquisition circuits in the array;

a global control unit operative to output said global activation signal to each pixel

acquisition circuit through the global trigger signal line, and output a reset signal to each pixel acquisition circuit through said reset signal line;

a readout unit operative to read the signals output by at least a part of the pixel acquisition circuits in that array.

17. The optical flow sensor as claimed in claim 16, wherein, said global control unit is operative to:

configure the operation mode of said pixel acquisition circuit array in each sampling time period, that operation mode including optical flow mode and image mode;

when the current sampling time period is configured in image mode, output said reset signal and said global trigger signal in that sampling time period in sequence, in order for that pixel acquisition circuit array to be globally activated and for the first electrical signal of each pixel acquisition circuit to be read by said readout unit;

when the current sampling time period is configured in optical flow mode, output said reset signal at the starting point of time of that sampling time period, in order for the time signal to be acquired by the pixel acquisition circuits meeting said predetermined trigger conditions and to be read by said readout unit.

18. The optical flow sensor as claimed in claim 16, wherein, said readout unit comprises:

a row scanner;

a column scanner;

a readout controller operative to instruct the row scanner to select one row of pixel acquisition circuits in sequence,

and when one row is selected by the row scanner, instruct the column scanner to read the signals output by at least a part of the pixel acquisition circuits in that row one by one.

19. The optical flow sensor as claimed in claim 16, wherein, said readout unit comprises:

a row scanner;

a column scanner;

a readout controller operative to instruct the row scanner to select one row of pixel acquisition circuits in sequence,

and when one row is selected by the row scanner, instruct the column scanner to read the signals output only by the pixel acquisition circuits that are in activated state.

20. An image acquisition system, comprising:

an optical flow sensor as claimed in claim 19;

an image pre-processor operative to obtain information from the optical flow sensor under image mode; and

an optical flow pre-processor operative to obtain information from the optical flow sensor under optical flow mode.