16. The sense circuit of claim 15, further comprising a limiter circuit coupled to the first and second inputs of the comparator.

17. The sense circuit of claim 16, wherein the limiter circuit comprises a first diode coupled in parallel with a second diode between the first input and the second input, wherein the first diode includes a forward direction from the first input to the second input and the second diode includes a forward direction from the second input to the first input.

18. The sense circuit of claim 16, wherein the limiter circuit further comprises a resistive component.

19. A method, comprising:

precharging a bitline of ~~the~~ a memory device to a precharge voltage, wherein the precharge voltage is based on a sense reference voltage adjusted based on an increase in a wordline voltage;

enabling a selector device coupled to the bitline, wherein enabling the device causes a cell current to flow through the bitline; and

determining a state of a memory cell coupled to the bitline based on a bitline voltage resulting from the cell current.

20. The method of claim 19, wherein determining the state of the memory cell coupled to the bitline based on the cell current comprises:

providing an amplifier output signal based on the adjusted sense reference voltage and a voltage of the bitline; and

comparing the amplifier signal to the bitline voltage.

21. The method of claim 20, further comprising:

providing a second amplifier output signal based on the adjusted sense reference voltage and the bitline voltage; and

adjusting the adjusted sense reference voltage based on the second amplifier signal.