LOW DAMAGE PHOTORESIST STRIP METHOD FOR LOW-K DIELECTRICS

CROSS-REFERENCE TO RELATED APPLICATION

[001] This application claims priority from U.S. Patent Application No.12/636,601, filed December 11, 2009 and incorporated by reference herein.

BACKGROUND

[002] The present invention pertains to methods for stripping photo-resist material and removing etch-related residues from the surface of a partially fabricated integrated circuit in preparation for further processing.

[003] Damascene processing techniques are often preferred methods in many modern integrated circuit manufacturing schemes because it requires fewer processing steps and offers a higher yield than other methods. Damascene processing involves forming metal conductors on integrated circuits by forming inlaid metal lines in trenches and vias in a dielectric layer (inter-metal dielectric). As part of the Damascene process, a layer of photoresist is deposited on a dielectric layer. The photoresist is a light-sensitive organic polymer which can be "spun on" in liquid form and dries to a solid thin film. The photosensitive photoresist is then patterned using light through the mask and wet solvent. A plasma etching process (dry etch) is then used to etch exposed portions of dielectric and transfer the pattern into the dielectric, forming vias and trenches in the dielectric layer.

[004] Once the dielectric layer is etched, the photoresist must be stripped and any etch-related residues must be thoroughly removed before subsequent processing to avoid embedding impurities in the device. Conventional processes for stripping photoresist employ a plasma formed from a mixture of gases with the presence of oxygen in the plasma. The highly reactive oxygen based plasma reacts with and oxidizes the organic photoresist to form volatile components that are carried away from the wafer surface.

[005] Highly oxidizing conditions are also generally unsuitable for use on low dielectric constant (low-k) materials. Low-k materials have been used as inter-metal

and/or inter-layer dielectrics between conductive interconnects in many modern devices to reduce the delay in signal propagation due to capacitive effects. The lower the dielectric constant of the dielectric material, the lower the capacitance of the dielectric and the lower the RC delay of the integrated circuit. Typically, low-k dielectrics are silicon-oxide based materials with some amount of incorporated carbon, commonly referred to as carbon doped oxide (CDO). It is believed, although not necessarily proven, that the oxygen scavenges or removes carbon from the low-k materials. In many of these materials such as CDOs, the presence of carbon is instrumental in providing a low dielectric constant. Hence, to the extent that the oxygen removes carbon from these materials, it effectively increases the dielectric constant. As processes used to fabricate integrated circuits moves toward smaller and smaller dimensions and requires the use of dielectric materials having lower and lower dielectric constants, it has been found that the conventional strip plasma conditions are not suitable.

[006] What is needed therefore are improved and more efficient methods for stripping photoresist and etch-related materials from dielectric materials, especially from low-k dielectric materials.

SUMMARY OF THE INVENTION

[007] The present invention addresses the aforementioned need by providing improved methods for stripping photoresist and removing etch-related residues from dielectric materials. In one aspect of the invention, methods involve removing material from a dielectric layer using a hydrogen-based etch process employing a weak oxidizing agent and fluorine-containing compound. Substrate temperature is maintained at a level of about 160 °C or less, e.g., less than about 90 °C.

[008] In certain embodiment, the methods involve introducing gas comprising a weak oxidizing agent, fluorine-containing compound and hydrogen into the reaction chamber, and applying RF power to form a plasma within the reaction chamber to convert at least a portion of the material to gaseous form, thereby removing at least a portion of the material from the partially fabricated integrated circuit. As stated previously, methods may be used to remove photoresist and/or residues from the etch

process. Methods may be effectively implemented on Damascene devices, including single and dual Damascene devices.

[009] According to various embodiments, the weak oxidizing agent comprises at least one of carbon dioxide, carbon monoxide, nitrous oxide, nitric oxide and nitrogen dioxide and water. In a particular embodiment, the weak oxidizing agent comprises carbon dioxide. In certain embodiments, the gas comprises between about 0.1 % to about 10.0 % carbon dioxide by volume. In some embodiments, the gas further comprises at least one inert carrier gas such as helium, argon or nitrogen. In certain embodiments, the gas does not comprise molecular oxygen.

[0010] According to various embodiments, the fluorine-containing compound comprises at least one of nitrogen trifluoride (NF_3), sulfur hexafluoride (SF_6), hexafluoroethane (C_2F_6), tetrafluoromethane (CF_4), trifluoromethane (CHF_3), difluoromethane (CH_2F_2), octofluoropropane (C_3F_8), octofluorocyclobutane (C_4F_8), octofluoro[1-]butane (C_4F_8), octofluoro[2-]butane (C_4F_8), octofluoroisobutylene (C_4F_8), fluorine (F_2), and the like. In a particular embodiment, the weak oxidizing agent comprises nitrogen trifluoride. In certain embodiments, the gas comprises between about 5ppm to about 10% nitrogen trifluoride by volume.

[0011] Methods of the invention may be implemented on any size wafer. Most modern wafer fabrication facilities use either 200 mm or 300 mm wafers. Process conditions may vary depending upon the wafer size. If a 300 mm wafer is used, the total flow rate of gas may range between about 1,000 sccm and about 40,000 sccm. If carbon dioxide is used as the weak oxidizing agent, the flow rate of carbon dioxide may range between about 10 sccm and about 2000 sccm, e.g., 800 sccm. If nitrogen trifluoride is used as the fluorine-containing gas, the flow rate of nitrogen trifluoride may range between about 1 and 20 sccm, e.g., 5 sccm. Typically, the RF plasma power for a 300 mm wafer ranges between about 300 Watts to about 3 Kilowatts for a plasma. Methods may be implemented using a direct or remote plasma.

[0012] During the application of plasmas to the work piece surface, substrate temperatures can range between about 50°C degrees and about 160°C. In certain embodiments, work piece temperatures are maintained at about 90°C or less.

Example chamber pressures can range between about 300 mTorr and about 2 Torr. In some embodiments, the wafer is held at a bias.

[0013] As mentioned previously, methods of the invention may be used with low-k dielectric materials, including carbon-doped low-k dielectric materials such as carbon-doped oxides (CDOs). Methods of the invention can be implemented on both non-porous and porous dielectric materials, including CDOs and other compositions.

[0014] Methods of the invention may be implemented in any suitable reaction chamber. The reaction chamber may be one chamber of a multi-chambered apparatus or it may be part of a single chamber apparatus. In some embodiments, a multi-stage removal process is used, with the fluoride-containing compound used only a subset of the stages. In certain embodiments, the fluoride-containing compound is used only in a first set of stages, e.g., a first stage. In embodiments wherein a multi-station apparatus is used, the fluoride-containing compound may be used as part of process gas used to generate a plasma in the first station, for example.

[0015] These and other features and advantages of the present invention will be described in more detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 is a process flow diagram illustrating aspects of some embodiments of the invention employed for stripping photoresist and removing etch-related residue from a partially fabricated integrated circuit.

[0017] FIGs. 2A-2C show cross sectional depictions of a low-k Damascene device during dry etch and photoresist strip processes in accordance with the invention.

[0018] FIGS. 3A and 3B show cross sectional depictions of a low-k device during dry after photoresist strip and HF-test processes in accordance with the invention.

[0019] FIG. 4A is a schematic illustration showing an apparatus suitable for practicing the present invention.

[0020] FIG. 4B is a simple block diagram showing a multi-station stripping tool suitable for practicing the present invention.

DETAILED DESCRIPTION

INTRODUCTION

[0021] In the following detailed description of the present invention, numerous specific embodiments are set forth in order to provide a thorough understanding of the invention. However, as will be apparent to those skilled in the art, the present invention may be practiced without these specific details or by using alternate elements or processes. In other instances well-known processes, procedures and components have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

[0022] In this application, the terms "semiconductor wafer", "wafer" and "partially fabricated integrated circuit" will be used interchangeably. One skilled in the art would understand that the term "partially fabricated integrated circuit" can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. The following detailed description assumes the invention is implemented on a wafer. However, the invention is not so limited. The work piece may be of various shapes, sizes, and materials. In addition to semiconductor wafers, other work pieces that may take advantage of this invention include various articles such as printed circuit boards and the like.

[0023] As mentioned previously, methods of the invention may be used to efficiently and effectively to remove photoresist and etch-related materials from a low-k dielectric materials. Methods of the invention are not limited to low-k dielectrics. Methods are also not limited to any particular category of low-k dielectrics. For instance, described methods may be effectively used on dielectrics with k values less than 4.0, dielectrics with k values less than about 2.8 and dielectrics with k values less than about 2.0 ("ultra-low-k" or ULK dielectrics). The low-k dielectric may be porous or non-porous (sometimes referred to as a "dense" low-k dielectric). Generally, low-k dense dielectrics are those having k values no greater than 2.8 and low-k porous dielectrics are those having k values no greater than 2.2. Low-k

dielectrics of any suitable composition may be used, including silicon oxide based dielectrics doped with fluorine and/or carbon. Non-silicon oxide based dielectrics, such as polymeric materials, may also be used. Any suitable process may be used to deposit the low-k dielectric, including as spin-on deposit and CVD deposit techniques. In the case of forming porous dielectrics, any suitable method may be used. A typical method involves co-depositing a silicon-based backbone and an organic porogen and subsequently removing the porogen component, leaving a porous dielectric film. Other methods include sol-gel techniques. Specific examples of suitable low-k films are carbon based spin-on type films such as SILK™ and CVD deposited porous films such as Coral™.

[0024] Methods of the invention use plasmas that are produced from gases that contain hydrogen and a weak oxidizing agent, and in certain processing operations, a fluorine-containing compound. One skilled in the art will recognize that the actual species present in the plasma may be a mixture of different ions and molecules derived from the hydrogen, weak oxidizing agent and/or fluorine-containing compound. It is noted that other species may be present in the reaction chamber, such as small hydrocarbons, carbon dioxide, water vapor and other volatile components as the plasma reacts with and breaks down the organic photoresist and other residues. One of skill in the art will also recognize that reference to the initial gas/gases introduced into the plasma is/are different from other gas/gases that may exist after the plasma is formed.

PROCESS

[0025] Figure 1 is a flow chart depicting one general high-level process flow in accordance with some embodiments of the present invention. Note that some typical operations related to the methods of the invention involved in integrated circuit (IC) fabrication are also included in Figure 1 to provide a context for how the invention may be used. To provide a visual context of some embodiments of the invention, Figures 2A through 2C show cross-sectional depictions of a portion of a low-k Damascene device during various pertinent fabrication processes.

[0026] Referring to Figure 1, a wafer with exposed regions of a low-k dielectric layer are etched leaving a patterned photoresist layer thereon is provided (block 101). Figures 2A and 2B depict the forming of a patterned low-k dielectric in the context of processing a Damascene device 200. Figure 2A shows device 200 before and Figure 2B shows device 200 after a dry etch process. Figure 2B corresponds to the state of the device provided in block 101 of Figure 1.

[0027] Referring to Figure 2A, layer 201 has a low-k dielectric layer 203 deposited thereon, which has portions of photoresist 205 deposited thereon. Depending on the particular integration scheme, underlying layer 201 may be a metal layer such as copper, an etch stop layer such as silicon carbide or silicon nitride, or another type of layer. Photoresist 205 was previously patterned using UV light lithography (or other suitable process) to leave exposed portions of low-k dielectric layer 203. Device 200 is then subjected to a dry etch process, typically one of sputter etching, plasma etching or reactive ion etching.

[0028] As shown in Figure 2B, after the dry etch process, the resulting device 200 has features 210 etched within an ultra low-k dielectric layer 203. Photoresist portions 205 must be stripped before further wafer processing. Note that the tops and sides of the exposed photoresist portions 205 have "skins" 207 that are relatively hard portions of the photoresist as a result of some dry etch processes and that can be compositionally different from the bulk photoresist portions 205. The skin is typically composed of dielectric residues re-deposited from low-k dielectric 203 and re-deposited polymer residue from the photoresist 205. In addition to the skin, a film 209 can also form over exposed sidewalls of low dielectric 203. This film typically is made of polymer residues and damaged portions of the low-k dielectric from ion bombardment during the dry etch process.

[0029] Referring back to Figure 1, the photoresist is stripped of a first portion of the photoresist (block 103). In certain embodiments, this first portion includes skin that was formed from the etch process and is generally tougher to remove. In this operation the wafer is exposed to a hydrogen-based plasma with a weak oxidizing agent and a fluorine-containing compound. For example, in certain embodiments, the wafer is exposed to a H2/CO2/NF3 plasma. As discussed further below, a

relatively small amount of fluorine-containing compound is employed in this operation. In one example, H2 flow rate is about 20,000 sccm (20 slpm), CO2 flow rate 800 sccm (0.8 slpm) and NF3 flow rate 5 sccm. The individual flow rates may vary depending on the particular embodiment. The H2 flow rate is two orders of magnitude larger than that of the CO2 flow rate, and four orders of magnitude larger than the NF3 flow. In certain embodiments, the CO2 flow rate is at least one order of magnitude larger than the NF3 flow. These ranges may be applied to other weak oxidizing agents and fluorine-containing compounds as appropriate.

[0030] This operation is typically performed in a different reaction chamber from the chamber where the etch took place. Such a reaction chamber may be referred to as a stand-alone "strip unit." Any apparatus with a suitable plasma reaction chamber can be used. The system may provide a direct (*in situ* plasma) or remote plasma.

[0031] It should be noted that the operation 103 may be used in certain embodiments to replace a conventional oxygen-based strip that is performed in the same reaction chamber in which the etch took place and typically involves exposure to an oxygen-based plasma. This oxidizing partial strip operation can damage some low-k dielectric materials, and may not be performed in certain implementations. Thus in certain embodiments, the wafer is provided in operation 101 without having previously undergone such a strip process in the etch chamber.

[0032] Referring again to Figure 1, the next operation is to expose the wafer to a hydrogen-based plasma with a weak oxidizing agent to strip the bulk photoresist and/or remove etch-related material (block 105). In certain embodiments, fluorine is not present in this operation, unlike in the previous operation. In certain embodiments, the bulk of the photoresist and residue is removed in this operation, which may itself include multiple sub-operations.

[0033] The total flow rate of gas, the relative amount of weak oxidizing agent and fluorine-containing compound and other conditions in the strip chamber can vary depending upon, among other factors, plasma type (downstream versus direct), RF power, chamber pressure, substrate (wafer) size and type of weak oxidizing agent used. In some examples using the Novellus Gamma™ system (downstream plasma

system), the plasma may comprise between about 0.1% to 10% carbon dioxide by volume and between about 5ppm to 10% nitrogen trifluoride (if present) by volume.

[0034] In addition to hydrogen, weak oxidizing agent, and fluorine-containing gas, a carrier gas such as helium, argon or nitrogen may be used. The carrier gas is typically an unreactive gas. For shipment and handling safety reasons, commercial hydrogen is available in mixtures with noble gases such as helium. These commercially available gas mixtures may be used for the methods of this invention.

[0035] After the majority of the photoresist and etch residue has been removed during plasma strip in operation 105, one or more additional plasma strip or wet clean operations may be performed. It should also be noted that in multi-station apparatuses, operations 103 and 105 may each be performed over one or more than one station.

[0036] The wafer is typically temperature controlled during exposure to the plasma. In particular, the temperature such that it is no more than about 200 °C, no more than about 160°C, no more than about 150°C, no more than about 140°C, no more than about 130°C, no more than about 120°C, no more than about 110°C, no more than about 100°C, no more than about 90°C, no more than about 80°C, or no more than about 60°C. In particular embodiments, the substrate is maintained at temperature no more than about 90°C. It has been found that these relatively low temperatures are critical in certain embodiments to preventing significant damage to the ULK film.

[0037] Figure 3A depicts a patterned ultra low-k dielectric layer 303, hard mask layer 315, and silicon carbide layer 301, after photoresist removal as described above. Etched into low-k dielectric layer 303 is recessed feature 310, which may be a via or trench. The feature 310 includes sidewalls 317 and bottom 319. It has been found that if the photoresist removal occurs at too high of a temperature, the low-k material near the sidewalls 317 is damaged. One manner in which this damage is tested is by an HF dip, for example a 100:1 dilution of HF for 45 seconds. In one example, a photoresist removal process as described above in was performed at 90°C and compared to a process using the same chemistry, but performed at 280°C. Figure 3B depicts the results with 317'' showing the profile of the feature stripped at 280°C, and

317' showing the profile of the feature stripped at 90°C. While the profile 317' was found to be substantially unchanged from the as-stripped feature profile, profile 317'' is bowed inward. The region between these two profiles is the area that is damaged under the high temperature stripping process. The higher temperature process may also remove a certain amount of etch stop material from the bottom of the feature.

[0038] Higher temperatures allow a faster etch rate; however, it has been found that more fluorine is required to etch as the temperature is increased. As a result, damage to the dielectric is increased. Damage can also occur, however, by long exposure times that come from using low temperatures. However, it has been found that temperatures in the ranges described above can prevent or reduce damage within the constraints of these competing effects.

[0039] In one example, the following process conditions were used to produce a low damage strip:

Station 1: 20 slpm H2/0.8 slpm CO2/5 sccm NF3

Station 2-5: 20 slpm H2/0.8 slpm CO2

Stations 1-5: 0.9 Torr / 90°C / 3.5 kW RF plasma / 103 seconds per station

[0040] In certain embodiments, the temperature is raised for one or more operations after exposure to the fluorine-containing plasma. For example, a temperature of less than 160°C or less than 90°C may be used during exposure to the fluorine-based plasma, and raised prior to or during exposure to the one or more operations that use fluorine-free plasmas. Temperature may be raised in stages in certain embodiments, with later stations using higher temperatures than earlier ones. The higher temperature may be within the range described, or may be higher than that described. For example, in certain embodiments, later stations can use higher temperatures such as 285 °C. However, in many embodiments, temperature is maintained at a low temperature throughout the strip process.

[0041] The above description provides examples of removing photoresist using low temperature hydrogen-based plasmas, in particular processes that involve exposing photoresist and etch-related residues to a plasma generated from hydrogen gas, wherein the wafer temperature is maintained at a low temperature, e.g., less than about 200 °C, less than about 160°C, less than about 150°C, less than about 140°C, less than about 130°C, less than about 120°C, less than about 110°C, less than about 100°C, less than about 90°C, less than about 80°C, or less than about 60°C. In certain embodiments, the gas used to generate the plasma consists essentially of hydrogen gas in one or more operations. In alternate embodiments, one or more of a weak oxidizing agent, a fluorine-containing gas and a carrier gas may be added to the hydrogen gas in one or more operations, as described above. Examples of process gas chemistries that may be employed to generate a plasma for the low-temperature exposure operations include H2; H2/CO2; H2/CO2/NF3 and H2/NF3, with other weak oxidizing agents and fluorine-containing agents described above substituted for or added to CO2 and NF3, respectively. Depending on the characteristics of the photoresist and etch residue present, these may be used at any or all of the removal operations depicted in Figures 2A-2C.

[0042] For example, to remove the "skin," the gas used to generate the hydrogen-based plasma may have essentially no CO2 or other weak oxidizing agent present. Also, in certain embodiments, there may essentially no NF3 or other fluorine-containing gas present. The gas used to generate the hydrogen-based plasma to remove the bulk photoresist may have essentially no CO2 or other weak oxidizing agent present. In many embodiments, there may essentially no NF3 or other fluorine-containing gas present, as described above. However, NF3 or other fluorine-containing gas may be present in certain embodiments.

APPARATUS

[0043] As mentioned, any suitable plasma reaction chamber apparatus may be used. Suitable plasma chambers and systems include the Gamma 2100, 2130 I^2CP (Interlaced Inductively Coupled Plasma), G400, and GxT offered by Novellus Systems, Inc. of San Jose, CA. Other systems include the Fusion line from Axcelis Technologies Inc. of Rockville, Maryland, TERA21 from PSK Tech Inc. in Korea,

and the Aspen from Mattson Technology Inc. in Fremont, CA. Additionally, various strip chambers may be configured onto cluster tools. For example, a strip chamber may be added to a Centura cluster tool available from Applied Materials of Santa Clara, CA.

[0044] Figure 4A is a schematic illustration showing aspects of a downstream plasma apparatus 400 suitable for practicing the present invention on wafers. Apparatus 400 has a plasma source 411 and an exposure chamber 401 separated by a showerhead assembly 417. Inside exposure chamber 401, a wafer 403 rests on a platen (or stage) 405. Platen 405 is fitted with a heating/cooling element. In some embodiments, platen 405 is also configured for applying a bias to wafer 403. Low pressure is attained in exposure chamber 401 via vacuum pump via conduit 407. Sources of gaseous hydrogen (with or without dilution/carrier gas), carbon dioxide (or other weak oxidizing agent), and if present nitrogen trifluoride (or other fluorine-containing gas) provide a flow of gas via inlet 409 into plasma source 411 of the apparatus. Plasma source 411 is surrounded in part by induction coils 413, which are in turn connected to a power source 415. During operation, gas mixtures are introduced into plasma source 411, induction coils 413 are energized and a plasma is generated in plasma source 411. Showerhead assembly 417, which has an applied voltage, terminates the flow of some ions and allows the flow of neutral species into exposure chamber 401. As mentioned, wafer 403 may be temperature controlled and/or a RF bias may be applied. Various configurations and geometries of the plasma source 411 and induction coils 413 may be used. For example, induction coils 413 may loop around the plasma source 411 in an interlaced pattern. In another example, the plasma source 411 may be shaped as a dome instead of a cylinder. A controller 450 may be connected to components of the process chamber, and control process gas composition, pressure, temperature and wafer indexing of the stripping operations. Machine-readable media may be coupled to the controller and contain instructions for controlling process conditions for these operations.

[0045] As mentioned, in some embodiments, the apparatus of the invention is a strip unit dedicated to stripping photoresist from wafers. Generally, such a strip unit tool will have multiple wafer process stations so that multiple wafers may be processes simultaneously. Figure 4B is a simple block diagram showing a top-down view of a

multi-station wafer strip unit tool 430 that may be used in accordance with the invention. Strip unit tool 430 has five strip stations 433, 435, 437, 439 and 441 and one load station 431. Strip unit tool 430 is configured such that each station is capable of processing one wafer and so all stations may be exposed to a common vacuum. Each of strip stations 433, 435, 437, 439 and 441 has its own RF power supply. Load station 431 is typically configured with a load-lock station attached thereto to allow the input of wafers into strip unit tool 430 without a break in vacuum. Load station 431 may also be configured with a heat lamp to pre-heat wafers before transferring to strip stations and photoresist stripping. Strip station 441 is typically configured with a load-lock station attached thereto to allow the output of wafers from strip unit tool 430 without a break in vacuum. A robotic arm 443 transfers wafers from station to station.

[0046] During typical manufacturing mode, wafers are processed in batch mode. Batch mode processing can increase wafer though-put and is therefore commonly used in manufacturing operation. In batch mode, each wafer is transferred to, and processed in, each of stations 431, 433, 435, 437, 439 and 441. For example, a typical batch mode process will proceed as follows: A wafer is first loaded into load station 431 where it is preheated with a heat lamp. Next, robotic arm 443 transfers the wafer to strip station 433 where it is plasma processed using a fluorine-based plasma for a time period sufficient to strip off about 1/5 of the photoresist. Robotic arm 443 then transfers the wafer to strip station 435 where it is plasma processed using a non-fluorine process for a time period sufficient to strip off about another 1/5 of the remaining photoresist. This sequence is continued such that the wafer is processed at strip stations 437, 439 and 441. At strip station 441, the photoresist should be largely removed and the wafer is then unloaded from the strip unit tool.

[0047] Although various details have been omitted for clarity's sake, various design alternatives may be implemented. Therefore, the present examples are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims.

CLAIMS

1. A method of removing material from a low-k dielectric layer on a work piece as part of a partially fabricated integrated circuit after an etch process, the method comprising:

forming a first plasma from a gas comprising hydrogen and a fluorine-containing compound; exposing the work piece to the first plasma; forming a second plasma from a gas comprising hydrogen; and exposing the work piece to the second plasma, wherein exposure to the first and second plasma removes material from the low-k dielectric layer; and

wherein the work piece temperature is maintained at a temperature below about 100°C.

2. The method of claim 1, wherein the work piece temperature is maintained at a temperature below about 90°C.

3. The method of any of claims 1-2, wherein the gas from which the first plasma is formed further comprises a weak oxidizing agent.

4. The method of claim 3, wherein the weak oxidizing agent comprises at least one of carbon dioxide, carbon monoxide, nitrous oxide, nitric oxide, nitrogen dioxide and water.

5. The method of claim 3, wherein the weak oxidizing agent is carbon dioxide.

6. The method of any of claims 1-5, wherein the fluorine-containing compound is comprises at least one of nitrogen trifluoride (NF_3), sulfur hexafluoride (SF_6), hexafluoroethane (C_2F_6), tetrafluoromethane (CF_4), trifluoromethane (CHF_3), difluoromethane (CH_2F_2), octofluoropropane (C_3F_8), octofluorocyclobutane (C_4F_8), octofluoro[1-]butane (C_4F_8), octofluoro[2-]butane (C_4F_8), octofluoroisobutylene (C_4F_8), and fluorine (F_2).

7. The method of claim 6, wherein the fluorine-containing compound is nitrogen trifluoride.

8. The method of any of claims 1-7, wherein the second plasma is substantially fluorine-free.

9. The method of any of claims 1-8 wherein the work piece has not undergone a previous oxygen-based plasma photoresist stripping operation.

10. The method of any of claims 1-9, wherein the material being removed from the dielectric layer comprises photoresist and/or residues from the etch process.

11. A method of removing material from a low-k dielectric layer on a work piece as part of a partially fabricated integrated circuit after an etch process, the method comprising:

forming a first plasma from a gas comprising hydrogen, a weak oxidizing agent and a fluorine-containing compound;

exposing the work piece to the first plasma to thereby remove etch-related residue from the low-k dielectric layer, wherein the work piece temperature is maintained at a temperature below about 100°C during the exposure to the first plasma.

12. The method of claim 11 wherein work piece temperature is maintained at a temperature below about 90°C during the exposure to the first plasma.

13. The method of any of claims 11-12 further comprising forming a second plasma from a gas comprising hydrogen and a weak oxidizing agent; and exposing the work piece to the second plasma.

14. The method of claim 13 wherein work piece temperature is maintained at a temperature below about 160°C during the exposure to the second plasma.

15. The method of claim 13 wherein work piece temperature is maintained at a temperature below about 90°C during the exposure to the second plasma.

16. The method of any of claims 13-15, wherein the second plasma is substantially fluorine-free.

17. The method of any of claims 13-16 wherein the work piece temperature is higher during exposure to the second plasma than during exposure to the first plasma.

18. The method of any of claims 11-17 wherein the volume percentage of the fluorine-containing compound in the gas is no more than 1%.

19. An apparatus for removing material from a low-k dielectric work piece surface as part of a partially fabricated integrated circuit after an etch process, the apparatus comprising:

a reaction chamber comprising:

a plasma source,

a showerhead positioned downstream of the plasma source, and

a work piece support downstream of the showerhead, said work piece support comprising a pedestal and temperature-controlling mechanism to control a temperature of a work piece supported on the work piece support; and

a controller for executing a set of instructions, said set of instruction comprising instructions for receiving in the reaction chamber the substrate having a low-k dielectric work piece surface, forming a first plasma from a gas comprising hydrogen, a weak oxidizing agent and a fluorine-containing compound; exposing the work piece to the first plasma to thereby remove the material from the low-k dielectric; forming a second plasma from a gas comprising hydrogen and a weak oxidizing agent; exposing the work piece to the second plasma to thereby remove the material from the low-k dielectric, and maintaining the work piece at a temperature below about 100°C during the exposure operations.

20. The method of claim 1, wherein the dielectric layer is an ultra-low k dielectric layer.

21. The method of claim 1, wherein the material removed comprises bulk photoresist and the work piece temperature is maintained at a temperature below about 160°C throughout removal of the bulk photoresist.