

ABSTRACT OF THE DISCLOSURE

A memory device includes a path state check circuit configured to check states of signal transmission paths, each signal transmission path including a data transmission path and a clock transmission path of the memory device. The path state check circuit includes a sampling circuit configured to perform a sampling operation by using pattern data that has passed through the data transmission path and a clock signal that has passed through the clock transmission path, and generate sample data, and a management circuit configured to generate a comparison of the sample data with the pattern data and manage check result information indicating whether a re-training operation for the memory device is to be performed, based on a result of the comparison.

[FIG. 1]