A PULSE COUNT FM DETECTOR

The present invention relates to a pulse count FM detector.

A known pulse count FM detector produces an FM detection output in such a way that a frequency modulation (FM) signal which is transposed into a pulse train by an FM prelimiter is converted into a train of pulses having a predetermined pulse width every period (single) or every half period (double), by a monostable multivibrator (pulse width modulation). This train of pulses is then passed through a low-pass filter.

This known detection system has the disadvantage that, since the pulse train generated by the pulse width modulation is a binary pulse signal, high-frequency components and carrier components contained therein are liable to appear at the output of the low-pass filter, which results in an inferior S/N (signal-to-noise) ratio of the FM detection output.

It is an object of the present invention to provide a pulse count FM detector which can achieve both an improved S/N ratio and an improvement in responsiveness.

According to one aspect of the present invention there is provided a pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) a pair of monostable circuits, the first of which generates output signals of a predetermined pulse width in response to the leading edges of the train of pulses output from the limiter-amplifier;

(c) an inverter connected between the output of the limiter-amplifier and the second monostable circuit, whereby the second monostable circuit generates output pulses of a predetermined width in response to the trailing edges of the train of pulses output from the limiter-amplifier;

(d) an analog adder which analog-adds the output signals of the monostable circuits; and

(e) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre frequency of the FM intermediate frequency, the output from the analog adder is constant.

According to a second aspect of the present invention there is provided a pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) a pair of monostable circuits, the first of which generates output signals of a predetermined pulse width in response to the leading edges of the train of pulses output from the limiter-amplifier;

(c) frequency division means located between an output terminal of the limiter amplifier and the input terminals of the pair of monostable circuits;

(d) an inverter connected between the output of the limiter-amplifier and the second monostable circuit, whereby the second monostable circuit generates output pulses of a predetermined width in response to the leading edges of the train of pulses output from the limiter-amplifier;

(e) an analog adder which analog-adds the output signals of the monostable circuits; and

(f) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre

frequency of the FM intermediate frequency, the output from the analog adder is constant.

According to a third aspect of the present invention there is provided a pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) four monostable circuits arranged in two pairs for generating output signals of a predetermined pulse width in response to leading edges or trailing edges of the train of pulses;

(c) a first frequency divider which is located between the output of the limiter-amplifier and the inputs to the first pair of monostable circuits;

(d) a second frequency divider connected to the inputs to the second pair of monostable circuits;

(e) a first inverter located between the output of the limiter-amplifier and the second frequency divider;

(f) second and third inverters respectively connected between the outputs of respective first and second frequency dividers and respective second monostable circuits of each pair of monostable circuits; such that each monostable of the first pair responds to every other one of the leading edges and each monostable of the second pair responds to every other one of the trailing edges of the train of pulses output from the limiter-amplifier;

(g) an analog adder which analog-adds the output signals of the monostable circuits; and

(h) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre frequency of the FM intermediate frequency, the output from the analog adder is constant.

According to a fourth aspect of the present

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invention there is provided a pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) eight monostable circuits arranged in four pairs of generating output signals of a predetermined pulse width in response to leading edges or trailing edges of the train of pulses;

(c) frequency division means connected to the output from the limiter-amplifier to provide four equispaced phase shifted outputs, a resective phase shifted output being applied to a respective first monostable circuit; whereby the first monostables of each pair respond sequentially to four successive leading and trailing edges of the train of pulses output from the limiter-amplifier;

(d) four inverters respectively connected between the four outputs of the frequency division means and respective second monostable circuits of each of the pairs of monostable circuits, whereby the second monostables of each pair respond sequentially to the next four successive leading and trailing edges of the train of pulses output from the limiter amplifier;

(e) an analog adder which analog-adds the output signals of the pairs of monostable circuits; and

(f) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre frequency of the FM intermediate frequency, the output from the analog adder is constant.

The present invention will now be descrbied in greater

detail by way of example with reference to the accompanying drawings wherein:-

Figures 1A and 1B are a block diagram and a waveform diagram, respectively, showing a first embodiment in the case where the invention is applied to a double count type FM detector;

Figures 2A and 2B are a block diagram and a waveform diagram, respectively, showing a second embodiment in the case where the invention is applied to a single count type FM detector;

Figures 3A and 3B are a block diagram and a waveform diagram, respectively, showing a third embodiment in the case where the invention is applied to a double pulse count FM detector; and

Figures 4A and 4B are a block diagram and a waveform diagram, respectively, showing a modification of the third embodiment shown in Figures 3A and 3B.

Referring first to the embodiment shown in Figs. 1A and 1B as applied to a double count type FM detector, the circuit shown in Fig. 1A includes a limiter - amplifier LA, two monostable circuits MM_1 and MM_2, and a low-pass filter LPF. The limiter-amplifier LA converts the waveform of an FM intermediate frequency amplifier output signal FMIF into a train of pulses V_1 having a predetermined amplitude.

The monostable circuit MM_1 receives the pulse train V_1, and forms a train of output pulses V_2 of a predetermined pulse width which are synchronous with the leading edges of the train of pulses V_1. The monostable circuit MM_2 receives a train of pulses $\overline{V_1}$ with the pulse train V_1 inverted by an inverter IV_1. It forms a train of output pulses V_3 which have a predetermined pulse width similar to the output pulse train V_2 and which are synchronous with the leading edges of the

train of pulses $\overline{V_1}$ (the trailing edges of the train of pulses V_1) likewise to the above. In this embodiment, the pulse width of each pulse in the trains of output pulses V_2 and V_3 to be formed by the monostable circuits MM_1 and MM_2 is set to be substantially equal to the pulse width of the train of pulses V_1 at the time at which the frequency of the train of pulses V_1 is the centre frequency of the FM intermediate frequency signal (the frequency during no modulation), unlike the pulse width in the known pulse count detector, referred to above.

The outputs V_2 and V_3 of the respective monostable circuits MM_1 and MM_2 are analog-added by two resistors R. The added pulse signal is transmitted to the low-pass filter LPF, the output of which provides an FM detection output DET.

Since the output pulses V_2 and V_3 from the respective monostable circuits MM_1 and MM_2 are provided every half period of the train of input pulses V_1, the pulse count FM detection operation of the double type is performed.

The detailed operations of the circuit shown in Fig. 1A will be described with reference to the waveform diagram shown in Figure 1B. As shown, the train of pulses V_1 are modulated from a low frequency via the centre frequency (the frequency during no modulation) to a high frequency. The output pulse train V_2 of the monostable circuit MM_1 becomes the train of pulses of the predetermined pulse width which are synchronous with the leading edges of the train of pulses V_1. On the other hand, the output pulse train V_3 of the monostable circuit MM_2 becomes the train of pulses of the predetermined pulse width which are synchronous to the trailing edges of the train of pulses V_1.

As in the known pulse count FM detector the trains of pulses V_2 and V_3 have equal pulse widths. The embodiments of

the present invention, however, greatly differ in that the pulse widths are enlarged and that the analog addition of both the trains of pulses is executed.

More specifically, the trains of output pulses V_2 and V_3 from the respective monostable circuits MM_1 and MM_2 are synthesized (analog-added) through the resistors R. As shown in Fig. 1B, the analog addition voltage V_4 is at a low level (zero volts) when both the trains of pulses V_2 and V_3 are at the low level, and it is divided by the resistors R and is at a medium level (V/2) when only one of the trains of pulses V_2 and V_3 is in the state of high level. Further, when both the trains of pulses V_2 and V_3 are at the high level, the analog addition voltage V_4 is at the high level (V).

In other words, when the frequency of the train of input pulses V_1 is lower than the centre frequency of the FM intermediate frequency signal, the trains of pulses V_2 and V_3 are not at the high level simultaneously, so that the analog addition voltage V_4 forms a train of pulses which change between the medium level (V/2) and the low level (zero volts).

Subsequently, when the frequency of the train of input pulses V_1 agrees with the centre frequency of the FM intermediate frequency signal, the trains of pulses V_2 and V_3 are at the high level alternately without overlap. Therefore, the analog addition voltage V_4 agrees with the medium level V/2.

When the frequency of the train of input pulses V_1 becomes higher than the centre frequency of the FM intermediate frequency signal, the high levels of the trains of pulses V_2 and V_3 overlap each other. The analog addition voltage V_4 is at the high level (V) for the period during which the high levels overlap, and it is at the medium level

V/2 when either the train of pulses V_2 or V_3 is at the high level. Accordingly, the analog addition voltage V_4 becomes a train of pulses which change between the medium level (V/2) and the high level (V).

Thus, the analog addition voltage V_4 becomes a modulation signal whose pulse width and pulse level both change in accordance with the frequency of the train of input pulses V_1.

As shown in Figure 1B, the level of the input signal V_4 to the low-pass filter coincides with the medium level V/2 without changing, during no modulation (that is, when the frequency of the train of input pulses V_1 is in agreement with the centre frequency of the FM intermediate frequency signal). Consequently, carrier (intermediate frequency) components do not appear at the output of the low-pass filter LPF. For the above reason, the detection output signal DET of very low distortion can be produced.

Further, the analog addition voltage V_4 changes between the low level (zero volts), the medium level (V/2) and the high level (V), and such voltage values are obtained every half period (double) of the train of input pulses V_1. Therefore, the FM detection output DET of quick response can be produced.

Referring now to the second embodiment shown in Fig. 2 as applied to a single count type FM detector, a train of pulses V_1 formed through a limiter-amplifier LA has its frequency reduced to ½ by a ½ frequency divider FD. Accordingly, the period of a train of frequency division output pulses V_1' is double that of the train of input pulses V_1.

An analog addition voltage V_4' with a pulse width and a pulse level modulated is produced by monostable circuits MM_1' and MM_2', analog addition resistors R, having an

arrangement similar to that of Figure 1A, and it is transmitted to a low-pass filter LPF. In this embodiment, the analog addition voltage V_4' is applied to the low-pass filter LPF through a buffer amplifier BA.

In addition, the pulse widths of trains of output pulses V_2' and V_3' from the respective monostable circuits MM_1' and MM_2' are set to be substantially equal to double the pulse width of the train of pulses V_1' at the time at which the frequency of the train of pulses V_1 is the centre frequency.

By setting the pulse widths in this manner, the analog addition voltage V_4' can be set at the medium level (V/2) of its assumable values (0 V - 1 V) when the frequency of the train of pulses V_1 is the centre frequency of an FM intermediate frequency signal.

Since this embodiment is of the single type, responsiveness is somewhat inferior. On the other hand, however, there is the advantage that the monostable circuits MM_1' and MM_2' may have a low response speed, in other words, circuits of low cost.

Referring now to the third embodiment shown in Fig. 3 as applied to the double type FM detector, a train of input pulses V_1 formed by a limiter-amplifier LA is, on one hand, subjected to ½ frequency division by a first ½ frequency divider FD and then applied to a monostable circuit MM_{11}. The frequency-divided pulse train is also applied to a monostable circuit MM_{21} through an inverter IV_{11}. Outputs from these monostable circuits MM_{11} and MM_{21} are converted into a logical sum signal V_2 by an OR circuit OR1 of high-level-preference.

The train of input pulses V_1 is also inverted by an inverter IV_2. The inverted pulse train is subjected to

frequency division by a second ½ frequency divider FD', and then applied to a monostable circuit MM_{12}. The frequency-divided pulse train $\overline{V_1''}$ is applied to a monostable circuit MM_{22} through an inverter IV_{12}. Outputs from these monostable circuits MM_{12} and MM_{22} are converted into a logical sum signal V_3 by an OR circuit OR2 of high-level-preference.

Likewise to the above, the logical sum signals V_2 and V_3 are applied to two resistors R so as to form an analog addition voltage V_4. Further, the analog addition voltage V_4 is transmitted through a buffer amplifier BA to a low-pass filter LPF, in which it is converted into an FM detection output signal DET.

In this embodiment, the pulse widths of the output pulses of the four monostable circuits MM_{11} to MM_{22} are set to be substantially equal to the pulse width of the train of pulses V_1 at the time at which the frequency of the pulse train V_1 is the centre frequency of an FM intermediate frequency signal (the frequency during no modulation).

In this embodiment, the outputs of one set of monostable circuits MM_{11}, MM_{21} and MM_{12}, MM_{22} have the logical sums taken, respectively. In effect, therefore, operations similar to those of the circuit shown in Figure 1A are performed.

Referring now to the modified form of circuit shown in Fig. 4 in which the pulse count FM detector has a still lower distortion factor.

This modified embodiment is so constructed that an analog addition voltage V_4 on the input side of a low-pass filter LPF have five levels, for example, 0 V, ¼ V, $\frac{2}{4}$ V, $\frac{3}{4}$ V and 1 V.

A train of input pulses V_1 formed by a limiter-amplifier LA is converted into frequency division outputs

C_1 to C_4 each having ¼ frequency, by a ring counter RC which acts as a delay circuit.

The pulse trains C_1 to C_4 subjected to ¼ frequency division are respectively applied to monostable circuits MM_{11} to MM_{14} located on one side. In addition, the pulse trains C_1 to C_4 are respectively inverted by inverters IV_{11} to IV_{14} and then applied to monostable circuits MM_{21} to MM_{24} located on the other side.

Outputs from the monostable circuits MM_{11} and MM_{21} are converted into their logical sum signal V_{11} by OR circuits OR_{11} of high-level-preference. The same applies to the other sets of monostable circuits MM_{12} and MM_{22}.

Such logical sum signals V_{11} to V_{14} are respectively applied to resistors R so as to form the analog addition voltage V_4. This analog addition voltage V_4 is transmitted through a buffer amplifier BA to the low-pass filter LPF, in which an FM detection output signal DET is formed.

The pulse widths of the output pulses of the monostable circuits MM_{11} to MM_{24} are set to be substantially equal to double the pulse width of the train of pulses V_1 at the time at which the frequency of the pulse train V_1 is the centre frequency.

By setting the pulse widths in this manner, the analog addition voltage V_4 can be set at the medium level (½ V) of its assumable values (0 V - 1 V) when the frequency of the train of pulses V_1 is the centre frequency of an FM intermediate frequency signal.

The operation of this modified circuit will now be described with reference to the waveform diagram shown in Figure 4B.

As shown in Figure 4B, the train of pulses V_1 are modulated from a low frequency via the centre frequency to a

high frequency.

The frequency division output C_1 of the ring counter RC has its level changed in synchronism with the fall of every second period of the train of input pulses V_1. Therefore, one period of this output becomes quadruple the period of the train of input pulses V_1.

The other frequency division outputs C_2 to C_4 of the ring counter RC change with successive delays each of which is equal to a half period of the train of input pulses V_1.

The logical sum output V_{11} between the outputs of the monostable circuits MM_{11} and MM_{21} which receive the frequency division output C_1 and the inverted signal thereof, becomes a train of pulses which have a predetermined pulse width and which are synchronous with the trailing edges every half period of the frequency division output C_1, namely, every two periods of the input pulse train V_1. The logical sum outputs V_{12} to V_{14} for the other frequency division outputs C_2 to C_4 become trains of pulses which have successive delays, each being equal to the half period of the input pulse train V_1, with respect to the pulse train V_{11}.

When the frequency of the pulse train V_1 is the centre frequency of the FM intermediate frequency signal (the frequency during no modulation), two of the pulse trains V_{11} to V_{14} are at the high level at the same time in succession. The analog addition voltage V_4 therefore becomes the medium level (1/2 V) of its assumable values (0 V - 1 V).

When the frequency of the input pulse train V_1 is lower than the centre frequency mentioned above, either one of the pulse trains V_{11} to V_{14} is at the high level or two of them are at the high level simultaneously, for a short time. The analog addition voltage V_4 is therefore a pulse signal which changes between the medium level (V/2) and a 1/4 level (V/4).

When the frequency of the input pulse train V_1 becomes still lower, any two or more of the pulse trains V_{11} to V_{14} are not at the high level simultaneously. As a result, the analog addition voltage V_4 becomes a pulse signal which changes between the 1/4 level (1/4 V) and the low level (0 V).

On the other hand, when the frequency of the pulse train V_1 becomes higher than the centre frequency, any two or three of the pulse trains V_{11} to V_{14} are at the high level at the same time in succession, for a part of the time. The analog addition voltage V_4 therefore becomes a pulse signal which changes between the medium level (V/2) and a 3/4 level (3/4 V).

When the frequency of the pulse train V_1 becomes still higher, any three or four of the pulse trains V_{11} to V_{14} are at the high level at the same time in succession. The analog addition voltage V_4 therefore becomes a pulse signal which changes between the 3/4 level (3/4 V) and the high level (1 V).

In this manner, the analog addition voltage V_4 becomes the signal wherein the level which the pulse can assume changes in accordance with the frequency of the pulse train V_1.

In an alternative construction (not illustrated) the inverters IV_1 and IV_{11} to IV_{14} may be omitted and the circuit modified by using as one of each set of monostable circuits, a monostable circuit of the positive edge trigger type and as the other monostable circuit, a monostable circuit of the negative edge trigger type.

In a further modification, the analog adder circuit comprises an operational amplifier circuit so as to amplify the maximum level into, e.g., 2 V or 4 V. Also with this measure, the gain of a succeeding-stage amplifier which

receives the detection output can be made low, the S/N (signal-to-noise) ratio does not deteriorate and can be improved still further because the gain on the input side can be made high.

The embodiment shown in Figure 4A may be further modified so as to change the addition output every 1/8 V, by increasing the frequency division ratio more.

The above described embodiments can be extensively utilized in the FM detectors of FM radio receivers and also in video tape recorders and video disk players.

CLAIMS.

1. A pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) a pair of monostable circuits, the first of which generates output signals of a predetermined pulse width in response to the leading edges of the train of pulses output from the limiter-amplifier;

(c) an inverter connected between the output of the limiter-amplifier and the second monostable circuit, whereby the second monostable circuit generates output pulses of a predetermined width in response to the trailing edges of the train of pulses output from the limiter-amplifier;

(d) an analog adder which analog-adds the output signals of the monostable circuits; and

(e) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre frequency of the FM intermediate frequency, the output from the analog adder is constant.

2. A pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) a pair of monostable circuits, the first of which generates output signals of a predetermined pulse width in response to the leading edges of the train of pulses output from the limiter-amplifier;

(c) frequency division means located between an output terminal of the limiter amplifier and the input terminals of the pair of monostable circuits;

(d) an inverter connected between the output of the limiter-amplifier and the second monostable circuit, whereby the second monostable circuit generates output pulses of a predetermined width in response to the leading edges of the train of pulses output from the limiter-amplifier;

(e) an analog adder which analog-adds the output signals of the monostable circuits; and

(f) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre frequency of the FM intermediate frequency, the output from the analog adder is constant.

3. A pulse count FM detector according to claim 2, wherein said frequency divider executes $\frac{1}{2}$ frequency division.

4. A pulse count FM detector according to claim 3, wherein a buffer amplifier is provided between the analog adder and the low-pass filter.

5. A pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) four monostable circuits arranged in two pairs for generating output signals of a predetermined pulse width in response to leading edges or trailing edges of the train of pulses;

(c) a first frequency divider which is located between the output of the limiter-amplifier and the inputs to the first pair of monostable circuits;

(d) a second frequency divider connected to the inputs to the second pair of monostable circuits;

(e) a first inverter located between the output of the limiter-amplifier and the second frequency divider;

(f) second and third inverters respectively connected between the outputs of respective first and second frequency dividers and respective second monostable circuits of each pair of monostable circuits; such that each monostable of the first pair responds to every other one of the leading edges and each

monostable of the second pair responds to every other one of the trailing edges of the train of pulses output from the limiter amplifier;

(g) an analog adder which analog-adds the output signals of the monostable circuits; and

(h) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre frequency of the FM intermediate frequency, the output from the analog adder is constant.

6. A pulse count FM detector according to claim 5, wherein two OR-circuits each receive the outputs from the monostable circuits of a respective pair and output respective single outputs to the analog adder.

7. A pulse count FM detector including:

(a) a limiter-amplifier which converts the waveform of an FM intermediate frequency signal into a train of pulses;

(b) eight monostable circuits arranged in four pairs of generating output signals of a predetermined pulse width in response to leading edges or trailing edges of the train of pulses;

(c) frequency division means connected to the output from the limiter-amplifier to provide four equi-spaced phase shifted outputs, a respective phase shifted output being applied to a respective first

monostable circuit of each of the pairs of monostable circuits, whereby the first monostables of each pair respond sequentially to four successive leading and trailing edges of the train of pulses output from the limiter-amplifier;

(d) four inverters respectively connected between the four outputs of the frequency division means and respective second monostable circuits of each of the pairs of monostable circuits, whereby the second monostables of each pair respond sequentially to the next four successive leading and trailing edges of the train of pulses output from the limiter amplifier;

(e) an analog adder which analog-adds the output signals of the pairs of monostable circuits; and

(f) a low-pass filter whose input terminal is supplied with an output signal from said analog adder and whose output terminal provides a detection output signal;

whereby said detector operates such that when the frequency of the train of pulses is the centre frequency of the FM intermediate frequency, the output from the analog adder is constant.

8. A pulse count FM detector according to claim 7, wherein said frequency division means is a ring counter which provides a division by four, and provides four equi-spaced phase shifted outputs.

9. A pulse count FM detector according to claim 7 or 8, wherein four OR circuits each receive the outputs from the monostable circuits of a respective pair and output respective single outputs to the analog adder.

10. A pulse count FM detector according to any one of the preceding claims 5 to 9, wherein a buffer amplifier is provided between the analog adder and the low-pass filter.

11. A pulse count FM detector constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 1A and 1B; or Figures 2A and 2B; or Figures 3A and 3B; or Figures 4A and 4B of the accompanying drawings.