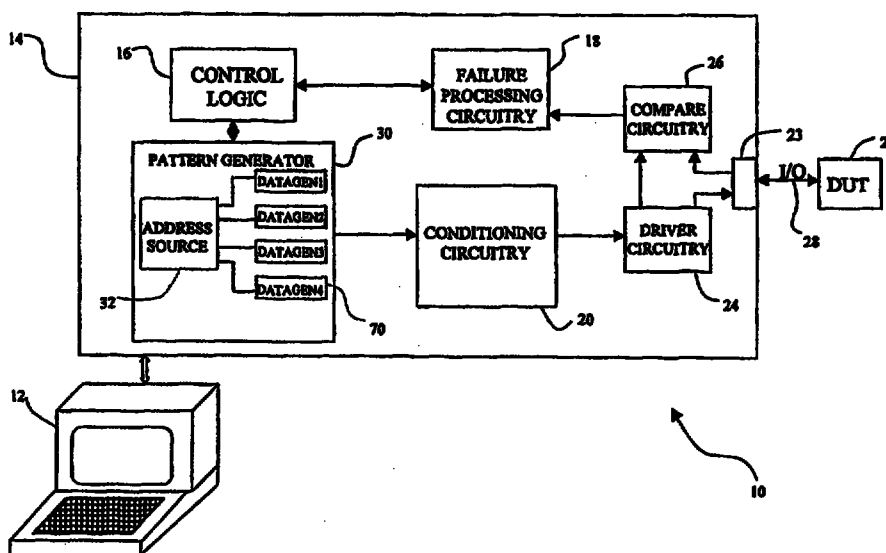


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(54) Title: PATTERN GENERATOR FOR A PACKET-BASED MEMORY TESTER



(57) Abstract

A pattern generator for use in a memory tester to provide packet address and data signals to a packet-based memory-under-test is disclosed. The pattern generator includes an address source for generating an external packet memory address signal. The external packet memory address signal represents a plurality of addressable memory elements in the memory-under-test. A plurality of data generators are disposed in parallel relationship and coupled to the output of the address source to receive at least a portion of the packet memory address signal. Each of the data generators has logic operative to derive an internal address from the packet address. The internal address corresponds to an individual memory element within the memory under test. A sequencer is disposed at the outputs of the data generators to distribute the data generator outputs in a packet waveform for application to the memory-under-test.