

3D STACKED PACKAGE INTEGRATED CIRCUIT CHIP AND ITS FAILURE LOCATION METHOD AND DEVICE

The present patent application claims priority from an earlier Chinese invention patent
5 application number 2022 1 0371179.6 (published as CN114441598B) that is filed with
CNIPA on 11 April 2022 and has the same title. Content and/or relevant subject matter
of the priority application is hereby incorporated entirely and/or wherever appropriate by
reference.

10 Embodiments of the present application relate to the field of semiconductor device
inspection technology, and in particular to a 3D stacked package integrated circuit chip
and its failure location method and device.

As semiconductor wafer manufacturing is moving towards advanced processes, Moore's
Law is facing great challenges. Traditional technologies such as overlay packaging and
15 stacked packaging no longer meet the requirements of Central Processing Unit (CPU),
Graphics Processing Unit (GPU), Field Programmable Gate Array (FPGA), etc.
Therefore, the demand for 2.5D/3D advanced packaging technology is gradually
increasing, becoming one of the core technologies to solve high-end product
applications and to continue Moore's Law.

20 However, the development of 3D packaging technology also brings new challenges to
failure analysis. For example, it has become very difficult to locate the failure of a 3D
stacked package IC chip. The device includes many layers, and the failure information
can be effectively measured by equipment such as indium gallium arsenic microscope
and enhanced thermal imager, but it is impossible to determine from which location of

the film layer this information comes. Therefore, how to locate the failure of 3D stacked package IC chips has become an urgent technical problem to be solved.

Embodiments of the present application provide a 3D stacked package integrated circuit chip and a failure location method and apparatus thereof to achieve failure location of a
5 3D stacked package integrated circuit chip.

In a first aspect, embodiments of the present application provide a method for locating a failure of a 3D stacked package integrated circuit chip (also known as a sample device, standard device or standard sample device), comprising:

- identifying of multiple contrast detection layers located at different depths in the
10 standard sample device;
- detecting, by means of a thermal imager, the phase values corresponding to the different detection frequencies of said contrast detection layer exposed in the failure state, after each grinding out of said contrast detection layer;
- determining a failure locus curve for each comparison detection layer based on
15 the correspondence between the detection frequency and the phase value for that comparison detection layer in the failure state; wherein said failure locus curve is a curve of the phase value of the comparison detection layer as a function of the detection frequency; and
- locating failure of the 3D stacked package IC chip to be tested according to the
20 failure location curve of each comparison detection layer.

Said standard sample device is the same type of 3D stacked package IC chip to be tested without failure, known as proper or intact 3D stacked package integrated circuit chip.

Optionally, said determining a plurality of contrast detection layers located at different
25 depths in the standard sample device, comprising a step of determining a plurality of

contrast detection layers located at different depths based on the thickness of said standard sample device.

Alternatively, a plurality of contrast detection layers located at different depths are determined based on the functional film layers possessed by said standard sample
5 device.

Optionally, said detecting the phase values corresponding to the different detection frequencies of said contrast detection layer in the failure state as exposed, comprising a step of, after the surface of the exposed contrast detection layer is short-circuited to failure, the phase values of the exposed contrast detection layer at different detection
10 frequencies are detected by a thermal imager from the side of said standard sample device, away from the grinding side.

Optionally, determining a plurality of contrast detection layers located at different depths based on the thickness of said standard sample device, comprising a step of dividing said standard sample device into multiple alternative comparison layers of equal
15 thickness according to a pre-set thickness, and a step of selecting said alternative contrast layer as said contrast detection layer.

Optionally, said determination of a plurality of contrast detection layers located at different depths based on the functional film layers that said standard sample device has, comprising a step of identifying the functional film layer of said standard sample device
20 as an alternative comparison layer, and selecting said alternative contrast layer as said contrast detection layer with an interval.

Optionally, said functional film layer of said standard sample device comprises: a solder ball layer, a PCB substrate, a first connected contact point layer, an adapter unit, a second connected contact point layer and a top chip set in sequence in a laminated

manner; said spaced selection of said alternative contrast film layer as said contrast detection layer comprises the solder ball layer located on the side of the PCB substrate away from said adapter unit, the first connected contact point layer between the PCB substrate and the adapter unit, and the second connected contact point layer between
5 said adapter unit and said top layer chip are selected as the comparison detection layers.

Optionally, said failure localization of the 3D stacked package integrated circuit chip to be tested according to the failure localization curve of each comparison detection layer, further comprising:

- detecting, by means of a thermal imager, the phase values of said 3D stacked
10 packaged integrated circuit chip to be tested at different detection frequencies; wherein the detection frequency range for said 3D stacked packaged integrated circuit chip to be tested lies within the detection frequency range for said standard sample device; and
- determining the failure position curve to be tested according to the
15 correspondence between the detection frequency and the phase value of said 3D stacked package integrated circuit chip to be tested; said failure position curve to be tested is a curve of the phase value of the 3D stacked package integrated circuit chip to be tested with the detection frequency.

Optionally, said failure localization (i.e. identifying location) of the 3D stacked package
20 integrated circuit chip (IC) to be tested based on the failure localization curve for each comparison detection layer, comprising a step of determining the position of the failure film layer of said 3D stacked package IC chip to be tested based on the relative distance between the failure positioning curve of each comparison detection layer and said failure position curve to be tested.

In a second aspect, embodiments of the present application provide a failure location device for a 3D stacked package integrated circuit chip for performing the failure location method for a 3D stacked package integrated circuit chip as described in any one of the first aspects, comprising.

- 5 A contrast detection layer determination unit for determining a plurality of contrast detection layers located at different depths in a standard sample device.

A phase value detection unit for detecting, by means of a thermal imager, the phase values corresponding to the different detection frequencies of said contrast detection layers exposed in the failure state, after grinding out each of said contrast detection
10 layers in turn.

A failure positioning curve determination unit for determining the failure positioning curve of each comparison detection layer based on the correspondence between the detection frequency and the phase value in the failure state of that comparison detection layer; wherein said failure positioning curve is a curve of the phase value of the comparison
15 detection layer as a function of the detection frequency

Failure location unit for failure location of the 3D stacked package IC chip to be tested according to the failure location curve of each comparison detection layer; wherein said standard sample device is said to be the same type of 3D stacked package IC chip to be tested that has not failed (i.e. being intact, undamaged or uncompromised).

- 20 In a third aspect, embodiments of the present application provide a 3D stacked package integrated circuit chip comprising multiple layers of film layers set in a stack, and failure location is performed by the failure location method of the 3D stacked package integrated circuit chip described in any one of the first aspects.

Embodiments of the present application provide a method for locating a failure of a 3D stacked package integrated circuit chip, by defining a plurality of contrast detection layers located at different depths in a standard sample device, and grinding the standard sample device to sequentially grind out the set contrast detection layers; performing a failure treatment on the contrast detection layers after each grinding out of the contrast detection layers, so that the contrast detection layers can be used to simulate the 3D stacked package. After the failure process, the thermal imager detects the phase values of the contrast detection layer at different detection frequencies in the failure state, so that a failure location curve can be determined according to the correspondence between the detection frequency and the phase value; each contrast detection layer corresponds to a failure location curve; when corresponding to the failure of the 3D stacked package IC chip to be tested, it is not necessary to grind the 3D stacked IC chip to be tested, and through matching the database, it is possible to deduce the layer where the failure position is located and achieve the purpose of accurate positioning of failure analysis.

FIG. 1 is a flow chart of a failure location method for a 3D stacked package integrated circuit chip provided by embodiments of the present application; and

FIG. 2 is a flow chart of another failure location method for 3D stacked package integrated circuit chips provided by embodiments of the present application; and

FIG. 3 is a flow chart of another failure location method for 3D stacked package integrated circuit chips provided by embodiments of the present application; and

FIG. 4 is a cross-sectional view of the structure of a 3D stacked package integrated circuit chip provided by an embodiment of the present application; and

Figure 5 is a plot of phase value versus detection frequency for a different depth contrast detection layer provided by an embodiment of the present application.

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The present application is described in further detail below in connection with the accompanying drawings and embodiments. It will be understood that the specific embodiments described herein are intended only to explain the present application and are not intended to limit it. It is also to be noted that, for ease of description, the accompanying drawings show only a portion, but not all, of the structure relating to the present application.

Embodiments of the present application provide a failure location method for a 3D stacked package integrated circuit chip, FIG. 1 is a flow chart of a failure location method for a 3D stacked package integrated circuit chip provided by embodiments of the present application, with reference to FIG. 1, the failure location method for a 3D stacked package integrated circuit chip, comprising.

S110, a plurality of contrast detection layers located at different depths in the standard sample device are identified.

Specifically, the standard sample device is a proper 3D stacked package integrated circuit chip of the same type as the 3D stacked package integrated circuit chip to be tested. The same type is understood to mean that the constituent film layers of the standard sample device and the location of each constituent film layer are the same as the constituent film layers of the 3D stacked package IC chip to be tested and the location of each constituent film layer. The failure of the 3D stacked IC chip can be

understood as the abnormal situation that the membrane layer at a certain location in the 3D stacked IC chip is short-circuited, which affects the normal operation of the 3D stacked IC chip.

For example, the standard sample device consists of a solder ball layer, a PCB substrate,
5 a first contact point layer, an adapter unit, a second contact point layer, and a multilayer top chip set in a laminated order from the bottom to the top, and the comparison detection layer can be all or some of these layers. Alternatively, the standard sample device can be divided into multiple film layers according to the preset thickness, and then all or some of the film layers can be selected as the comparative detection layer.
10 The smaller the predetermined thickness, the greater the number of selected comparative detection layers, the more accurate the failure of the chip to be tested 3D stacked package integrated circuit to locate.

S120, each time after grinding out the contrast detection layer, the phase values corresponding to the different detection frequencies of the exposed contrast detection
15 layer in the failure state are detected by the thermal imager.

Specifically, the rapid growth of advanced packaging applications, complex interconnect schemes, and higher performance power devices presents unprecedented challenges for fault location and analysis. Defective or poorly performing semiconductor devices typically exhibit anomalous distributions of local power losses, leading to local
20 temperature increases. For example, after a short circuit failure of a 3D stacked package IC chip, the location where the short circuit occurs generates higher temperatures that become hot spots. Based on the nature of material heat transfer, the higher temperatures generated at the short circuit location are transferred out over time toward the lower temperature, which in turn is transferred to the outer surface of the device.

Infrared Thermal Camera (Infrared Thermal Camera) is a device that uses infrared thermal imaging technology to convert the image of the temperature distribution of the measured target into a visual image by detecting the infrared radiation of the measured target and using signal processing, photoelectric conversion and other means. Infrared

5 phase-locked thermal imaging detection technology is a new digital nondestructive testing technology, infrared phase-locked thermal imaging detection technology is the combination of infrared thermal imaging technology and digital phase-locked technology, using the intensity of the external excitation source according to the sinusoidal law of excitation of the test piece or material, the temperature change caused on the surface
10 of the component is also a sinusoidal law of change, the surface temperature of the component to load frequency oscillation change, the amplitude and phase and material properties When there is a defect inside the sample structure, the temperature change caused at the defective part of the sample and the corresponding surface without defect will have a difference in amplitude and phase. The difference in amplitude and phase is
15 monitored by an enhanced thermal imager and thus the failure information can be effectively measured, but it is not possible to determine from which location of the film layer this information comes.

Among them, the theoretical relationship between the phase difference of heat transfer and the detection frequency of Lock-in Thermography (LIT) is based on the following
20 determination.

$$\Delta\phi_n = \sum_n \frac{Z_n}{\sqrt{\frac{2 * \lambda_n}{c_{p,n} * \rho_n 2\pi f}}}$$

Where f is the detection frequency, Z_n is the depth, and Δφ_n is the detected phase value. According to the formula, it can be seen that the phase and frequency relationship

has a positive correlation for hotspots at a certain depth, and the corresponding phase values are different for hotspots at different depths and at the same detection frequency.

Based on this, the depth of the hot spot can be inferred from the phase value and frequency relationship. By defining the contrast detection layer, the contrast detection

5 layer is used as the film layer of the 3D stacked package IC chip located at different critical depths. The intact or good 3D stacked package IC chip is used as a standard sample device, and the first defined contrast detection layer is ground from the bottom of the standard sample device, and then the contrast detection layer is failed so that this contrast detection layer is under the failed state. After power is applied to the standard
10 sample device, this contrast detection film layer generates thermal radiation. The phase values corresponding to the different detection frequencies of the exposed contrast detection layer in the failure state are detected by a thermal imager. The standard sample device is continued to be ground to a second defined contrast detection layer, and then the contrast detection layer is failed so that this contrast detection layer is under
15 the failure state. After power is applied to the standard sample device, this contrast detection film layer generates thermal radiation. The phase values corresponding to the different detection frequencies of the exposed contrast detection layer in the failure state are detected by a thermal imager. This is followed analogously until the last defined contrast detection layer is milled, which is subjected to the failure process as well as the
20 detection of the phase angle.

S130, according to the corresponding relationship between the detection frequency and the phase value of each comparison detection layer in the failure state to determine the failure positioning curve of the comparison detection layer.

Specifically, the detection frequencies used in obtaining the correspondence between
25 the detection frequencies and the phase values of the different layers of the contrast

detection layer can be the same or different. Preferably, the same detection frequency is used to obtain the correspondence between the detection frequency and the phase value for different layers of the comparison detection layer. For example, the phase values are collected using frequencies 1Hz, 2Hz, 4Hz and 6Hz. These same detection
5 frequencies can be used to detect the phase values when subsequently locating the failure of the 3D stacked package IC chip to be tested, making the location results more accurate.

In addition, when obtaining the correspondence between the detection frequency and the phase value for different layers of the comparison detection layer, the phase value
10 can be detected several times at the same detection frequency. For example, the phase values are collected three times at 1 Hz, 2 Hz, 4 Hz and 6 Hz. The average value of the three phase values is then used as the phase value at the corresponding detection frequency, which can reduce the detection error and improve the accuracy of the positioning results. A right-angle coordinate system is established with the detection
15 frequency as the horizontal coordinate and the phase value as the vertical coordinate. A pair of detection frequency and phase value is expressed in the right-angle coordinate system as a coordinate point, and the coordinate points are connected to determine the failure location curve. That is, the failure locus curve is a curve that compares the phase value of the detection layer with the detection frequency. Alternatively, after multiple
20 measurements, multiple phase values corresponding to the detection frequency are expressed as coordinate points in the Cartesian coordinate system, and then the test result with converged data is selected as the failure location curve, which can also reduce detection errors and improve the accuracy of the location results.

S140, according to the failure location curve of each comparison detection layer to be
25 tested 3D stacked package integrated circuit chip failure location.

Exemplarily, Table 1 shows the phase values for different contrast detections collected using frequencies 1 Hz, 2 Hz, 4 Hz and 6 Hz. Referring to Table 1, three contrast detection layers located at different depths in the standard sample device are identified. Where the first contrast detection layer is at a greater depth in the standard sample device than the second contrast detection layer is in the standard sample device, where the second contrast detection layer is at a greater depth in the standard sample device than the third contrast detection layer is in the standard sample device. The phase values collected by the first contrast detection layer at the detection frequencies of 1 Hz, 2 Hz, 4 Hz, and 6 Hz are 124.72, 166.25, 224.89, and 258.22, respectively; the phase values collected by the second contrast detection layer at the detection frequencies of 1 Hz, 2 Hz, 4 Hz, and 6 Hz are 55.71, 78.88, 109.47, and 127.06; the phase values collected for the third contrast detection layer at detection frequencies of 1 Hz, 2 Hz, 4 Hz and 6 Hz were 37.74, 50.26, 71.67, 86.56, respectively. the failure localization curves of the phase versus detection frequency for the different contrast detection layers can be determined from these data.

Table 1: Phase values collected using frequencies 1Hz, 2Hz, 4Hz and 6Hz

	First comparison detection layer	Second contrast detection layer	Third contrast detection layer
1Hz	124.72	55.71	37.74
2Hz	166.25	78.88	50.26
4Hz	224.89	109.47	71.67
6Hz	258.22	127.06	86.56

When corresponding to the failure of the 3D stacked package IC chip to be tested, the failed 3D stacked package IC chip to be tested is detected or analysed directly without grinding. For example, if a phase value of 120 is detected at a detection frequency of 4 Hz, it is possible to determine that the location where the failure of the 3D stacked IC chip to be tested occurs is between the first contrast detection layer and the second contrast detection layer, thus enabling inference of the layer and depth where the failure location is located and achieving accurate positioning for failure analysis. In addition, according to the correspondence between the detection frequency and the phase value of each contrast detection layer in the failure state, the failure positioning curve of this contrast detection layer is determined, and the curve can determine the phase value corresponding to the non-experimental acquisition at 3 HZ, 5HZ, etc. Thus, for example, when the detection frequency is 5 Hz for the 3D stacked package IC chip to be tested, the obtained phase value can also be compared with the non-experimental collected phase value corresponding to 5 HZ on the failure location curve, so as to achieve the purpose of inferring the layer and depth where the failure location is located, and to achieve the accurate location of the failure analysis. Preferably, the detection rate of the 3D stacked package IC chip to be tested is one or more of the detection rates of the standard sample device, which can improve the accuracy of the failure location of the 3D stacked package IC chip to be tested.

The failure location method of a 3D stacked package integrated circuit chip provided by embodiments of the present application, by defining a plurality of contrast detection layers located at different depths in a standard sample device and grinding the standard sample device to sequentially grind out the set contrast detection layers; performing a failure treatment on the contrast detection layers after each grinding out of the contrast detection layers, so that the contrast detection layers can be used to simulate the 3D

stacked package After the failure process, the thermal imager detects the phase values of the contrast detection layer at different detection frequencies in the failure state, so that a failure location curve can be determined according to the correspondence between the detection frequency and the phase value; each contrast detection layer corresponds to a failure location curve; when corresponding to the failure of the 3D stacked package IC chip to be tested, it is not necessary to grind the 3D stacked IC chip to be tested, and through matching the database, it is possible to deduce the layer where the failure position is located and achieve the purpose of accurate positioning of failure analysis.

FIG. 2 is a flow chart of another failure location method for 3D stacked packaged integrated circuit chips provided by embodiments of the present application, and with reference to FIG. 2, the failure location method for 3D stacked packaged integrated circuit chips comprises.

S210, a plurality of contrast detection layers located at different depths are determined based on the thickness of the standard sample device.

Specifically, determining a plurality of contrast detection layers located at different depths based on the thickness of the standard sample device may include: dividing the standard sample device into multiple alternative contrast layers of equal thickness based on a predetermined thickness; and spacing the alternative contrast layers to be selected as the contrast detection layers. Exemplarily, the standard sample device is divided into six alternative contrast layers from bottom to top, namely, a first alternative contrast layer, a second alternative contrast layer, a third alternative contrast layer, a fourth alternative contrast layer, a fifth alternative contrast layer, and a sixth alternative contrast layer. The first, third, and fifth alternative contrast layers are selected as the contrast detection

layers. That is, the first alternative layer is the first comparison detection layer described above, the third alternative layer is the second comparison detection layer described above, and the fifth alternative layer is the third comparison detection layer described above.

5 When corresponding to the failure of the 3D stacked IC, for example, at the same detection frequency, the detected phase value is the same as the phase value of the first contrast detection layer, the failure of the 3D stacked IC is located in the first alternative layer; the detected phase value is between the phase values of the first contrast detection layer and the second contrast detection, the failure of the 3D stacked
10 IC is located in the second alternative layer; the detected phase value is the same as the phase value of the second contrast detection, the failure of the 3D stacked IC is located in the third alternative layer; the detected phase value is the same as the phase value of the second contrast detection. The detected phase value is the same as the phase value of the second contrast detection, then the failure of the 3D stacked package
15 IC chip is located in the third alternative layer; the detected phase value is located between the phase values of the second contrast detection layer and the third contrast detection, then the failure of the 3D stacked package IC chip is located in the fourth alternative layer; and so on. In this way, the entire 3D stacked IC chip to be tested can be located by selecting alternative contrast layers as the contrast detection layer at
20 intervals.

S220, grinding out each contrast detection layer in turn, and after short-circuit failure treatment on the surface of the exposed contrast detection layer, the phase values of the exposed contrast detection layer at different detection frequencies are detected by a thermal imager from the side of the standard sample device away from the grinding
25 side.

Specifically, grind the location of the contrast detection layer with different values and perform a failure treatment on the surface of the contrast detection layer to form a failure simulation hot spot. For example, silver glue can be used to create short-circuit points to put the contrast detection layer in a failure state. The phase values of the exposed
5 contrast detection layer at different detection frequencies are then detected by a thermal imager from the side of the standard sample device away from the grinding side.

S230, according to the corresponding relationship between the detection frequency and the phase value of each comparison detection layer in the failure state to determine the failure positioning curve of the comparison detection layer.

10 S240, the phase value of the 3D stacked package integrated circuit chip to be tested is detected by the thermal imager at different detection frequencies; wherein the detection frequency range of the 3D stacked package integrated circuit chip to be tested lies within the detection frequency range of the standard sample device.

S250, according to the corresponding relationship between the detection frequency and
15 the phase value of the 3D stacked package integrated circuit chip to be measured to determine the failure position curve to be measured.

Specifically, the failure position curve to be tested is the curve of the phase value of the 3D stacked package IC chip to be tested as a function of the detection frequency. For example, the same frequencies 1Hz, 2Hz, 4Hz and 6Hz are used to collect the phase
20 values and thus determine the failure position curve to be measured. The way to determine the failure position curve to be tested can be referred to step S130 and is not repeated here. By using the phase values at different detection frequencies to determine the failure position curve to be measured, it is possible to compare the phase values at each frequency with the failure position curve, which can further improve the accuracy
25 of the failure position.

S260, according to the relative distance between the failure positioning curve of each comparison detection layer and the failure position curve to be measured, the position of the failure film layer of the 3D stacked package IC chip to be measured is determined.

Specifically, if the failure location curve to be measured is almost coincident with one of the failure location curves, it can be assumed that the failure of the 3D stacked IC chip to be measured is located at the location of the film layer corresponding to the failure location curve. If the failure location curve is located between the two failure location curves, it can be determined that the failure location of the 3D stacked IC chip under test is located between the film layers corresponding to the two failure location curves.

Moreover, when the failure location curve to be measured is located between two failure location curves, if the distance between the failure location curve to be measured and one of the failure location curves is greater than the distance between the other failure location curve, it can be determined that the location where the failure of the 3D stacked package IC chip to be measured occurred is closer to the film layer corresponding to the closer failure location curve.

FIG. 3 is a flow chart of another failure location method for 3D stacked packaged integrated circuit chips provided by embodiments of the present application, and with reference to FIG. 3, the failure location method for 3D stacked packaged integrated circuit chips comprises.

S310, a plurality of contrast detection layers located at different depths are determined based on the functional film layers that the standard sample device has.

Specifically, determining a plurality of contrast detection layers located at different depths based on the functional film layer that the standard sample device has may include: identifying the functional film layer that the standard sample device has as an

alternative contrast layer; spacing said alternative contrast layer to be selected as the contrast detection layer.

FIG. 4 is a cross-sectional view of the structure of a 3D stacked package integrated circuit chip provided by an embodiment of the present application, and with reference to

5 FIG. 4, the functional film layer of the standard sample device includes: a solder ball layer 100, a PCB substrate 200, a first connected contact point layer 300, an adapter unit 400, a second connected contact point layer 500, and a top chip 600 set in a sequential cascade, wherein the solder ball layer 100 may include a plurality of The first contact point layer 300 may include a plurality of first contact points B (one exemplary
10 drawing), and the second contact point layer 500 may include a plurality of second contact points C (two exemplary drawings). The interval selection of alternative contrast film layers as said contrast detection layer includes: the selection of the solder ball layer 100 located on the side of the PCB substrate 200 away from the adapter unit 400, the first connected contact point layer 300 between the PCB substrate 200 and the adapter
15 unit 400, and the second connected contact point layer 500 between the adapter unit 400 and the top layer chip 600 as the contrast detection layer 10.

Wherein the solder ball layer 100 serves as the first contrast detection layer 11, the first connected contact point layer 300 serves as the second contrast detection layer 12, and the second connected contact point layer 500 serves as the third contrast detection layer
20 13. the depth of the first contrast detection layer 11 in the standard sample device is greater than the depth of the second contrast detection layer 12 in the standard sample device, and the depth of the second contrast detection layer 12 in the standard sample device is greater than the depth of the third contrast detection layer 13 in the standard sample device.

S320, grinding out each contrast detection layer in turn, and after short-circuiting the surface of the exposed contrast detection layer for failure, the phase values of the exposed contrast detection layer at different detection frequencies are detected by a thermal imager from the side of the standard sample device away from the grinding side.

- 5 Specifically, grinding to different locations of the contrast detection layer 10 and failure treatment on the surface of the contrast detection layer 10 creates a failure simulation hot spot. For example, silver glue can be used to create a short circuit point to put the contrast detection layer 10 in a failure state. The phase values of the exposed contrast detection layer at different detection frequencies are then detected by a thermal imager
- 10 from the side of the standard sample device away from the grinding side (the side of the third contrast detection layer 13 away from the second contrast detection layer 12 in Figure 4).

- Select the welding ball layer 100, the first even contact point layer 300 and the second even contact point layer 500 as a way to compare the detection layer 10, to meet the
- 15 interval selected alternative contrast layer as a contrast detection layer 10, while the welding ball layer 100 includes a plurality of welding ball A, the first even contact point layer 300 and the second even contact point layer 500 include a plurality of metal contact points, can use silver glue directly connected Weld ball layer 100 in the two solder ball A can form a short circuit point, the use of silver glue directly connected to the first
- 20 contact point layer 300 in the two first contact point B can form a short circuit point, the use of silver glue directly connected to the second contact point layer in the two second contact point C can form a short circuit point, thus simplifying the failure of the comparative detection layer 10 way to deal with.

S330, according to the corresponding relationship between the detection frequency and the phase value of each comparison detection layer in the failure state to determine the failure positioning curve of the comparison detection layer.

5 S340, the phase value of the 3D stacked package integrated circuit chip to be tested is detected by the thermal imager at different detection frequencies; wherein the detection frequency range of the 3D stacked package integrated circuit chip to be tested lies within the detection frequency range of the standard sample device.

10 S350, according to the corresponding relationship between the detection frequency and the phase value of the 3D stacked package integrated circuit chip to be measured to determine the failure position curve to be measured.

S360, according to the relative distance between the failure positioning curve of each comparison detection layer and the failure position curve to be measured, the position of the failure film layer of the 3D stacked package IC chip to be measured is determined.

Specifically, FIG. 5 is a phase value versus detection frequency diagram of a different
15 depth contrast detection layer provided by an embodiment of the present application. Referring to FIG. 5, in combination with FIG. 4, curve a is the failure location curve corresponding to the solder ball layer 100; curve b is the failure location curve corresponding to the first connected contact point layer 300; curve c is the failure location curve corresponding to the second connected contact point layer 500. If the failure
20 location curve obtained by detecting the 3D stacked IC chip to be tested almost coincides with one of the failure location curves, it can be assumed that the failure location of the 3D stacked IC chip to be tested is located at the location of the film layer corresponding to the failure location curve. If the failure location curve is located between the two failure location curves, it can be determined that the failure location of the 3D stacked IC is
25 located between the film layers corresponding to the two failure location curves. For

example, if the failure location curve is located between curve a and curve b, it can be determined that the failure of the 3D stacked IC chip is located on PCB substrate 200.

In summary, the embodiment of the present application provides a technical solution in which the hot spot depth can be inferred from the phase/frequency relationship graph

5 based on the heat transfer properties of the material. Different key locations of the package can be defined (e.g., solder ball layer 100, PCB substrate 200, first contact point layer 300, adapter unit 400, second contact point layer 500 and top chip 600, where multiple layers of chips can be included above the top chip 600), a good sample is made, ground to different locations, and then the hot spot is simulated by failure (e.g., using
10 silver glue The phase/frequency curve of this depth position can be obtained by applying different frequency measurements of phase values. Then, in the actual failure analysis process, it is only necessary to first take a good piece for database establishment, test the failure sample at different frequencies as well, select the test results with converged data, and then go to the already established phase/frequency relationship graphs for
15 different locations to determine the location of the failure and achieve accurate positioning of the failure layer and location. It should be noted that for different products, different phase/frequency relationship graphs need to be established separately for use in actual failure analysis.

Embodiments of the present application also provide a failure location device for a 3D
20 stacked package integrated circuit chip for performing the failure location method for a 3D stacked package integrated circuit chip described in any of the above embodiments, comprising.

A contrast detection layer determination unit for determining a plurality of contrast detection layers located at different depths in a standard sample device.

A phase value detection unit for detecting the phase values corresponding to the different detection frequencies of said contrast detection layers exposed in the failure state after grinding out each of said contrast detection layers in turn.

5 A failure positioning curve determination unit for determining the failure positioning curve of each comparison detection layer based on the correspondence between the detection frequency and the phase value in the failure state of that comparison detection layer.

Failure location unit for failure location of the 3D stacked package IC chip to be tested according to the failure location curve of each comparison detection layer; wherein said standard sample device is said to be the same type of 3D stacked package IC chip to
10 be tested that has not failed.

Referring to FIG. 4, embodiments of the present application also provide a 3D stacked package integrated circuit chip including multiple layers of stacked set of film layers for failure location by the failure location method of the 3D stacked package integrated circuit chip described in any of the above embodiments. Having the same technical effect,
15 it is not repeated here.

Note that the foregoing is only a preferred embodiment of the present application and the technical principles employed. It will be understood by those skilled in the art that the present application is not limited to the particular embodiments described herein, and that various obvious variations, readjustments and substitutions can be made to those
20 skilled in the art without departing from the scope of protection of the present application. Thus, although the present application is described in some detail by the above embodiments, the present application is not limited to the above embodiments, but may include more other equivalent embodiments without departing from the conception of the present application, the scope of which is determined by the scope of the appended
25 claims.

Claims

1. A method for failure localization of a 3D stacked package integrated circuit (IC) chip (i.e. device, chip, sample device, standard sample device or sample chip),
5 the method comprising
- determining a plurality of contrast detection layers located at different depths in a standard sample device;
 - detecting, by a thermal imager, phase values corresponding to different detection frequencies of said contrast detection layer in a failure state, said
10 contrast detection layer being exposed by grinding;
 - determining a failure locus curve for each comparison detection layer based on correspondence between the detection frequencies and the phase values for comparing said contrast detection layer in the failure state, said failure locus curve being a curve of the phase value of said contrast
15 detection layer as a function of the detection frequencies; and
 - locating failures of the 3D stacked package IC chip or the sample standard device according to the failure location curve of each said contrast detection layer; wherein said standard sample device is the same type of an intact 3D stacked package IC chip without any failure.
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2. The method for locating failures in 3D stacked packaged integrated circuit chips according to claim 1, characterized in that said determining a plurality of contrast detection layers located at different depths in a standard sample device, comprising determining a plurality of contrast detection layers located at different

depths according to a thickness of said standard sample device; or the functional film layers of said standard sample device.

3. The method for locating failure of a 3D stacked package integrated circuit chip according to claim 1, characterized in that said detection exposes the phase values corresponding to different detection frequencies of said contrast detection layer in the failure state, comprising a step of detecting the phase values of the exposed contrast detection layer at different detection frequencies by a thermal imager from a side of said standard sample device distant away from a grinded side of said standard sample device.

4. The method for locating failure of a 3D stacked package integrated circuit chip according to claim 2, characterized in that determining a plurality of contrast detection layers located at different depths based on the thickness of said standard sample device, comprising a step of dividing said standard sample device into multiple alternative contrast layers according to a predetermined thickness; and a further step of selecting said at least one of the multiple alternative contrast layers as said contrast detection layers having intervals with said at least one of the multiple alternative contrast layers.

5. The method for locating failure of a 3D stacked package integrated circuit chip according to claim 2, characterized in that said determining a plurality of contrast detection layers located at different depths based on the functional film layers that said standard sample device has, comprising a step of identifying a functional film

layer of said standard sample device to be an alternative contrast layer; and
setting said alternative contrast layer apart to be said contrast detection layer.

6. The failure location method for 3D stacked packaged integrated circuit chips
according to claim 5, characterized in that said functional film layer of said
standard sample device comprises a solder ball layer, a PCB substrate, a first
connected contact point layer, an adapter unit, a second connected contact point
layer and a top chip set in a sequential cascade; said setting said alternative
contrast layer apart to be said contrast detection layer comprising a step of
selecting the solder ball layer located on a side of the PCB substrate distant away
from said adapter unit, the first connected contact point layer between the PCB
substrate and the adapter unit, and the second connected contact point layer
between said adapter unit and said top layer chip as said contrast detection layers.

7. The failure location method for 3D stacked packaged integrated circuit chips
according to claim 1, characterized in that before said failure location of the 3D
stacked packaged integrated circuit chips to be tested or examined according to
the failure location curve of each comparison detection layer, further comprising:
- detecting, by a thermal imager, phase values of said 3D stacked packaged
integrated circuit chip tested at different detection frequencies, the
detection frequency range for said 3D stacked packaged integrated circuit
chip to be tested occurring within the detection frequency range for said
standard sample device; and
 - determining the failure position curve to be tested according to
correspondence between the detection frequency and the phase value of

said 3D stacked package integrated circuit chip to be tested, said failure position curve to be tested being a curve of the phase value of the 3D stacked package integrated circuit chip to be tested with the different detection frequencies.

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8. The failure location method for 3D stacked package integrated circuit chips according to claim 7, characterized in that said failure location of the 3D stacked package integrated circuit chips to be tested according to the failure location curve of each comparison detection layer, comprising:

10 determining a position or location of the failure film layer of said 3D stacked package IC chip to be tested based on a relative distance between the failure positioning curve of each comparison detection layer and said failure position curve.

- 15 9. A failure location device for a 3D stacked packaged integrated circuit chip, characterized in that the failure location method for performing the 3D stacked packaged integrated circuit chip of any one of claims 1-8, the device comprising:

20 ➤ a contrast detection layer determination unit for determining a plurality of contrast detection layers located at different depths in the standard sample device.

➤ a phase value detection unit for detecting, by a thermal imager, the phase values corresponding to different detection frequencies of said contrast detection layers exposed in the failure state, after grinding off each of said contrast detection layers in turn;

- 5 ➤ a failure positioning curve determination unit for determining a failure positioning curve of each comparison detection layer based on the correspondence between the detection frequency and the phase value in the failure state of that comparison detection layer, said failure positioning curve being a curve of the phase value of the comparison detection layer as a function of the detection frequency; and
- 10 ➤ a failure location unit for identifying failure location of the 3D stacked package IC chip to be tested according to the failure location curve of each comparison detection layer, said standard sample device being said to be the same type of 3D stacked package IC chip to be tested that is intact or not failed.
10. A 3D stacked package integrated circuit chip, characterized in that it includes a multilayer stacked set of film layers, failure location by the failure location method of the 3D stacked package integrated circuit chip of any one of preceding claims 1-8.
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