

CLAIMS

What is claimed is:

1. A waveform processor comprising:
 - one or more data storage devices that include:
 - a first memory for storing a plurality of master instructions, wherein a master instruction comprises a plurality of digital data fields and the master instructions have a defined order; and
 - a second memory for storing a plurality of digital waveforms;
 - a first sequencer comprising a first plurality of logic blocks configured to access the first memory and sequentially execute the master instructions according to their defined order, the first sequencer having a first digital output configured to output digital values based at least in part on results of executing the master instructions;
 - a second sequencer coupled to the first sequencer and configured to receive values from the first digital output, the second sequencer comprising a second plurality of logic blocks configured to:
 - access the second memory;
 - generate analog waveforms at least in part by transforming one of the plurality of digital waveforms according to one or more of the digital values received from the first sequencer; and
 - output the generated analog waveforms to an external system; and
 - a waveform analyzer comprising a third plurality of logic blocks configured to integrate analog waveforms received from the external system and to output results of said integration to the first sequencer.
2. The waveform processor of claim 1,
 - wherein the one or more data storage devices further include a third memory for storing a plurality of waveform instructions, wherein a waveform instruction comprises a plurality of digital data fields and the waveform instructions have a defined order, and
 - wherein the second plurality of logic blocks of the second sequencer are further configured to:
 - access the third memory and sequentially execute the waveform instructions according to their defined order; and

generate said analog waveforms according to the executed waveform instructions.

3. The waveform processor of claim 2, wherein the waveform instructions include at least a first branch instruction and wherein the second sequencer is further configured to identify a non-sequential waveform instruction of the plurality of waveform instructions to execute subsequent to the first branch instruction based at least in part on a digital signal received by the second sequencer from the first sequencer.

4. The waveform processor of claim 2, wherein the second plurality of logic blocks of the second sequencer are further configured to repeatedly execute the plurality of waveform instructions according to their defined order.

5. The waveform processor of claim 1, wherein the master instructions include at least a first branch instruction and wherein the first sequencer is further configured to identify a non-sequential master instruction of the plurality of master instructions to execute subsequent to the first branch instruction based at least in part on a digital signal received by the first sequencer.

6. The waveform processor of claim 5, wherein the digital signal received by the first sequencer is received by the first sequencer from the waveform analyzer and comprises a result of said integration by the waveform analyzer.

7. The waveform processor of claim 5, wherein the first sequencer is further configured to output a digital instruction to the second sequencer based at least in part on the result of said integration received by the first sequencer from the waveform analyzer.

8. The waveform processor of claim 1, wherein the integration of analog waveforms by the waveform analyzer is triggered by execution of a master instruction by the first sequencer.

9. The waveform processor of claim 1, wherein the external system is a quantum

system including a qubit, and wherein the generated analog waveforms are designed to rotate a state of the qubit.

10. The waveform processor of claim 1, wherein the first sequencer is further configured with a second digital output configured to output digital values based at least in part on results of executing the master instructions, the waveform processor further comprising:

a third sequencer coupled to the first sequencer and configured to receive values from the second digital output, the third sequencer configured to output digital values according to one or more of the digital values received from the first sequencer.

11. The waveform processor of claim 1, wherein transforming one of the plurality of digital waveforms by the second sequencer comprises performing a linear transformation of the one of the plurality of digital waveforms based at least in part on the one or more digital values received from the first sequencer.

12. The waveform processor of claim 1, wherein the one or more data storage devices, the first sequencer, the second sequencer and the waveform analyzer are assembled on a single substrate.

13. The waveform processor of claim 1, wherein the first sequencer, the second sequencer and the waveform analyzer are embodied in a field-programmable gate array.

14. The waveform processor of claim 1, wherein the first sequencer, the second sequencer and the waveform analyzer are embodied in an application specific integrated circuit.

15. The waveform processor of claim 1, wherein the first sequencer, the second sequencer and the waveform analyzer are configured to receive a common clock signal.

16. The waveform processor of claim 1, wherein the second sequencer is configured to generate the analog waveforms as comprising IQ waveform pairs.

17. The waveform processor of claim 1, wherein the second sequencer is configured to generate the analog waveforms as single-sideband modulated waveforms.
18. The waveform processor of claim 1, wherein:
the second sequencer comprises a digital-to-analog converter; and
the waveform analyzer comprises an analog-to-digital converter.
19. A system comprising the waveform processor of claim 1 and a superconducting qubit coupled to the waveform processor.
20. A system comprising a plurality of instances of the waveform processor of claim 1 communicatively coupled to one another.
21. A method comprising:
selecting, by a first sequencer that comprises a first plurality of logic blocks, a first master sequence instruction from a plurality of master sequence instructions stored in a first memory of one or more data storage devices, wherein a master sequence instruction comprises a plurality of digital data fields and the master instructions have a defined order;
executing, by the first sequencer, the first master sequence instruction;
outputting, by the first sequencer, one or more digital values to a second sequencer comprising a digital-to-analog converter and a second plurality of logic blocks;
generating, by the second sequencer, a first analog waveform that has characteristics at least in part by transforming one of the plurality of digital waveforms according to the one or more digital values received from the first sequencer;
applying the first analog waveform to a system;
integrating, by a waveform analyzer comprising a first analog-to-digital converter and a third plurality of logic blocks assembled on a substrate, a first received analog waveform from the system;
providing, by the waveform analyzer, a result of the integration to the first

sequencer; and

executing, by the first sequencer, a second master sequence instruction of the plurality of master sequence instructions based on the received result from the waveform analyzer.

22. The method of claim 21, further comprising:

computing, by the first sequencer, an internal result based in part on the result of the integration;

providing, by the first sequencer, the internal result to the second sequencer; and

outputting, by the second sequencer, a second analog waveform to the system based in part on the internal result.

23. The method of claim 21, wherein the system is a quantum system including a qubit, and wherein the first analog waveform is designed to rotate a state of the qubit.

24. The method of claim 21, further comprising:

identifying, by the first sequencer, a non-sequential master instruction of the plurality of master instructions to execute subsequent to the first master sequence instruction based at least in part on the received result from the waveform analyzer.