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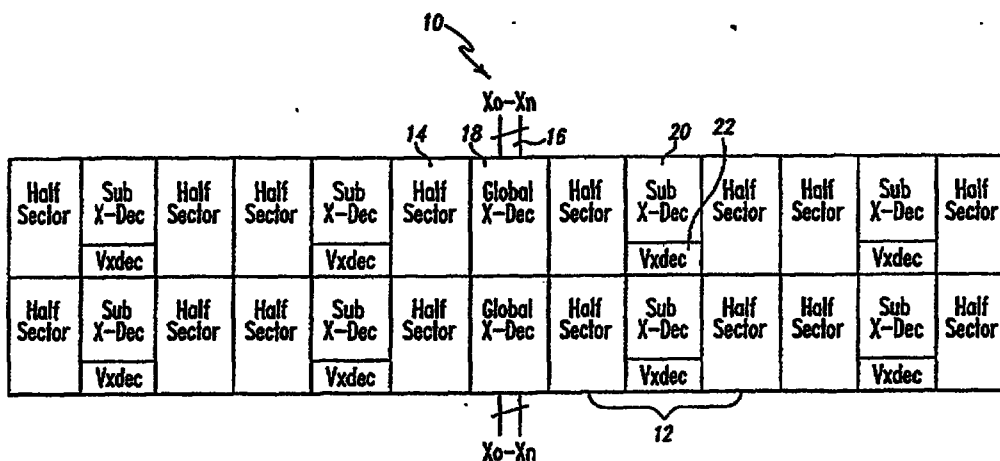
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(54) Title: FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT



(57) Abstract: The present invention discloses a memory wordline decoder that includes plurality of pre-decoded address lines that are electrically connected with a global x-decoder. A sub x-decoder is electrically connected with the global x-decoder for receiving electrical control signals from the global x-decoder. A memory sector is electrically connected with the sub x-decoder. The global x-decoder selectively controls the sub x-decoder to select a plurality of wordlines in the memory sector. A vertical x-decoder is electrically connected with the global x-decoder and the sub x-decoder. The vertical x-decoder is used to select a predetermined wordline by the global x-decoder during operation.

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