(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 April 2005 (21.04.2005)

PCT

(10) International Publication Number
WO 2005/036640 A1

(51) International Patent Classification[7]: H01L 21/8238

(21) International Application Number:
PCT/US2004/022508

(22) International Filing Date: 15 July 2004 (15.07.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/663,621 16 September 2003 (16.09.2003) US

(71) Applicant *(for all designated States except US)*: **FREESCALE SEMICONDUCTOR, INC.** [US/US]; 6501 William Cannon Drive West, Austin, Texas 78735 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **STEIMLE, Robert, F.** [US/US]; 7928 Eldorado Drive, Austin, TX 78737 (US). **MURALIDHAR, Ramachandran** [US/US]; 10601 Pickfair Drive, Austin, Texas 78750 (US). **PAULSON, Wayne, M.** [US/US]; 5821 W. Park Ave., Chandler, AZ 85226 (US). **RAO, Rajesh, A.** [IN/US]; 12524 Zeller Lane, Austin, TX 78753 (US). **WHITE, Bruce, E.** [US/US]; 3204 Bluebell Bend Cove, Round Rock, TX 78664 (US). **PRINZ, Edward, J.** [DE/US]; 6105 Utica Cove, Austin, TX 78739 (US).

(74) Agents: **KING, Robert, L.** et al.; Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, Texas 78729 (US).

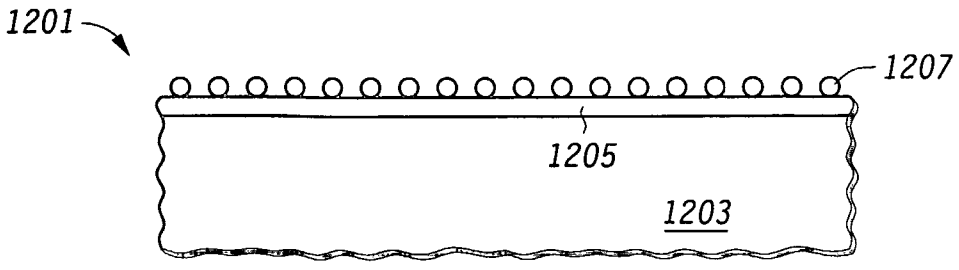
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: SEMICONDUCTOR DEVICE WITH NANOCLUSTERS




(57) Abstract: A process of forming a device with nanoclusters. The process includes forming nanoclusters (e.g. silicon nanocrystals) and forming an oxidation barrier layer over the nanoclusters to inhibit oxidizing agents from oxidizing the nanoclusters during a subsequent formation of a dielectric of the device. At least a portion of the oxidation barrier layer is removed after the formation of the dielectric. In one example, the device is a memory wherein the nanoclusters are utilized as charge storage locations for charge storage transistors of the memory. In this example, the oxidation barrier layer protects the nanoclusters from oxidizing agents due to the formation of gate dielectric for high voltage transistors of the memory.

WO 2005/036640 A1