ABSTRACT

A METHOD OR FORMING A HIGH PERFORMANCE AND LOW COST CMOS DEVICE

A method of fabricating a CMOS device with reduced processing costs as a result of a reduction in photolithographic masking procedures, has been developed. The method features formation of L shaped silicon oxide spacers on the sides of gate structures, with a vertical spacer component located on the sides of the gate structure, and with horizontal spacer components located on the surface of the semiconductor substrate with a thick horizontal spacer component located adjacent to the gate structures, while a thinner horizontal spacer component is located adjacent to the thicker horizontal spacer component. After formation of a block out shape in a PMOS region of the CMOS device, a high angle implantation procedure is used to form a P type halo region in a top portion of the NMOS region, followed by another implantation procedure performed at lower implant angles, resulting in an N type LDD region in a portion of the NMOS region underlying the thicker horizontal spacer component, and resulting in an N type heavily doped source/drain region in a portion of the NMOS underlying the thinner horizontal spacer component. Another block out shape, and another series of similar implantation procedures is performed to create the halo, LDD and source/drain regions in the PMOS region. After formation of a photoresist block out shape on specific CMOS regions, a composite insulator spacer is formed on the sides of gate structures not covered by the photoresist shape, followed by formation of metal silicide on the gate structures and source/drain regions not covered by the photoresist block out shape.

FIGURE 10