

MICROSTRUCTURE PROVIDED WITH A MAGNETIC
ANTENNA OR A MAGNETIC DETECTION ELEMENT

The present invention concerns a microstructure which is formed of a semiconductor substrate in which an electronic circuit is integrated and which includes a magnetic antenna or a magnetic detection element connected to this electronic circuit. The magnetic antenna or magnetic detection element
5 includes a coil formed by a conductive wire.

As the technological field of magnetic sensors and transponders comprising an antenna sensitive to the magnetic field of an electromagnetic signal develops, those skilled in the art seek to reduce the dimensions of such sensors and transponders. With this aim, it has been proposed that an
10 antenna in the form of a spiral coil be formed directly on one face of a semiconductor substrate above a passivation layer covering the active region of the electronic circuit integrated in the semiconductor substrate.

One object of the invention is to provide a microstructure with a magnetic antenna or a magnetic detection element having maximum efficiency
15 and sensitivity for given dimensions of the semiconductor substrate in which the electronic circuit is integrated.

The present invention thus concerns a microstructure formed of a semiconductor substrate, in which is integrated an electronic circuit, and of a magnetic antenna or a magnetic detection element connected to this
20 electronic circuit and including a coil formed by a conductive wire, this microstructure being characterised in that the coil includes a first portion arranged on the side of an upper face of said substrate and a second portion arranged on the side of a lower face of the substrate, these first and second portions being connected by a first opening made in said substrate
25 between its upper and lower faces.

A second opening made in the semiconductor substrate is preferably provided for returning the first and second ends of said second portion of said coil on the side of the upper face of the semiconductor substrate where the electronic circuit is arranged and its two electric connection pads to said
30 magnetic antenna or to said magnetic detection element, respectively by said first and second openings.

As a result of the various aforementioned features of the invention, the magnetic antenna or magnetic detection element has maximum efficiency for given dimensions of a microstructure, i.e. of the semiconductor which forms it.
35 The two large faces of the microstructure are used to have a maximum

number of turns having large efficient cross-sections. Next, the fact of providing an opening passing through the semiconductor substrate allows electric connections via the edge of the microstructure, i.e. via the lateral surface of the semiconductor substrate, which are difficult to make and
5 increase the manufacturing cost, to be avoided.

According to various preferred embodiments of the invention, two openings are provided either in the central region, or in the peripheral region of the semiconductor substrate.

Other advantages and particular features of the invention will be
10 described in more detail hereinafter with the aid of the following description, which is made with reference to the annexed drawings, in which:

- Figures 1a and 1b are respectively two upper and lower plane views of a microstructure according to the invention;
- Figures 2a and 2b, respectively 3a and 3b are similar views to Figures
15 1a and 1b and concern respectively second and third embodiments of the invention;
- Figure 4 is a partial cross-section along the line IV-IV of Figure 3b;
- Figure 5 shows an alternative embodiment of Figure 4;
- Figure 6 is a plane view of the upper face of a microstructure
20 according to a fourth embodiment;
- Figure 7 is a partial cross-section along the line VII-VII of Figure 6;
- Figures 8a and 8b are plane views of the upper and lower faces of a microstructure according to a fifth embodiment;
- Figures 9a and 9b shows schematically an opening allowing an electric
25 connection between the upper and lower faces of a semiconductor substrate of a microstructure according to the invention;
- Figure 10 is a similar view to Figure 9b and shows an alternative embodiment wherein external passivation layers are provided arranged on either side of the semiconductor substrate;
- 30 - Figure 11 shows an alternative embodiment of Figure 9b;
- Figures 12a and 12b are plane views of the upper and lower faces of a sixth embodiment of the invention.

With reference to Figures 1a and 1b, a first embodiment of a microstructure according to the invention will be described hereinafter. This
35 microstructure includes a semiconductor substrate 2 and a magnetic antenna or a magnetic detection element comprising a coil 4 which is formed by a conductive wire 6. A first portion 8 of coil 4 is arranged on upper face 10 of

semiconductor substrate 2. It will be noted that the semiconductor substrate includes conventional passivation and metallisation layers provided on the surface of an electronic circuit integrated in this substrate. A second portion 9 of coil 4 is arranged on lower face 11 of substrate 2.

5 In order to connect electrically the two portions 8 and 9 of coil 4, in accordance with the invention a first opening 14 is made in substrate 2. The electric junction 26 situated at the centre of opening 14 is used to connect electrically the two portions 8 and 9 of coil 4. Electric wire 6 begins on upper face 10 by an end contact bump 20 situated in the central region of face 10.
10 Next, wire 6 develops in a flat spiral as far as opening 14 where it widens out to form electric junction 26. On lower face 11, wire 6 also defines a flat spiral starting from junction 26 and going as far as electric junction 27 situated at the centre of a second opening 16 which is itself situated in the central region of face 11. A last segment of wire 6 electrically connects junction 27 to end
15 contact bump 21 situated in the central region of upper face 10. End contact bumps 20 and 21 are respectively connected to two electric contact pads of the electronic circuit arranged in semiconductor substrate 2.

Opening 14 made in substrate 2 is used to connect electrically first and second portions 8 and 9 of coil 4 arranged respectively on the side of upper
20 face 10 and on the side of lower face 11 of substrate 2. Thus, first opening 14 is an opening passing through substrate 2, which allows an electric junction 26, electrically connecting upper face 10 and lower face 11 of substrate 2, to be arranged at the centre thereof.

The references described hereinbefore will not be described again in
25 detail in the embodiments described hereinafter.

The second embodiment described in Figures 2a and 2b differs essentially from the first embodiment in that end contact bumps 20 and 21 are situated in the peripheral region of semiconductor substrate 2. Given that the electric contact pads for the external connection terminals or bumps are
30 generally situated on the periphery of semiconductor substrate 2, this second embodiment is advantageous compared to the first embodiment described hereinbefore.

Figures 3a and 3b show a third embodiment which differs essentially from the first two embodiments in that the two openings 14 and 16 are
35 situated in the peripheral region of substrate 2. Thus, no opening is provided in the central region of substrate 2. Consequently, a compact design of the electronic circuit can be provided, the two openings 14 and 16 not requiring

any particular design other than a conventional design to be provided in particular in the event that coil 4 is only arranged on upper face 10, as is the case in the prior art.

5 In order for openings 14 and 16 to be on the periphery of substrate 2, a conductive path 30 is provided on lower face 11 of the substrate, said path electrically connecting two contact bumps 32 and 33 arranged on the side of lower face 11, above surface 11A of a passivation layer 35 covering face 11 and conductive path 30. As shown in Figure 4, conductive path 30 is preferably arranged in a channel 37 made in lower face 11 of substrate 2.

10 However, in a variant shown in Figure 5, conductive path 30 may be arranged at the surface of lower face 11, thus defining a rectilinear bump. Consequently, conductive wire 6 has a raised portion in the region in which it is superposed with conductive path 30.

Figures 6 and 7 show a fourth preferred embodiment of the invention.
15 This fourth embodiment differs essentially from the third embodiment described hereinbefore in that end contact bump 20 of wire 6, arranged on the side of upper face 10 of substrate 2 in the central region thereof, is connected to an electric contact pad 22 situated in the peripheral region of substrate 2 at the level of metallisation 44. An insulating (or passivation)
20 layer 42 is provided above metallisation 44 of the electronic circuit integrated in substrate 2. At the surface of insulating layer 42 is arranged a conductive path 40 one end of which defines an electric contact pad with a corresponding pad of a metallisation 44 while the other end define an electric contact pad with end contact bump 20. The electric connection between
25 contact bump 20 and conductive path 40 is achieved through an opening provided in passivation layer 46 which covers conductive path 40 and face 10. Pad 22 defined by the end of path 40 situated on the periphery of substrate 2 is connected to metallisation 44 and more particularly to the corresponding pad of the metallisation by an opening provided for this
30 purpose in insulating layer 42.

It will be noted that conductive path 40 can be formed at the level of a metallisation or another layer made of conductive material of the electronic circuit used to establish the interconnections thereof; in particular in a technology with several layers of levels of interconnection.

35 Thus, in this fourth embodiment, the two openings 14 and 16, as well as the two electric contact pads of the electric circuit to coil 4 are situated in

the peripheral region of semiconductor substrate 2. This thus allows an entirely conventional design for the electronic circuit integrated in substrate 2.

A fifth embodiment is described in Figures 8a and 8b, which differs essentially from the other embodiments described hereinbefore in that the two openings 14 and 17 are both situated in the central region of substrate 2. The second opening 17 has the peculiarity of not passing through substrate 2 entirely, but stopping at the level of metallisation 44 of the electronic circuit integrated in substrate 2 on the side of upper face 10. The base of opening 17 made in substrate 2 is defined by a contact pad 23 of metallisation 44. On the side of lower face 11 of substrate 2, end contact bump 21 of wire 6 is electrically connected to contact pad 23 by a conductive path 50 arranged in a similar way to Figure 4 or 5. This conductive path 50 is covered by a passivation layer 35 whose external surface 11A carries portion 9 of coil 4. Thus, wire 6 and conductive path 50 are electrically insulated from each other.

This fifth embodiment can be particularly advantageous when semiconductor substrate 2 is relatively fragile and openings situated in its peripheral region could generate zones of lower resistance. Thus, in order to prevent substrate 2 breaking in its peripheral region, the two openings 14 and 17 are provided in the central region of substrate 2. It will be noted that opening 17 in the particular arrangement shown in Figures 8a and 8b may not pass through substrate 2 entirely given that this opening is used to connect one end 21 of coil 4 to a contact pad 23 of the metallisation of the electronic circuit.

Figures 9a and 9b show schematically two respectively plane and cross-sectional views of an aforementioned opening 14, 16 between lower face 11 and upper face 10 of semiconductor substrate 2. Opening 14, 16 has a truncated cross-section. It is obtained by anisotropic micromachining on lower side 11 of substrate 2. Wire 6 ends inside opening 14, 16 where it preferably widens out to define an electric junction 26, 27 situated in the central region of opening 14, 16. On the side of upper face 10, wire 6 has an initial pad covering the hole of the opening in this face and also defining electric junction 26, 27. Anisotropic micromachining generating a truncated cross-section of opening 14, 16 has two advantages. First, this micromachining can be relatively rapid. Secondly, the electric junction can be easily made without it being necessary to fill a hole, in particular with vertical walls, with an electrically conductive material.

Figure 10 shows opening 17 of the fifth embodiment shown in Figures 8a and 8b. It will be noted that conductive path 50 situated on the side of lower face 11 is electrically connected, through opening 17 by an electric junction 23 similar to junctions 26 and 27 described hereinbefore, to a
5 contact pad of the level of metallisation 44 of the integrated circuit. Lower passivation and upper passivation layers 35 and 42 are provided and cover respectively conductive path 50 and metallisation 44.

Figure 11 shows an alternative embodiment of openings 14 and 16 of the preceding Figures. In this variant, openings 14' and 16' differ in that a
10 hole 54 remains present after the electric junction between lower face 11 and upper face 10 have been made.

Finally, Figures 12a and 12b show respectively upper and lower faces 10 and 11 of a sixth embodiment of the invention. This sixth embodiment differs from the preceding embodiments in that the two openings 14 and 16
15 are respectively situated at two locations in the inner region of substrate 2 and in that contact bumps 20 and 21 are situated in the peripheral region of substrate 2, without requiring any conductive path crossing wire 6 of coil 4 as is the case in particular for the fifth embodiment described hereinbefore. The antenna or detection element thus defines four secondary spiral coils two
20 of which are situated on upper face 10 and the two others on lower face 11.

As this sixth embodiment shows, several alternative arrangements of coil 4 on upper face 10 and lower face 11 of substrate 2 can be provided by those skilled in the art without departing from the scope of the present invention.

25 In order to have a sensitive and efficient magnetic antenna or magnetic detection element available, conductive wire 6 is relatively thick, preferably greater than 10 μ m. This in no way excludes lower thicknesses for certain applications. The growth of the external parts of the two portions 8 and 9 of conductive wire 6 can advantageously be achieved by galvanic deposition on
30 both sides of semiconductor substrate 2.



CLAIMS

1. Microstructure formed of a semiconductor substrate (2), in which is integrated an electronic circuit, and of a magnetic antenna or a magnetic detection element connected to this electronic circuit and including a coil (4) formed by a conductive wire (6), characterised in that said coil (4) includes a
5 first portion (8) arranged on the side of an upper face (10) of said substrate and a second portion (9) arranged on the side of a lower face (11) of said substrate, these first and second portions being electrically connected by a first opening (14) made in said substrate between its upper and lower faces.
- 10 2. Microstructure according to claim 1, wherein said electronic circuit is arranged on said upper face (10) of said substrate (2), characterised in that a second opening (16) is provided in said substrate between its upper and lower faces (10, 11), the first and second ends of said second portion (9) of said coil (4) being returned on the side of the upper face (10)
15 respectively by said first and second openings.
3. Microstructure according to claim 2, characterised in that said first and second openings are situated in the peripheral region of said substrate (2).
4. Microstructure according to claim 2, characterised in that said
20 first and second openings (14, 16) are situated in the central region of said semiconductor substrate (2), each of the two portions (8, 9) of said coil (4) defining a partial spiral coil which surrounds said first and second openings.
5. Microstructure according to claim 3 or 4, characterised in that a
25 conductive path (30, 50) partially forming the second portion (9) of said coil (4) crosses in superposition turns defined by said second portion, this path being arranged under these turns and insulated therefrom by an insulating or passivation layer.
6. Microstructure according to claim 2, characterised in that each of
30 the two portions (8, 9) of said coil (4) defines two secondary spiral coils which are juxtaposed with each other, said first and second openings (14, 16) being respectively situated at the centre of two secondary coils situated on the upper face (10), and the lower face (11) respectively, of said semiconductor substrate (2).
7. Microstructure according to claim 6, characterised in that said
35 coil (4) is arranged so that the two ends thereof (20, 21) are arranged on



the side of said upper face (10) and are situated in the peripheral region of said semiconductor substrate (2).

8. Microstructure according to any of claims 2 to 6, characterised in that one end (20) of said coil (4) situated on the side of said upper face (10) is in a central region of said first portion (8) of said coil, this end being
5 connected to a contact pad (22), provided at the level of the metallisation (44) of said electronic circuit and situated in a region external to said first portion, by a conductive path (40) arranged between two insulating and/or passivation layers which are situated between said metallisation (44) and
10 said first portion (8) of said coil (4).

9. Microstructure according to any of the preceding claims, characterised in that said openings (14, 16, 17) are obtained by anisotropic micromachining from said lower face (11) of the substrate (2), these openings having a truncated cross-section, the large base of such cross-
15 section being situated on said lower face.

10. Microstructure according to any of the preceding claims, characterised in that said conductive wire (6) of said coil (4) has a thickness greater than 10 μm , the external parts of the two portions (8, 9) of said coil (4) being obtained by galvanic growth.