CLAIMS

1. A device, comprising:

an interposer having a first quantum chip and a second quantum chip; and

an electrical conductor comprising at least one of a pogo pin or a land grid array; and

a readout resonator of the first quantum chip routed to an inner portion of the interposer, wherein the inner portion is located between the first quantum chip and the second quantum chip., and the readout resonator is coupled to a printed circuit board by the electrical conductor.

2. The device according to the preceding of claim 1, further comprising:

at least two connection buses coupling the first quantum chip and the second quantum chip, the at least two connection buses located on the inner portion, wherein the readout resonator is located between the at least two connection buses.

3. The device according to the preceding of claim 2, wherein the readout resonator is coupled to a printed circuit board by an electrical conductor that is skew to the at least two connection buses.

4. The device according to the preceding of claim, wherein the electrical conductor is a pogo pin, and 3, wherein the printed circuit board is substantially parallel to the interposer and opposes a front side of the interposer.

5. The device according to of claim 3, wherein the electrical conductor is a land grid array, and wherein the printed circuit board is substantially parallel to the interposer and opposes a front side of the interposer.

6. The device according to of claim 3, further comprising a second electrical conductor, wherein the second electrical conductor is a through-silicon via, and wherein the printed circuit board is substantially parallel to the interposer and opposes a back side of the interposer.

7. The device ~~according to any~~ of ~~the preceding claims and with features of~~ claim 2, further comprising:

~~a~~ a second readout resonator of the first quantum chip routed to a peripheral portion of the interposer, the peripheral portion circumscribing the first quantum chip and the second quantum chip.

8. ~~A method, comprising:~~

~~bonding a first quantum chip and a second quantum chip to an interposer; and~~

~~routing a readout resonator of the first quantum chip to an inner portion of the interposer, the inner portion located between the first quantum chip and the second quantum chip.~~

~~9. The method according to the preceding claim, further comprising:~~

~~coupling the first quantum chip and the second quantum chip via at least two connection buses, the at least two connection buses located on the inner portion, wherein the readout resonator is located between the at least two connection buses.~~

~~10. The method according to the preceding claim, further comprising:~~

~~coupling the readout resonator to a printed circuit board via an electrical conductor that is skew to the at least two connection buses.~~

~~11. The method according to the preceding claim, wherein the electrical conductor is a pogo pin, and wherein the printed circuit board is substantially parallel to the interposer and opposes a front side of the interposer.~~

~~12. The method according to claim 10, wherein the electrical conductor is a land grid array, and wherein the printed circuit board is substantially parallel to the interposer and opposes a front side of the interposer.~~

~~13. The method according to claim 10, wherein the electrical conductor is a through-silicon via, and wherein the printed circuit board is substantially parallel to the interposer and opposes a back side of the interposer.~~

~~14. The method according to any of the preceding claims 9 to 13, further comprising:~~

~~routing a second readout resonator of the first quantum chip to a peripheral portion of the interposer, the peripheral portion circumscribing the first quantum chip and the second quantum chip.~~

~~15.~~ An apparatus, comprising:

~~a~~ a substrate having one or more qubit chips; and

~~one~~ one or more resonators coupled to qubits on the one or more qubit chips, the one or more resonators routed to one or more inner regions of the substrate~~,~~ such that a routed path between the qubits on the one or more qubit chips and the one or more inner regions positioned between one or more pairs of adjacent chips of the one or more qubit chips~~—~~ is unobstructed.

~~16.~~ 9. The apparatus ~~according to the preceding~~ of claim 8, wherein the one or more pairs of adjacent chips of the one or more qubit chips are coupled together via buses positioned on the one or more inner regions, wherein the one or more resonators are positioned between the buses.

~~17.~~ 10. The apparatus ~~according to the preceding~~ of claim 9, wherein the one or more resonators are coupled to a printed circuit board via one or more conductors that are skew to the buses.

~~18.~~ 11. The apparatus ~~according to the preceding~~ of claim 10, wherein the one or more conductors comprise at least one of pogo pins, land grid arrays, or through-silicon vias.

~~19. A method, comprising:~~

~~bonding one or more qubit chips to a substrate; and~~

~~routing one or more resonators of the one or more qubit chips to one or more inner regions of the substrate, the one or more inner regions positioned between one or more pairs of adjacent chips of the one or more qubit chips.~~

~~20. The method according to the preceding claim, further comprising:~~

~~coupling the one or more pairs of adjacent chips of the one or more qubit chips together via buses positioned on the one or more inner regions, wherein the one or more resonators are positioned between the buses.~~

~~21. The method according to the preceding claim, further comprising:~~

~~coupling the one or more resonators to a printed circuit board via one or more conductors that are skew to the buses.~~

~~22. The method according to the preceding claim, wherein the one or more conductors comprise at least one of pogo pins, land grid arrays, or through-silicon vias.~~

~~23.~~ 12. An interposer, comprising:

~~quantum chips; and~~

~~quantum input/output ports routed between adjacent pairs of the quantum chips.~~

~~24. The~~ , wherein the quantum input/output ports are located on a peripheral portion of the interposer ~~according to the preceding claim, further comprising:~~.

13. The interposer of claim 12, further comprising:

cross-chip lines coupling the adjacent pairs of the quantum chips, the cross-chip lines located between the adjacent pairs of the quantum chips, wherein the quantum input/output ports are located between the cross-chip lines.

~~25.~~ 14. The interposer ~~according to the preceding~~ of claim 13, wherein a printed circuit board is coupled to the quantum input/output ports by pins that are skew to the cross-chip lines.