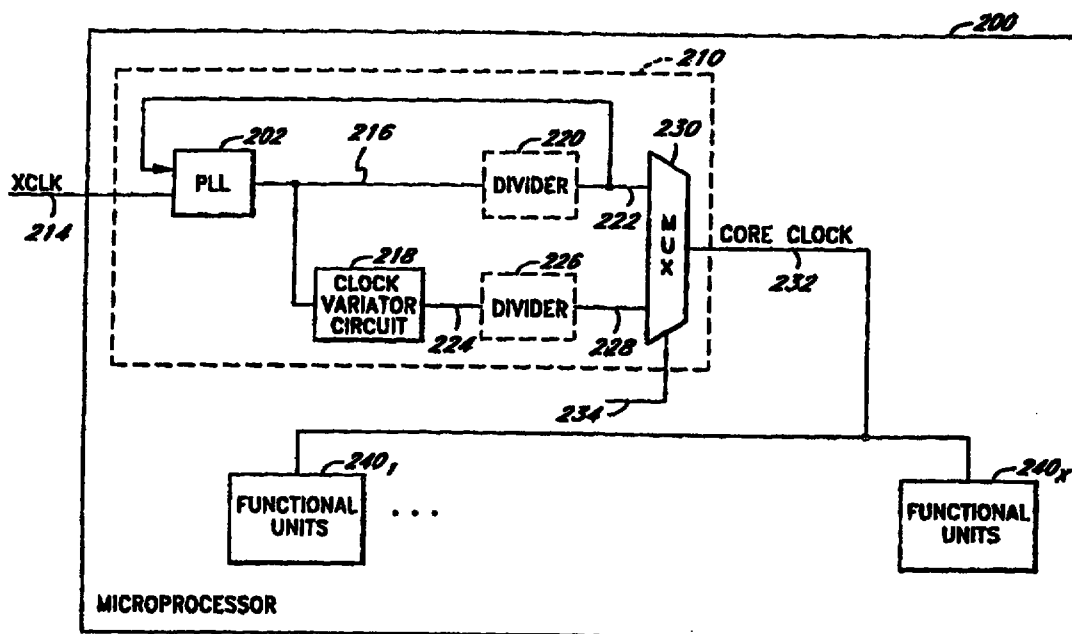




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H03K 17/62, H03H 11/26	A1	(11) International Publication Number: WO 99/56393 (43) International Publication Date: 4 November 1999 (04.11.99)
(21) International Application Number: PCT/US99/08888 (22) International Filing Date: 23 April 1999 (23.04.99) (30) Priority Data: 09/071,375 30 April 1998 (30.04.98) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): STINSON, Jason, C. [US/US]; 317 Mercy Street, Mountain View, CA 94041 (US). LILYA, Edwin, R. [US/US]; 109 Kerwin Way, Folsom, CA 95630 (US). NAZARETH, Mathew, B. [US/US]; 2330 Vehicle Drive #48, Rancho Cordova, CA 95670 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).	(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.	

(54) Title: METHOD AND APPARATUS FOR VARYING A CLOCK FREQUENCY ON A PHASE BY PHASE BASIS



(57) Abstract

A circuit (218) to vary a frequency of an input clock (216) is disclosed. The circuit (218) includes a delay generator (310) to generate at least two delayed clocks (D1 and DM) from the input (216) clock and a select circuit (320) coupled to receive the at least two delayed clocks (D1 and DM) and provide an output clock (325) from one of the at least two delayed clocks (D1 and DM). The select circuit (320) switches the output clock from the one of the at least two delayed clocks to the other of the at least two delayed clocks on a first edge.