

Circuit arrangement with a filter quadripole

The invention relates to a circuit arrangement with a filter quadripole. Such circuit arrangements are used, for example, in receiver circuits as used, for example, for pagers.

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Receiver circuits are generally to satisfy certain requirements as regards the turn-on time. The term turn-on time is then used for the period of time between applying the supply voltage to the receiver circuit and the reaching of an operating state in which a perfect processing of the signals received by the receiver circuit is possible. In battery-
10 operated receiver circuits, the turn-on time has a considerable effect on the useful life of the battery.

For example, pagers need to have turn-on times in the range of milliseconds. It must be born in mind that this turn-on time for the whole pager is formed by the sum of the turn-on times of individual circuit components and sub-sets, so that the
15 duration of the turn-on time for receiver circuits in pagers is required to be restricted to a few microseconds.

Alternatively, receiver circuits having a low intermediate frequency, more particularly, in the kilohertz range, require high-pass filters for d.c. decoupling in a high-gain signal path for the received signal that is to be processed which high-pass filters have a
20 cut off frequency that is selected to be low with an accordingly low intermediate frequency i.e. have a high time constant. During the turn-on time i.e. while the receiver circuit is taken into operation, the signal regularly shows voltage jumps produced by this receiver circuit, which jumps may be the result of asymmetries, self-reception but also other influences. In the case of self-reception, the signal produced by the local oscillator of the receiver circuit
25 overcouple on its antenna input and, in consequence, is mixed with itself to an offset d.c. voltage in the mixer connected to the local oscillator. In the build-up time of the oscillator, during the turn-on time when the receiver circuit is taken into operation, this offset d.c. voltage appears as a voltage jump on the output of the receiver circuit. This voltage jump is amplified with high gain provided for the signal to be received in the receiver circuit and, as

a result, overloads the high-pass filters which the signal passes through in the signal path. Depending on the amplitude of this voltage jump (noise voltage) and the time constant of the high-pass filters, the decay time of the noise voltage on the output of the receiver circuit (or of the high-pass filters, respectively) may be several milliseconds. For the requirements to be made on the pagers and their receiver circuits, the decay time is much too long.

It is an object of the invention to provide a circuit arrangement comprising a filter quadripole for a receiver circuit, more particularly, for a pager, which circuit arrangement has a considerably shorter turn-on time than a pager.

This object is achieved by the circuit arrangement comprising

- a filter quadripole having two output terminals and
- a voltage follower circuit having two terminals, said terminals having identical electric potentials when the voltage follower circuit is in its turned-on state, each of the terminals of the voltage follower circuit being connected to one of the output terminals of the filter quadripole respectively, and the voltage follower circuit only being in its turned-on state during the turn-on time interval of the circuit arrangement.

The invention utilizes the recognition that the turn-on time is determined, in essence, by the variation with time of the signal on the output of the filter quadripole when the circuit arrangement is taken into operation. The circuit arrangement according to the invention provides a reduction of the decay time of the noise voltages on the output terminals of the filter quadripole from the millisecond range to the microsecond range. This satisfies an essential requirement of reducing the turn-on time of the whole receiver circuit to the microsecond range.

Special advantages are obtained when a high-pass filter takes the place of the filter quadripole. The high-pass filter output terminals are bridged by the terminals of the voltage follower circuit. The voltage follower circuit, which is only in operation during the turn-on time, forces the voltage potentials on the output terminals of the filter quadripole to match. When the filter quadripole is taken into operation, the voltage follower circuit decisively accelerates building-up times and transients respectively in the filter quadripole.

Further advantageous embodiments of the invention are stated in the dependent Claims.

A very simple embodiment of the invention is shown in the drawing and will be further explained in the following.

- 5 The sole figure of this drawing diagrammatically shows a filter quadripole which is arranged as a high-pass filter and comprises a capacitor 1 as a capacitive circuit element and a resistor 2 as an ohmic circuit element. The capacitor 1 has the capacitance C , the resistor 2 the resistance R . The product $R \cdot C$ determines in known manner the cut off frequency of the filter quadripole, i.e. of the high-pass filter forming this filter quadripole.
- 10 For receiving an input signal, two input terminals 3, 4 of the filter quadripole 1, 2 are connected to a signal voltage source 5 which produces an input voltage U_e (signal voltage, useful signal) when the circuit arrangement is in operation. When the input voltage U_e is supplied, the filter quadripole 1, 2 produces an output voltage U_a on two output terminals 6, 7. The capacitor 1 of the filter quadripole is arranged as a series capacitor between the input
- 15 terminal 4 and the output terminal 7, the resistor 2 as a shunt resistor between the output terminals 6, 7.

- A voltage follower circuit comprises a transistor pair formed by two
- 20 transistors 8, 9 in the present example arranged as npn transistors. Their main current paths are interconnected via their emitter terminals and connected to a switchable current source 10 which is also connected to ground 11. The switchable current source 10 can be turned on and off via a switch input 12. In the turned-on state it carries a direct current I_0 , in the turned-off state it is currentless. On the other hand, the transistor pair 8, 9 is coupled with its main
- 25 current paths to a current mirror circuit which comprises two pnp transistors 13, 14 in the example shown in the figure. Either of these pnp transistors that forms the input transistor of the current mirror circuit 13, 14 - transistor 13 - and whose base and collector terminals are interconnected, is connected to the main current path of the transistor 8. The second pnp transistor 14 forms the output transistor of the mirror current path while its collector terminal
- 30 is connected to the main current path of the second transistor 9 of the transistor pair. Furthermore, the two emitter terminals of the mirror current circuit 13, 14 are connected to a power supply terminal 15, and the collector terminal and the base terminal of the second transistor 9 of the transistor pair are interconnected. The base terminals of the transistors 8, 9 form each a terminal 16, 17 by which the voltage follower circuit is connected to the

output terminals 6, 7 respectively, of the filter quadripole 1, 2.

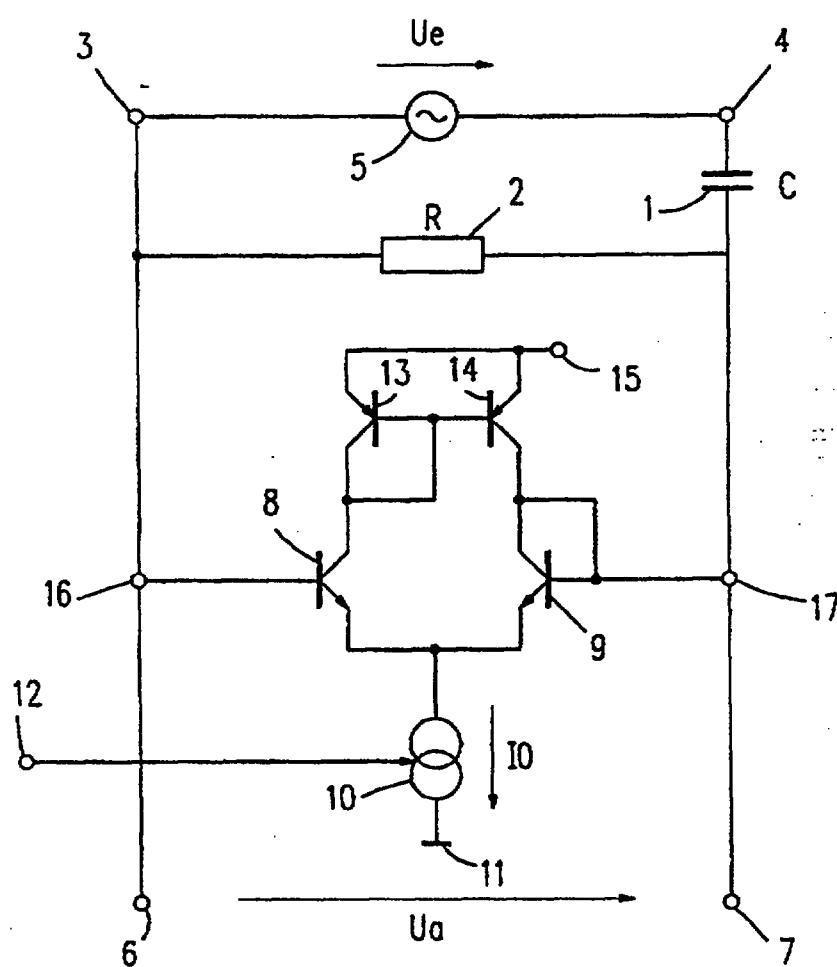
When the filter quadripole 1, 2 and the circuit arrangement comprising same are operated in accordance with the invention, the switchable current source 10 is rendered currentless through the switch input 12. This provides that the whole voltage follower circuit is inoperative and the transfer characteristic of the filter quadripole 1, 2 is not affected. In the starting phase of the filter quadripole 1, 2, i.e. when it is taken into operation (the power supply turned on), the switchable current source 10 is turned on for a defined period of time. It can be turned on through the switch input 12 by a control circuit which controls the whole operation of the circuit arrangement, which arrangement includes the filter quadripole 1, 2, for example, of a receiver circuit or a pager respectively. As long as the d.c. current I_0 flows i.e. as long as the switchable current source 10 continues to be turned on, the voltage follower circuit forces corresponding voltage potentials to be present on its terminals 16 and 17 i.e. also on the output terminals 6 and 7 of the filter quadripole 1, 2. This provides a very rapid and strong attenuation of any voltage jump on these output terminals 6, 7. If a voltage difference already occurs on the output terminals 6 and 7 before the switchable control source 10 is turned on, the voltage follower circuit rapidly causes this voltage difference to fade out. In the present example, this means that the capacitor 1 is recharged for a period of time which can be set to the desired value by accordingly selecting the d.c. current I_0 . As a result, the turn-on time of the filter quadripole may be made very brief.

After the turn-on time has ended, the switchable current source 10 is again turned off and, therefore, no longer consumes power from the power supply terminal 15. Even if the d.c. current I_0 is very large, this d.c. current forms only a minor load on the power supply terminal 15, i.e. for example, a battery connected to this terminal.

CLAIMS:

1. A circuit arrangement comprising
 - a filter quadripole having two output terminals and
 - a voltage follower circuit having two terminals, said terminals having identical electric potentials when the voltage follower circuit is in its turned-on state, each of the terminals of the voltage follower circuit being connected to one of the output terminals of the filter quadripole respectively, and the voltage follower circuit only being in its turned-on state during the turn-on interval of the circuit arrangement.
2. A circuit arrangement as claimed in Claim 1, characterized in that the filter quadripole forms a high-pass filter.
3. A circuit arrangement as claimed in Claim 2, characterized in that the filter quadripole has two input terminals, at least one of which being connected to at least one of said output terminals via at least one capacitive circuit element, and in that the filter quadripole comprises at least one ohmic circuit element that bridges the output terminals.
4. A circuit arrangement as claimed in one of the preceding Claims, characterized in that the voltage follower circuit comprises a transistor pair whose main current paths are interconnected and connected to a switchable current source and, on the other hand, are coupled to a current mirror circuit and whose control terminals form the terminals of the voltage follower circuit, the current mirror circuit output being connected not only to one of the main current paths but also direct to the control terminal of the associated transistor of the transistor pair.
5. A pager, characterized by a circuit arrangement as claimed in one of the preceding Claims.

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(54) Title: CIRCUIT ARRANGEMENT WITH A FILTER QUADRIPOLE		
(57) Abstract A description is given of a circuit arrangement comprising a filter quadripole having two output terminals; and a voltage follower circuit having two terminals, said terminals having identical electric potentials when the voltage follower circuit is in its turned-on state, each of the terminals of the voltage follower circuit being connected to one of the output terminals of the filter quadripole respectively, and the voltage follower circuit only being in its turned-on state during the turn-on time interval of the circuit arrangement. This circuit arrangement is suitable for a receiver circuit, more particularly, for a pager and has a very brief turn-on time.		