CLAIMS

1. A semiconductor structure, comprising:

a substrate and at least one active pillar located above the substrate, the active pillar extending in a first direction, and the first direction being parallel to a plane where the substrate is located,

wherein the active pillar comprises a body area extending in the first direction and a peripheral area surrounding the body area, and the peripheral area comprises a channel area, and

wherein a type of doped ions of the channel area is the same as a type of doped ions of the body area, the type of doped ions of the channel area is P-type or N-type, and a doping concentration of the channel area is greater than a doping concentration of the body area.

2. The semiconductor structure according to claim 1, wherein the body area comprises an inner layer extending in the first direction and an outer layer surrounding the inner layer, and a doping concentration of the inner layer is greater than a doping concentration of the outer layer.

3. The semiconductor structure according to claim 2, wherein the doping concentration of the body area is gradually reduced from a center to a periphery in a radial direction of the active pillar.

4. The semiconductor structure according to claim 1, wherein the peripheral area further comprises a first doped area and a second doped area, and the first doped area, the channel area and the second doped area are successively arranged in the first direction, wherein the body area further comprises an extension area not surrounded by the peripheral area, and the

extension area is adjacent to the first doped area.

5. The semiconductor structure according to claim 4, further comprising: a conductive structure extending in a second direction and electrically connected to the extension area, wherein the second direction intersects with the first direction and is parallel to the plane where the substrate is located.

6. The semiconductor structure according to claim 4, further comprising: a conductive structure extending in a third direction and electrically connected to the extension area, wherein the third direction is a direction perpendicular to the plane where the substrate is located.

7. The semiconductor structure according to claim 1, wherein the semiconductor structure comprises multiple active pillars arranged in multiple active pillar rows and multiple active pillar columns, the multiple active pillar rows extend in a second direction, the second direction intersects with the first direction and is parallel to the plane where the substrate is located, the multiple active pillar columns extend in a third direction, and the third direction is a direction perpendicular to the plane where the substrate is located.

8. The semiconductor structure according to claim 7, further comprising: a conductive structure located on the substrate, wherein the conductive structure has a plate shape, and the conductive structure is electrically connected to extension areas in the multiple active pillar rows.

9. The semiconductor structure according to any one of claims 5 to 6 or 8, wherein the conductive structure is grounded.

10. The semiconductor structure according to claim 7, further comprising: multiple word lines, wherein each of the multiple word lines extends in the third direction, the multiple word lines are arranged in the second direction, each of the multiple word lines corresponds to a respective one of the multiple active pillar columns, and each of the word lines covers multiple channel areas in the respective one of the multiple active pillar columns; and

multiple bit lines, wherein each of the multiple bit lines extends in the second direction, the multiple bit lines are arranged in the third direction, each of the multiple bit lines corresponds to a respective one of the multiple active pillar rows, and each of the bit lines is electrically connected to multiple first doped areas in the respective one of the multiple active pillar rows.

11. The semiconductor structure according to claim 7, further comprising: multiple word lines, each of the multiple word lines extends in the second direction, the multiple word lines are arranged in the third direction, each of the multiple word lines corresponds to a respective one of the multiple active pillar rows, and each of the multiple word lines covers multiple channel areas in the respective one of the multiple active pillar rows; and

multiple bit lines, wherein each of the multiple bit lines extends in the third direction, the multiple bit lines are arranged in the second direction, and each of the multiple bit lines is electrically connected to multiple first doped areas in the respective one of the multiple active pillar columns.

12. The semiconductor structure according to claim 10 or 11, wherein each of the multiple word lines surrounds corresponding channel area.

13. The semiconductor structure according to claim 10 or 11, wherein each of the multiple word lines comprises a first sub-layer and a second sub-layer opposite to each other, and the

first sub-layer covers one of two opposite side walls of corresponding channel area and the second sub-layer covers the other one of the two opposite side walls of the corresponding channel area.

14. The semiconductor structure according to claim 10 or 11, wherein each of the multiple bit lines surrounds corresponding first doped area.

15. The semiconductor structure according to claim 11, wherein each of the multiple bit lines comprises multiple sub-portions, and the multiple sub-portions and the multiple first doped areas in the respective one of the active pillar columns are alternately stacked onto one another in the third direction.