

FINAL POLISHING PROCESSING METHOD FOR HEAVILY-DOPED WAFER AND POLISHED HEAVILY-DOPED WAFER

CROSS-REFERENCE TO RELATED DISCLOSURE

[0001] The present disclosure claims a priority to the Chinese patent disclosure No. 202511382364.5 filed in China on September 25, 2025, a disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of semiconductor manufacturing technology, and in particular, to a processing method for a heavily-doped wafer in a final polishing process and a polished heavily-doped wafer.

BACKGROUND

[0003] In the production of semiconductor wafers, final polishing is a critical step for ensuring surface quality of the wafer, and it is used to remove a damage layer that may be introduced in a previous process, and ensure that a surface of the wafer achieves a high standard of flatness and cleanliness for subsequent devices fabrication.

[0004] The heavily-doped wafers, such as P/P+-type wafers, have found extensive application in various fields, particularly in semiconductor power devices. However, in a case that the heavily-doped wafers are subjected to the final polishing using the final polishing process, it is usually impossible to obtain excellent surface quality, resulting in a low final yield.

SUMMARY

[0005] This section provides a general overview of the present disclosure, and is not intended as a comprehensive disclosure of the entire scope or all features of the present disclosure.

[0006] An object of the present disclosure is to provide a processing method for a heavily-doped wafer in a final polishing process, which can improve surface quality of the heavily-doped wafer which is subjected to the final polishing, and increase the final yield.

[0007] According to a first aspect of the present disclosure, a processing method for a heavily-doped wafer in a final polishing process is provided. The processing method includes:

performing, by using a first polishing slurry, a first polishing step on a heavily-doped wafer;

performing, by using a second polishing slurry, a second polishing step on the heavily-doped wafer on which the first polishing step has been performed; and

performing, by using a third polishing slurry, a third polishing step on the heavily-doped wafer on which the second polishing step has been performed,

wherein the first polishing slurry and the second polishing slurry both include an alkaline additive, and the third polishing slurry does not include the alkaline additive.

[0008] In some embodiments, a volume ratio of the alkaline additive to a solvent in the first polishing slurry is greater than a volume ratio of the alkaline additive to a solvent in the second polishing slurry.

[0009] In some embodiments, the volume ratio of the alkaline additive to the solvent in the first polishing slurry is in a range of 1:2500 to 1:1500, and the volume ratio of the alkaline additive to the solvent in the second polishing slurry is in a range of 1:5000 to 1:2500.

[0010] In some embodiments, the alkaline additive is an inorganic base or an organic base.

[0011] In some embodiments, the alkaline additive includes KOH, NaOH or NH₄OH.

[0012] In some embodiments, the first polishing step is performed to achieve a first target removal thickness, the second polishing step is performed to achieve a second target removal thickness, and the third polishing step is performed to achieve a third target removal thickness, wherein the first target removal thickness is greater than the second target removal thickness, and the second target removal thickness is greater than the third target removal thickness.

[0013] In some embodiments, a ratio of the first target removal thickness, the second target removal thickness and the third target removal thickness is 6:3:1.

[0014] In some embodiments, a sum of the first target removal thickness, the second target removal thickness and the third target removal thickness is greater than 150% of a thickness of a damaged layer of the heavily-doped wafer on which the first polishing step is to be performed.

[0015] According to a second aspect of the present disclosure, a polished heavily-doped wafer is provided, which is obtained by a processing method for the heavily-doped wafer in a final polishing process. The processing method includes: performing, by using a first polishing slurry, a first polishing on a heavily-doped wafer; performing, by using a second polishing slurry, a second polishing on the heavily-doped wafer on which the first polishing step has been performed; and performing, by using a third polishing slurry, a third polishing on the heavily-doped wafer on which the second polishing step has been performed, wherein the first polishing slurry and the

second polishing slurry both include an alkaline additive, and the third polishing slurry does not include the alkaline additive, wherein a quantity of Differential Interference Contrast (DIC) defects with a size of 5 nm or more on the polished heavily-doped wafer is less than 5.

[0016] In some embodiments, the quantity of DIC defects with the size of 5 nm or more on the polished heavily-doped wafer is less than 3.

[0017] According to a third aspect of the present disclosure, a polished heavily-doped wafer is provided. The polished heavily-doped wafer includes a p-type or n-type dopant with a concentration of greater than 1×10^{18} atoms/cm³, and a quantity of DIC defects with a size of 5 nm or more on the polished heavily-doped wafer is less than 5.

[0018] According to the above solutions, the final polishing process is designed as three-step polishing, the polishing slurry of the first polishing step and the second polishing step include the alkaline additive, and the polishing slurry of the third polishing step does not include the alkaline additive, so as to solve surface defect problems of the heavily-doped wafer which is subjected to the final polishing. The first polishing step uses a strong chemical etching effect of the alkaline additive to rapidly remove a surface of the heavily-doped wafer which contains crystal-originated defects, so as to prevent the crystal-originated defects from being enlarged into the DIC defects due to a long-term effect of conventional pure mechanically polishing on the crystal-originated particles. Next, the second polishing step is used to remove the damage on the surface of the heavily-doped wafer caused by mechanically polishing and chemical etching in the first polishing step, and the third polishing step is used to perform pure mechanically repairing on the surface of the heavily-doped wafer, so as to finally obtain the heavily-doped wafer which has extremely few DIC defects on its surface, improve the surface quality of the heavily-doped wafer which is subjected to the final polishing, and thereby increase the final yield.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Through the following description with reference to the accompanying drawings, the features and advantages of the embodiments of the present disclosure will become more readily understood. The drawings are not drawn to scale, and some features may be enlarged or reduced to show the details of specific components. In the drawings:

[0020] FIG. 1 is a schematic diagram of a final polisher in the related art;

[0021] FIG. 2 is a schematic cross-sectional view of a polished heavily-doped wafer obtained by using a processing method for a heavily-doped wafer in a final polishing process in the related art;

[0022] FIG. 3 exemplarily shows schematic morphological features of a single DIC defect formed on a polished heavily-doped wafer;

[0023] FIG. 4 is a flowchart of a processing method for a heavily-doped wafer in a final polishing process according to an embodiment of the present disclosure;

[0024] FIG. 5 is a comparison diagram of DIC defect test results between a series of polished heavily-doped wafers obtained by using the processing method for the heavily-doped wafer in the final polishing process according to the related art and a series of polished heavily-doped wafers obtained by using the processing method for the heavily-doped wafer in the final polishing process according to an embodiment of the present disclosure;

[0025] FIG. 6 is another comparison diagram of DIC defect test results between a series of polished heavily-doped wafers obtained by using the processing method for the heavily-doped wafer in the final polishing process according to the related art and a series of polished heavily-doped wafers obtained by using the processing method for the heavily-doped wafer in the final polishing process according to an embodiment of the present disclosure;

[0026] FIG. 7 is a schematic diagram showing the distribution of DIC defects on the surface of a polished heavily-doped wafer obtained by using a processing method for a heavily-doped wafer in a final polishing process in the related art;

[0027] FIG. 8 is a schematic diagram showing the distribution of DIC defects on the surface of a polished heavily-doped wafer obtained by using the processing method for a heavily-doped wafer in a final polishing process according to an embodiment of the present disclosure;

[0028] FIG. 9 is a schematic diagram of an exemplary final polisher for performing a processing method for a heavily-doped wafer in a final polishing process according to an embodiment of the present disclosure.

[0029] In the drawings, the same or corresponding technical features or components are denoted by the same or corresponding reference numerals.

DETAILED DESCRIPTION

[0030] The present disclosure is described in detail below with reference to the accompanying drawings and by way of exemplary embodiments. It should be noted that the following detailed description of the present disclosure is for illustrative purposes only and is by no means intended to limit the present disclosure.

[0031] Before obtaining a finished wafer, it generally needs to go through manufacturing

processes such as cropping, wire sawing, edge grinding, chemical etching, double side grinding, double side polishing, edge polishing and final polishing.

[0032] Among the various polishing processes in the above-mentioned manufacturing processes, the double side polishing process is typically performed at an earlier stage in the processing sequence, and the purpose thereof is to remove a damage layer formed in previous processes such as wire sawing and double side grinding, and to improve the overall geometric characteristics of the wafer, such as flatness and thickness uniformity. The main goal is to ensure that the wafer meets basic physical properties.

[0033] The double side polishing process is performed by using a double side polisher. The double side polisher generally includes an upper platen and a lower platen that are arranged opposite each other, as well as a carrier plate positioned between the upper platen and the lower platen. The carrier plate is used to hold the wafer to be polished. The upper platen and the lower platen are provided thereon with an upper polishing pad and a lower polishing pad, respectively. In the double side polishing process, the upper platen and the lower platen simultaneously apply pressure to the wafer held in the carrier plate, so that the upper polishing pad and the lower polishing pad are in contact with the front and back sides of the wafer, respectively. Double side polishing of the wafer is thus accomplished through the movement of the carrier plate relative to the upper platen and the lower platen.

[0034] An edge polishing process is primarily performed on an edge of the wafer, which is usually performed after the double side polishing process. The purpose is to improve the flatness of the wafer edge and remove edge defects such as protrusions and micro-cracks.

[0035] The edge polishing process is performed by using an edge polisher. Typically, the edge polisher includes a rotatable support plate and an edge polishing head. The support plate is used to hold the wafer to be edge polished and can drive the wafer to rotate about its central axis. During the edge polishing process, the edge polishing head can contact the edge of the rotating wafer to achieve polishing of the wafer edge.

[0036] At the final stage of various polishing processes in the above manufacturing process, the wafer that has been subjected to the above polishing processes (such as double side polishing process and edge polishing process) will finally be subjected to a final polishing process. The final polishing process is typically performed on the front side of the wafer to remove the damage formed in the previous processes including the previous polishing process and to achieve global planarization of the surface of the wafer. It is a precision processing, which enable the surface of the wafer to meet the quality standards required for subsequent device manufacturing (such as

photolithography process).

[0037] The final polishing process must be performed with the aid of a final polisher capable of performing this precision processing.

[0038] FIG. 1 shows an exemplary final polisher 1 in the related art. As shown in FIG. 1, the final polisher 1 includes a polishing head 2, a polishing table 3, and a polishing slurry supply pipeline 4. The polishing head 2 holds a wafer to be polished at its lower portion. The polishing table 3 is provided with a polishing pad 5 on its upper surface. The polishing slurry supply pipeline 4 is used to deliver the polishing slurry to the polishing pad 5. During the polishing process, the wafer held by the polishing head 2 is pressed against the polishing pad 5, and the final polishing of the wafer is achieved by the relative rotation between the polishing pad 5 and the wafer.

[0039] Typically, the final polishing process includes a rough polishing process and a fine polishing process. In the rough polishing process, a polishing slurry with a larger abrasive particle size is used to remove micro-damage from a previous layer. In the fine polishing process, a polishing slurry with a smaller abrasive particle size is used to clean and mirror-finish the surface of the wafer to achieve the required flatness and smoothness of the surface of the wafer.

[0040] In the final polishing process in the related art, the polishing slurry used for final polishing removes a subsurface damage layer on the surface of the wafer solely through mechanically polishing of abrasive particles. In this case, as mentioned above, different degrees of surface polishing effects are generally obtained by selecting abrasive particles of appropriate sizes.

[0041] However, in a case that a heavily-doped wafer is subjected to final polishing, this purely mechanically polishing process can easily introduce defects on the surface of the heavily-doped wafer.

[0042] The heavily-doped wafers possess a higher hardness due to their high oxygen content. In addition, in the single crystal growth, due to a material characteristic of the heavily-doped wafer, micro-void defects, i.e., Crystal Originated Pit (COPs), at a high density are easily formed at the center of the wafer, as indicated by A on the polished heavily-doped wafer W shown in FIG. 2. Therefore, after the heavily-doped wafer is processed by previous processes such as double side grinding and Low Temperature Oxidation (LTO), the area with COP accumulation appears as a crystal defect area. The COP is a critical factor that adversely affects the subsequent device performance (e.g., Gate Oxide Integrity (GOI)).

[0043] The inventors observed that, at a final polishing process, a conventional process which mainly uses mechanically polishing may lead to serious problems in a case of processing the heavily-doped wafer with the COPs. Due to the high surface hardness of the heavily-doped wafer,

a surface material removal rate of the heavily-doped wafer is low when the surface is polished by mechanically polishing, so it takes a considerable amount of time to remove the crystal defect area. This long-term mechanically polishing cannot effectively remove the COPs, and instead it enlarges the COP into a larger DIC defect, as indicated by B on the polished heavily-doped wafer W shown in FIG. 2. The DIC defect seriously reduces the surface quality and the final yield of the heavily-doped wafer.

[0044] It should be understood that FIG. 2 is not drawn to scale, and for clarity, both COP and DIC defects on the polished heavily-doped wafer W are schematically enlarged.

[0045] The DIC defect refers to a step-like defect observed by DIC techniques, for example, with a DIC microscope. FIG. 3 exemplarily shows the schematic morphological features of a single DIC defect. As shown in the figure, in terms of the overall morphology, the DIC defect is generally a raised step-like defect or a recessed pit-like defect. In addition, FIG. 3 shows a span of the DIC defect in a horizontal direction and a span in a vertical direction, wherein the horizontal direction refers to the direction extending along the plane where the surface of the heavily-doped wafer is located, and the vertical direction is the direction perpendicular to the plane where the surface of the heavily-doped wafer is located.

[0046] Referring to FIG. 3, a size of the DIC defect is characterized by the span of the DIC defect in the vertical direction, i.e., the maximum height difference H. That is, in the present disclosure, the size of the DIC defect refers to a height difference between the highest point and the lowest point of the DIC defect. In other words, the size of the DIC defect is the height difference, or elevation difference, between the highest point and the lowest point on the surface of the heavily-doped wafer where the DIC defect is located, and its unit is nanometers (nm).

[0047] It should be noted that the DIC defect in FIG. 3 is exemplary and is only intended to schematically illustrate the basic morphological features of the DIC defect, rather than indicating that the DIC defects exactly match the morphology depicted in FIG 3.

[0048] The DIC defect is an important indicator that affects heavily-doped wafer quality and device performance. Excessive DIC defects will not only reduce the yield and reliability of heavily-doped wafer products, but also limit the disclosure of heavily-doped wafer products in advanced technology fields.

[0049] Therefore, it is desirable to propose a processing method for a heavily-doped wafer in a final polishing process, which can reduce the formation of DIC defects while removing the damage from the previous processes and achieving mirror-like restoration of the surface of the heavily-doped wafer.

[0050] Referring to FIG. 4, according to an embodiment of the present disclosure, a processing method for a heavily-doped wafer in a final polishing process is provided.

[0051] The processing method includes:

S100: performing, by using a first polishing slurry, a first polishing step on a heavily-doped wafer;

S200: performing, by using a second polishing slurry, a second polishing step on the heavily-doped wafer on which the first polishing step has been performed; and

S300: performing, by using a third polishing slurry, a third polishing step on the heavily-doped wafer on which the second polishing step has been performed,

wherein the first polishing slurry and the second polishing slurry both include an alkaline additive, and the third polishing slurry does not include the alkaline additive.

[0052] It is understood that the first polishing slurry, the second polishing slurry and the third polishing slurry are all solid-liquid mixtures containing abrasive particles. The abrasive particles are used to physically grind the surface of the heavily-doped wafer to remove surface materials. In addition, the first polishing slurry, the second polishing slurry and the third polishing slurry all contain solvents that are used to disperse or dissolve the abrasive particles and other additives such as chemical additives.

[0053] The following provides a detailed description of each of the above steps.

[0054] The step S100 (a first polishing step) is used to remove a damage layer from previous processes on the surface of the heavily-doped wafer.

[0055] The damage layer from previous processes on the surface of the heavily-doped wafer refers to an area where damage (such as micro-scratches or cracks) introduced by the previous processing process (such as double side grinding, etc.) before the wafer is subjected to the first polishing step.

[0056] In the case that an alkaline additive is added to the first polishing slurry, the first polishing slurry is alkaline. This enables the first polishing step to combine the mechanically polishing effect of the abrasive particles and the chemical etching effect produced by OH⁻ ions, thereby providing a very high material removal rate. As a result, the thickness of the damage layer from previous processes can be rapidly removed, so as to prevent the long-term effect of the conventional low-speed mechanically polishing on the COPs, thereby to prevent the COPs in the defective area from being enlarged into DIC defects, and reduce the risk of forming DIC defects.

[0057] Specifically, in the first polishing step, a tip stress principle of chemical etching can be used to quickly remove severe damage. After the silicon oxide of the surface of the heavily-doped

wafer is removed, the OH⁻ ions can be used to quickly etch the heavily-doped wafer along the crystal lattice, thereby further reducing the risk of enlarging tiny crystal defects into the DIC defects.

[0058] Step S200 (a second polishing step) is used to remove the damage on the surface of the heavily-doped wafer caused by mechanically polishing and chemical etching in the first polishing step. An alkaline additive is added to the second polishing slurry, allowing a relatively high material removal rate to be achieved through the combination of material grinding and chemical etching.

[0059] Step S300 (a third polishing step) is used to repair the damage on the surface of the heavily-doped wafer caused by the mechanically polishing and chemical etching in the second polishing step. This step enables the surface of the heavily-doped wafer to achieve a mirror-like finish, resulting in a highly flat and smooth surface.

[0060] The third polishing slurry is formulated without alkaline additives, i.e., purely mechanically polishing is performed in the third polishing step, to avoid excessive chemical etching on the surface of the heavily-doped wafer, thereby avoiding deterioration of the flatness of the surface of the heavily-doped wafer and ensuring the final quality of the surface of the heavily-doped wafer.

[0061] Through the above solution, the removal of the damage layer from previous processes and the mirror-like restoration on the surface of the heavily-doped wafer are gradually accomplished by the three polishing steps, effectively shortening the time to remove the crystal defect area on the surface of the heavily-doped wafer. This helps to avoid the gradual enlargement of the COP in the defect area due to prolonged grinding, thereby reducing the risk of forming the DIC defects.

[0062] Hence, the formation of DIC defects can be reduced while removing the damage from the previous processes and achieving mirror-like restoration on the surface of the heavily-doped wafer, thereby improving the surface quality of the heavily-doped wafer, and increasing the final yield.

[0063] It is conceivable that, the volume ratio of the alkaline additive to the solvent in the first polishing slurry may be greater than the volume ratio of the alkaline additive to the solvent in the second polishing slurry, so that the concentration of OH⁻ ions in the first polishing slurry is higher than the concentration of OH⁻ ions in the second polishing slurry.

[0064] In this case, the first polishing step has a stronger alkali etching effect to achieve a relatively greater polishing ability and a faster polishing rate, so as to rapidly remove the surface

including the COPs, thereby to suppress a physical process of enlarging the micro-COPs into the DIC defects in a better manner.

[0065] The etching effect of the second polishing step is weaker than that of the first polishing step, resulting in a relatively lower polishing rate. This allows for the removal of the damage caused by the chemical etching in the first polishing step and the reduction in the damage to the current layer, and avoids the deterioration of parameters such as heavily-doped wafer flatness caused by excessive chemical action. As a result, a relatively finer polishing effect than that of the first polishing step can be achieved.

[0066] It can be understood that the initial concentration of the alkaline additive added to the first polishing slurry and the initial concentration of the alkaline additive added to the second polishing slurry may be the same. For example, the initial concentration of the alkaline additive may be 50 wt% for both.

[0067] For alkaline additives with the same initial concentration, the amount of the alkaline additive added to the solvent of the first polishing slurry may be greater than the amount of the alkaline additive added to the solvent of the second polishing slurry.

[0068] It is conceivable that, the volume ratio of the alkaline additive to the solvent in the first polishing slurry may be in a range of 1:2500 to 1:1500, and the volume ratio of the alkaline additive to the solvent in the second polishing slurry may be in a range of 1:5000 to 1:2500.

[0069] When the volume ratio of the alkaline additive to the solvent in the first polishing slurry is higher than 1:1500, the chemical action is too strong, which may easily lead to deterioration of heavily-doped wafer flatness and other qualities.

[0070] When the volume ratio of the alkaline additive to the solvent in the first polishing slurry is lower than 1:2500, the polishing rate of the first polishing step is low, which is not conducive to suppressing the generation of DIC defects and is also unfavorable for device capacity matching.

[0071] When the volume ratio of the alkaline additive to the solvent in the second polishing slurry is lower than 1:5000, the chemical action of the second polishing slurry is insufficient, making it ineffective in repairing the damage caused by the chemical etching in the first polishing step.

[0072] It is conceivable that, the alkaline additive may be an inorganic base.

[0073] For example, the alkaline additive may include KOH, NaOH, or NH₄OH.

[0074] It should be understood that, the alkaline additive may be an organic base, such as aminomethyl propanol, quaternary ammonium salt, and the like.

[0075] It is conceivable that, the first polishing step is performed to achieve a first target removal

thickness, the second polishing step is performed to achieve a second target removal thickness, and the third polishing step is performed to achieve a third target removal thickness, wherein the first target removal thickness is greater than the second target removal thickness, and the second target removal thickness is greater than the third target removal thickness.

[0076] In this case, material can be removed from the surface of the heavily-doped wafer using a stepwise decrease in the target removal amount. This not only helps to reduce the probability of the DIC defects, but the amount to be removed at each step can also be matched or adapted to the material removal rate of each polishing step. For example, a larger material removal rate matches a larger amount to be removed, thereby optimizing the polishing process and improving the overall efficiency of the final polishing process.

[0077] In the above embodiments, the ratio of the first target removal thickness, the second target removal thickness, and the third target removal thickness may be 6:3:1, so as to better match the desired material removal rates of the three steps.

[0078] Furthermore, to ensure the stability of the process and to sufficiently remove the damage from the previous process, it is conceivable that, a sum of the first target removal thickness, the second target removal thickness and the third target removal thickness is greater than 150% of a thickness of a damage layer of the heavily-doped wafer on which the first polishing step is to be performed.

[0079] It should be understood that the thickness of a previous damage layer is calculated based on a mean value, and the previous layer damage may fluctuate due to process variations and spare parts replacement. In actual production, the fluctuation of the previous layer damage can be controlled within 20%. Based on this fluctuation range, the maximum actual damage layer thickness may reach 120% of the thickness of the previous damage layer calculated based on the mean value. In combination with statistical principles and the 1.5 sigma shift management convention in quality management, the maximum actual damage layer thickness may reach approximately 150% of the thickness of the previous damage layer calculated based on the mean value. Therefore, by ensuring that the sum of the target removal thickness is greater than the possible maximum value of the actual damage layer thickness, the complete removal of the previous processes damage can be ensured.

[0080] It should be noted that the damage layer here refers to the damage layer present on the surface of the heavily-doped wafer when the heavily-doped wafer is about to be polished, or more specifically, immediately prior to the first polishing step. The damage layer is the area on the surface of the heavily-doped wafer where damage has been introduced by the previous processes

before the first polishing step, such as double side polishing.

[0081] It should be noted that the measurement of the thickness of the damage layer may be performed using a suitable measurement method selected based on the material of the heavily-doped wafer, the processing technology and device conditions, and other factors, and which is not limited herein.

[0082] According to the embodiments of the present disclosure, a polished heavily-doped wafer is further provided, which is obtained by a processing method for a heavily-doped wafer in a final polishing process according to an embodiment of the present disclosure. The processing method for a heavily-doped wafer in a final polishing process in the embodiments of the present disclosure includes the processing method according to any of the above-mentioned embodiments.

[0083] A quantity of DIC defects with a size of 5 nm or more (i.e., greater than or equal to 5 nm) on the polished heavily-doped wafer is less than 5.

[0084] It is achievable that, the quantity of DIC defects with a size of 5 nm or more on the polished heavily-doped wafer is less than 3.

[0085] Specifically, the polished heavily-doped wafer is obtained by performing a first polishing on a wafer by using a first polishing slurry, performing a second polishing on the heavily-doped wafer on which the first polishing step has been performed by using a second polishing slurry, and performing a third polishing on the heavily-doped wafer on which the second polishing step has been performed by using a third polishing slurry, wherein the first polishing slurry and the second polishing slurry both include an alkaline additive, and the third polishing slurry does not include the alkaline additive.

[0086] Taking the processing method for the heavily-doped wafer in the final polishing process according to the related art as comparative example A and the processing method for the heavily-doped wafer in the final polishing process according to the embodiments of the present disclosure as example B, FIG. 5 shows, in the form of box plots, statistical results of DIC defects in a series of polished heavily-doped wafers obtained in the case of comparative example A and a series of polished heavily-doped wafers obtained in the case of example B. The vertical axis represents the quantity of DIC defects with the size of 5 nm or more detected on a single polished heavily-doped wafer.

[0087] The polished heavily-doped wafer specifically refer to a heavily-doped wafer with a diameter of 300 mm or 12 inches.

[0088] As shown in FIG. 5, the average number of DIC defects with a size of 5 nm or more on the polished heavily-doped wafer obtained from the comparative example A is 2806.92, while the

average number of DIC defects with the size of 5 nm or more on the polished heavily-doped wafer obtained from the example B is 0.166667. It can be seen that the processing method for the heavily-doped wafer in the final polishing process according to the embodiments of the present disclosure can effectively reduce the DIC defects on the polished heavily-doped wafer obtained thereby.

[0089] FIG. 6 shows the quantity of DIC defects with a size of 5 nm or more in each of a series of polished heavily-doped wafers obtained in the case of the comparative example A and a series of polished heavily-doped wafers obtained in the case of the example B. From FIG. 6, the fluctuation in the quantity of DIC defects across the series of polished heavily-doped wafers can be observed.

[0090] As shown in FIG. 6, the quantity of DIC defects in a series of polished heavily-doped wafers obtained in example B is generally low and basically maintained at a consistent level. This indicates that the processing method for the heavily-doped wafer in the final polishing process according to the embodiments of the present disclosure offers high reliability and stability in reducing the DIC defects.

[0091] Furthermore, as shown in FIG. 7, the quantity of DIC defects with a size of 5 nm or more on the surface of the polished heavily-doped wafer obtained by comparative example A is quite high and densely distributed. As shown in FIG. 8, the quantity of DIC defects with a size of 5 nm or more on the surface of the polished heavily-doped wafer obtained by example B is extremely low. It can be seen that the surface quality of the polished heavily-doped wafer obtained by the processing method for the heavily-doped wafer in the final polishing process according to the embodiments of the present disclosure is higher.

[0092] According to an embodiment of the present disclosure, a polished heavily-doped wafer is further provided. The polished heavily-doped wafer includes a p-type or n-type dopant with a concentration of greater than 1×10^{18} atoms/cm³, and a quantity of DIC defects with a size of 5 nm or more on the polished heavily-doped wafer is less than 5.

[0093] It should be also understood that, the quantity of DIC defects with a size of 5 nm or more on the polished heavily-doped wafer may be less than 3.

[0094] FIG. 9 shows an exemplary final polisher 10 for performing a processing method for a heavily-doped wafer in a final polishing process according to an embodiment of the present disclosure. As shown in FIG. 9, the final polisher 10 includes a polishing head 20, a polishing table 30, and a polishing slurry supply pipeline 40. The polishing head 20 holds a heavily-doped wafer to be polished on its lower surface. A polishing pad 31, for contacting the heavily-doped wafer, is

provided on the upper surface of the polishing table 30. The polishing slurry supply pipeline 40 is used to provide the polishing slurry to the polishing pad 31, so that the heavily-doped wafer can be polished through the contact between the polishing pad 31 and the heavily-doped wafer.

[0095] The final polisher 10 may include a first containment tank 50 for storing the first polishing slurry, a second containment tank 60 for storing the second polishing slurry, and a third containment tank 70 for storing the third polishing slurry. By providing independent containment tanks, it is convenient to adjust the usage sequence and quantity of each polishing slurry according to the corresponding polishing steps, thereby improving the flexibility and adaptability of the process.

[0096] The following describes a process of using the final polisher 10 to perform a processing method for a heavily-doped wafer in a final polishing process according to an embodiment of the present disclosure.

[0097] In the case that the final polisher 10 is used to perform final polishing on the heavily-doped wafer, while the heavily-doped wafer is adsorbed and held by the polishing head 20, a certain flow rate of first polishing slurry is first supplied from the first containment tank 50 to the polishing pad 31 via the polishing slurry supply pipeline 40. After the polishing slurry is supplied to the polishing pad 31 and contacts the heavily-doped wafer, the respective drive shafts of the polishing head 20 and the polishing table 30 drive the polishing head 20 and the polishing table 30 to perform relative rotational movement. Simultaneously, the polishing head 20 applies pressure to the heavily-doped wafer, thereby accomplishing the first polishing step of the heavily-doped wafer.

[0098] Subsequently, in a similar manner, a certain flow rate of the second polishing slurry is supplied from the second containment tank 60 to the polishing pad 31 via the polishing slurry supply pipeline 40 to perform the second polishing step. Finally, a certain flow rate of the third polishing slurry is supplied from the third containment tank 70 to the polishing pad 31 via the polishing slurry supply pipeline 40 to perform the third polishing step. As a result, a polished heavily-doped wafer is ultimately obtained, in which the surface damage layer has been removed, the surface has been mirror-finished, and the quantity of DIC defects has been reduced.

[0099] Unless otherwise defined, technical or scientific terms used in the present disclosure shall have the ordinary meanings understood by those skilled in the art to which this disclosure pertains. The terms "comprise" and "include" are open-ended, i.e., a systems, device, article, composition, formulation or method that includes elements other than those listed after such terms in the claims is still considered to fall within the scope of the claims.

[0100] Although the present disclosure has been described with reference to exemplary embodiments, it should be understood that the present disclosure is not limited to the specific embodiments described and illustrated in detail herein. Various modifications may be made to the exemplary embodiments by those skilled in the art without departing from the scope defined by the claims of the present disclosure.

[0101] The features mentioned and/or illustrated in the above description of the exemplary embodiments of the present disclosure may be combined in the same or similar manner into one or more other embodiments, combined with features in other embodiments or substituted for corresponding features in other embodiments. The technical solutions obtained by these combinations or substitutions shall also be considered as included in the protection scope of the present disclosure. Therefore, the protection scope of the present disclosure shall be subject to the protection scope of the claims.

What is claimed is:

1. A processing method for a heavily-doped wafer in a final polishing process, comprising:
performing, by using a first polishing slurry, a first polishing step on a heavily-doped wafer;
performing, by using a second polishing slurry, a second polishing step on the heavily-doped wafer on which the first polishing step has been performed; and

performing, by using a third polishing slurry, a third polishing step on the heavily-doped wafer on which the second polishing step has been performed,

wherein the first polishing slurry and the second polishing slurry both comprise an alkaline additive, and the third polishing slurry does not comprise the alkaline additive.

2. The processing method for the heavily-doped wafer in the final polishing process according to claim 1, wherein a volume ratio of the alkaline additive to a solvent in the first polishing slurry is greater than a volume ratio of the alkaline additive to a solvent in the second polishing slurry.

3. The processing method for the heavily-doped wafer in the final polishing process according to claim 1, wherein the volume ratio of the alkaline additive to the solvent in the first polishing slurry is in a range of 1:2500 to 1:1500, and the volume ratio of the alkaline additive to the solvent in the second polishing slurry is in a range of 1:5000 to 1:2500.

4. The processing method for the heavily-doped wafer in the final polishing process according to claim 1, wherein the alkaline additive is an inorganic base or an organic base.

5. The processing method for the heavily-doped wafer in the final polishing process according to claim 1, wherein the alkaline additive comprises KOH, NaOH or NH₄OH.

6. The processing method for the heavily-doped wafer in the final polishing process according to claim 1, wherein the first polishing step is performed to achieve a first target removal thickness, the second polishing step is performed to achieve a second target removal thickness, and the third polishing step is performed to achieve a third target removal thickness, wherein the first target removal thickness is greater than the second target removal thickness, and the second target removal thickness is greater than the third target removal thickness.

7. The processing method for the heavily-doped wafer in the final polishing process

according to claim 6, wherein a ratio of the first target removal thickness, the second target removal thickness and the third target removal thickness is 6:3:1.

8. The processing method for the heavily-doped wafer in the final polishing process according to claim 6, wherein a sum of the first target removal thickness, the second target removal thickness and the third target removal thickness is greater than 150% of a thickness of a damaged layer of the heavily-doped wafer on which the first polishing step is to be performed.

9. A polished heavily-doped wafer, obtained by the processing method for the heavily-doped wafer in the final polishing process according to any one of claims 1 to 8, wherein a quantity of Differential Interference Contrast defects with a size of 5 nm or more on the polished heavily-doped wafer is less than 5.

10. A polished heavily-doped wafer, comprising a p-type or n-type dopant with a concentration of greater than 1×10^{18} atoms/cm³, and a quantity of Differential Interference Contrast defects with a size of 5 nm or more on the polished heavily-doped wafer is less than 5.