

FIG. 1

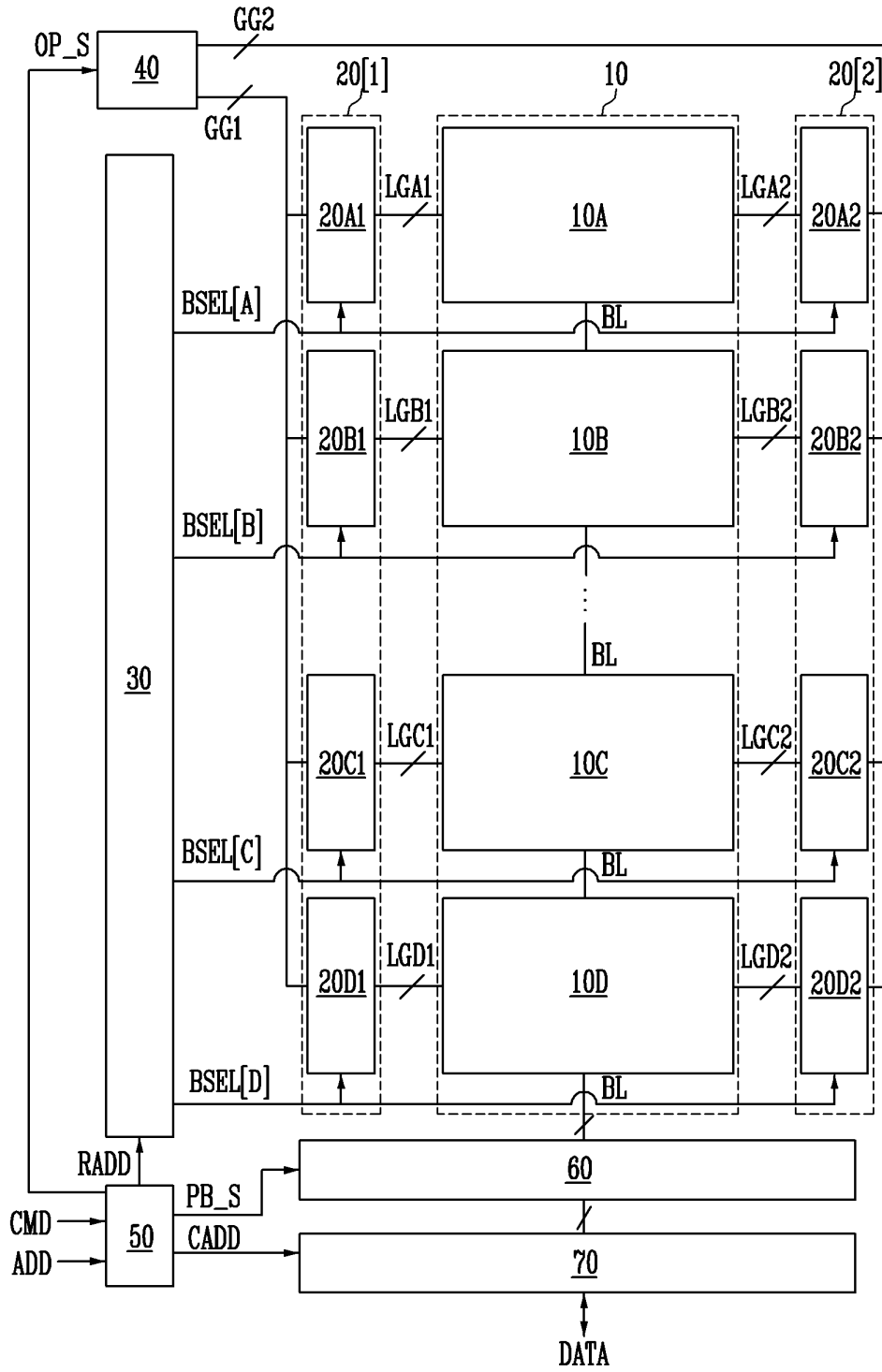


FIG. 2A

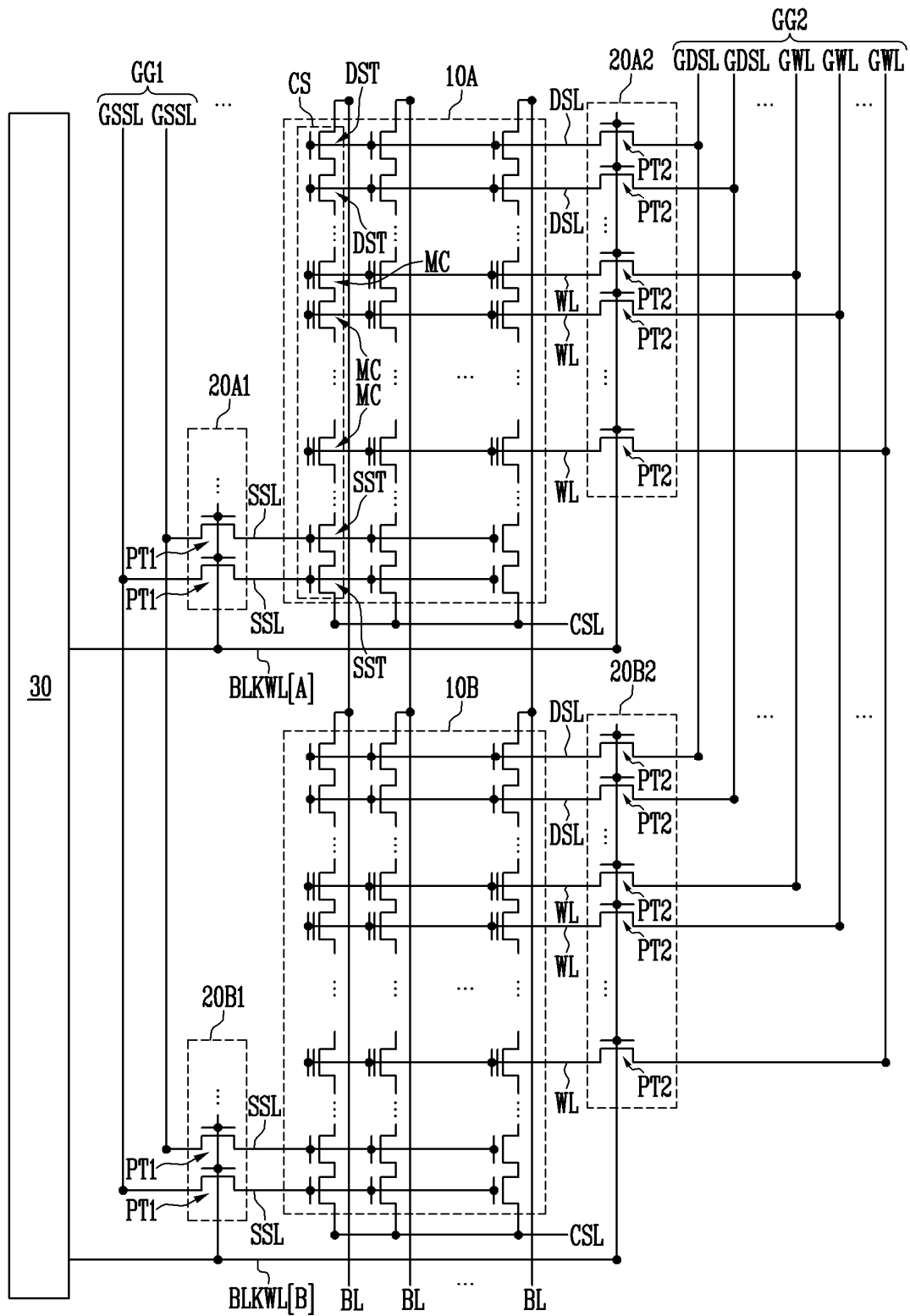


FIG. 2B

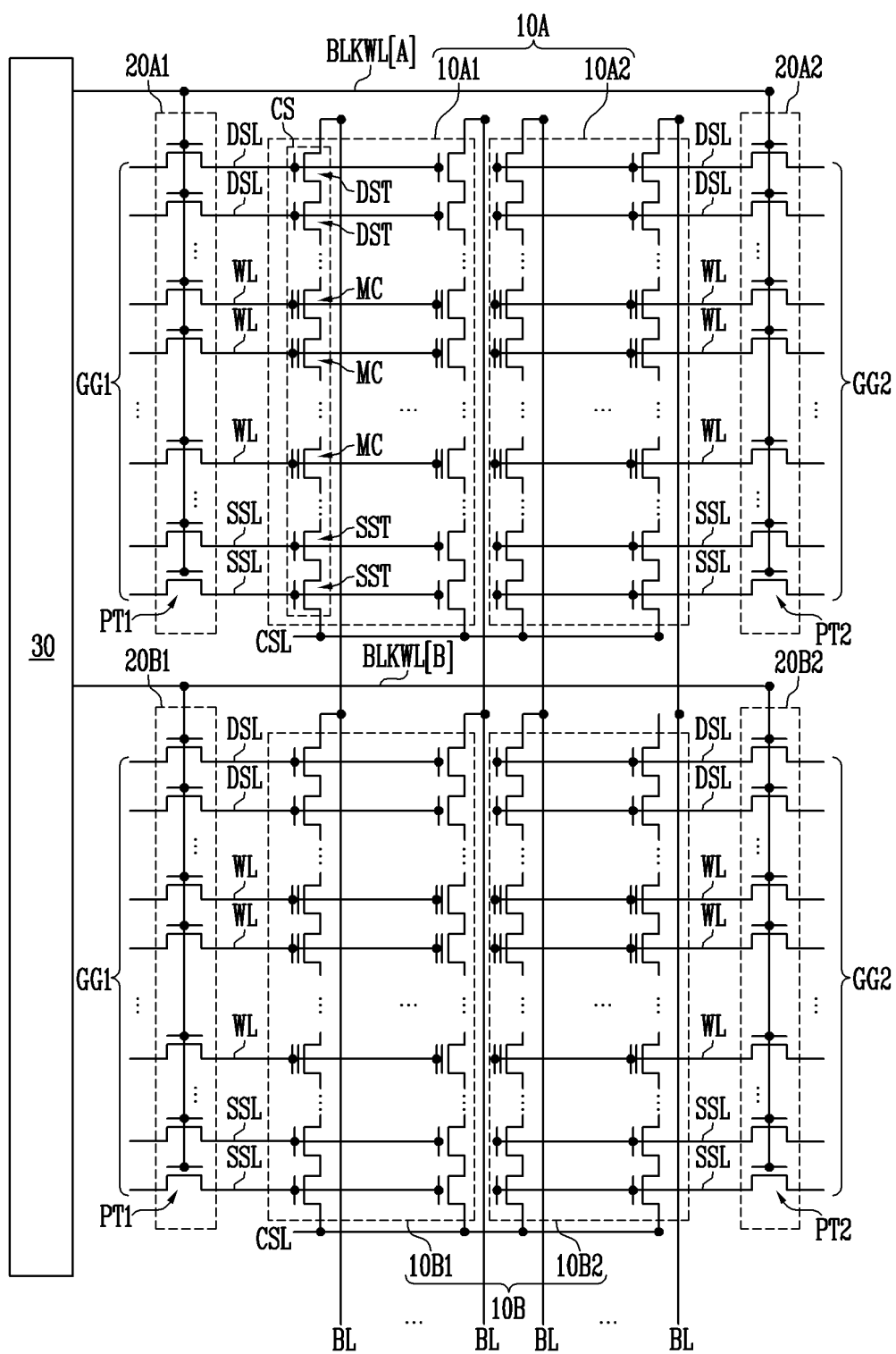


FIG. 3

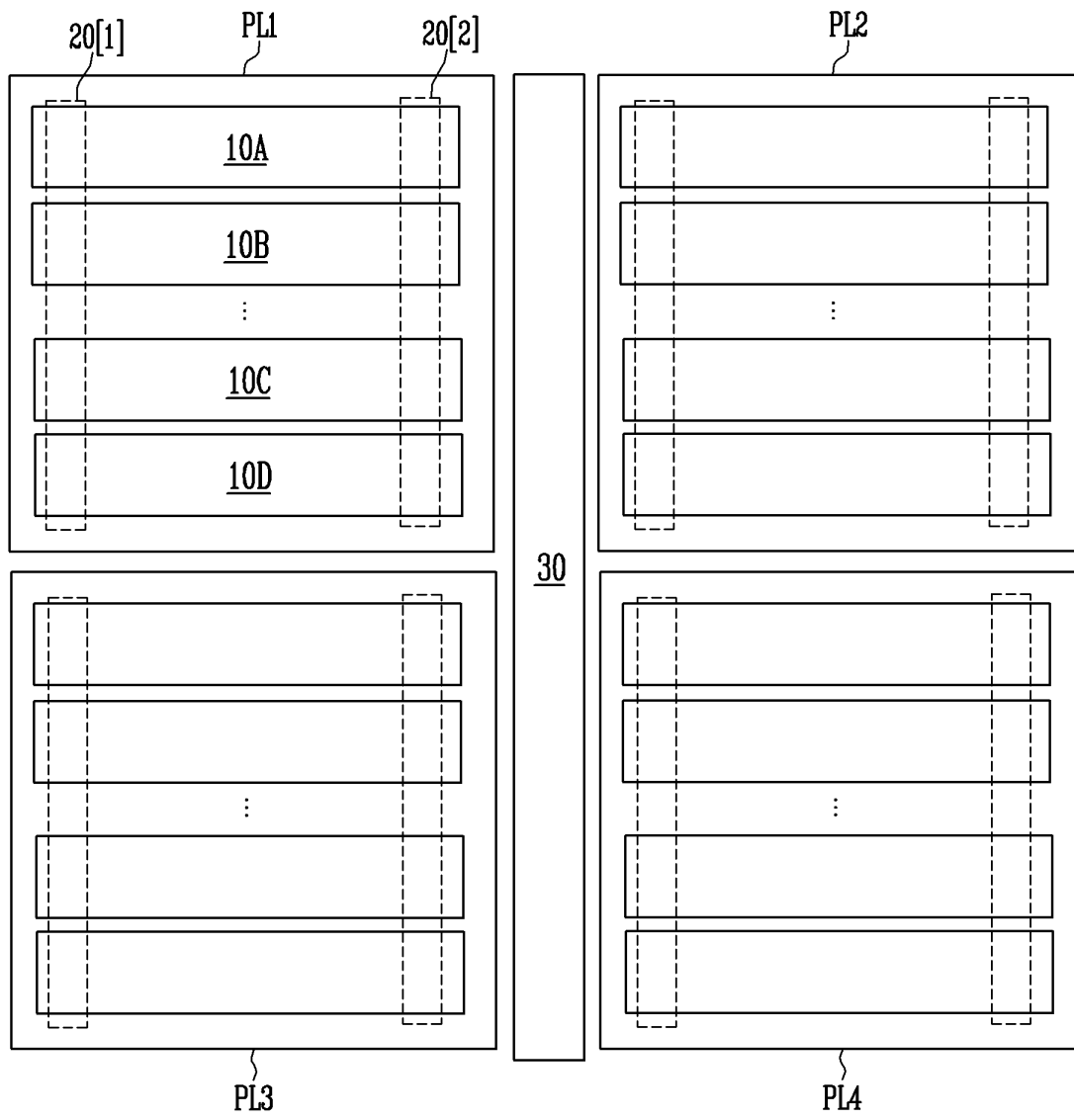


FIG. 4

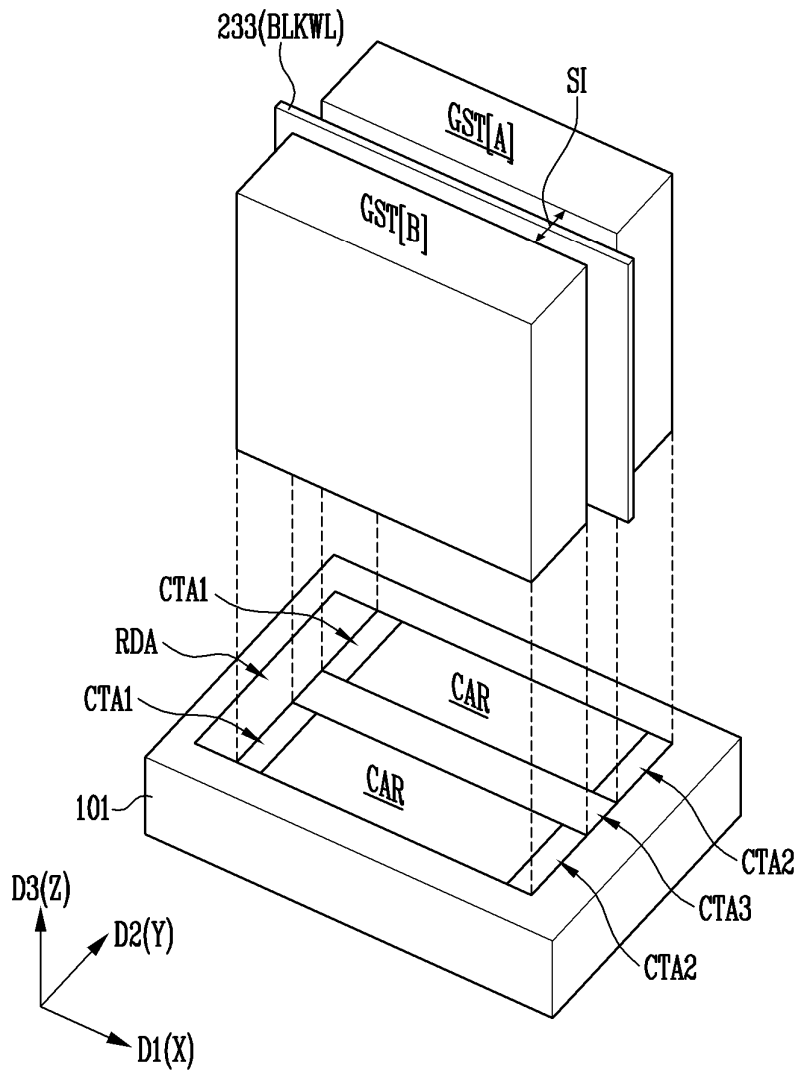


FIG. 5A

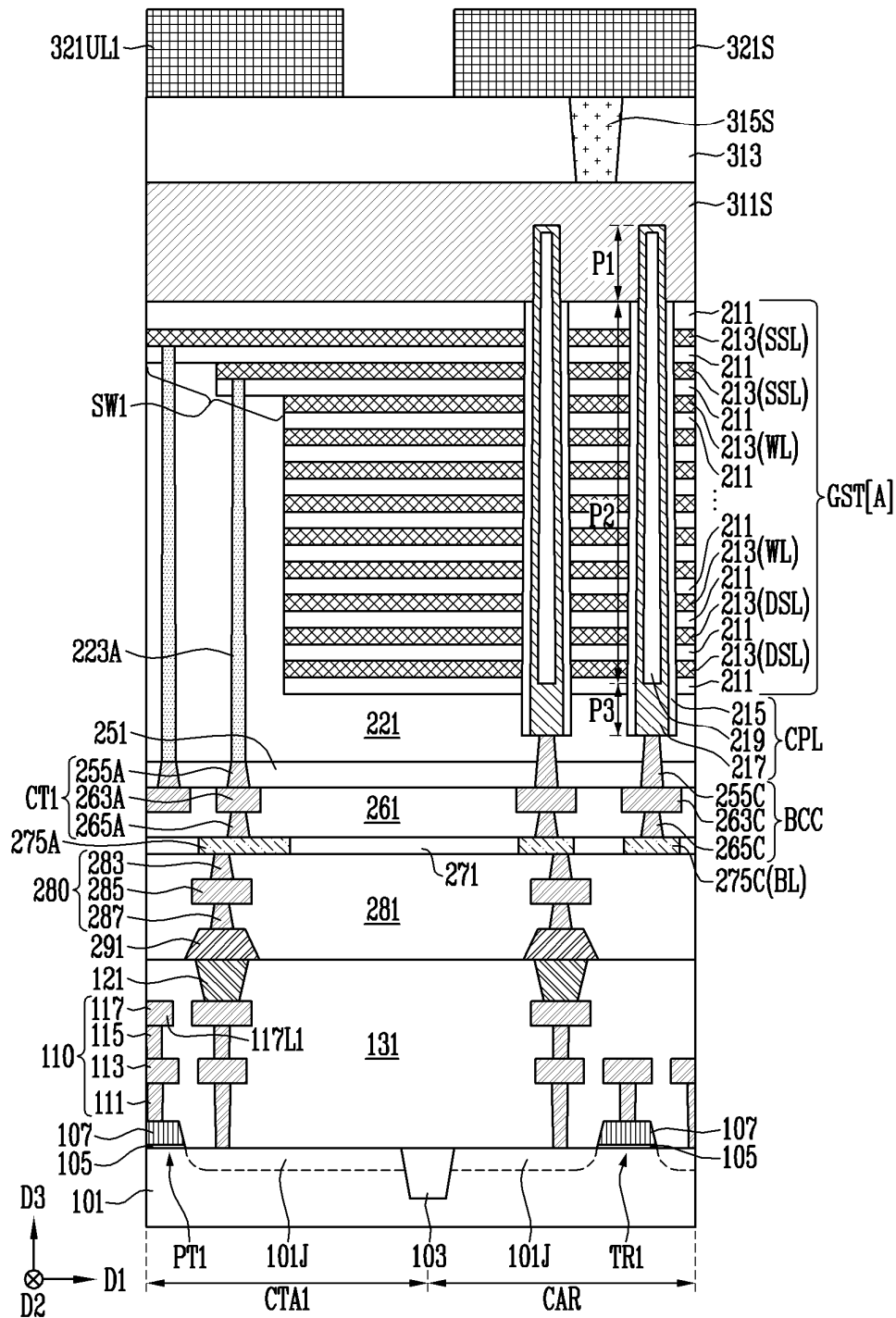


FIG. 5B

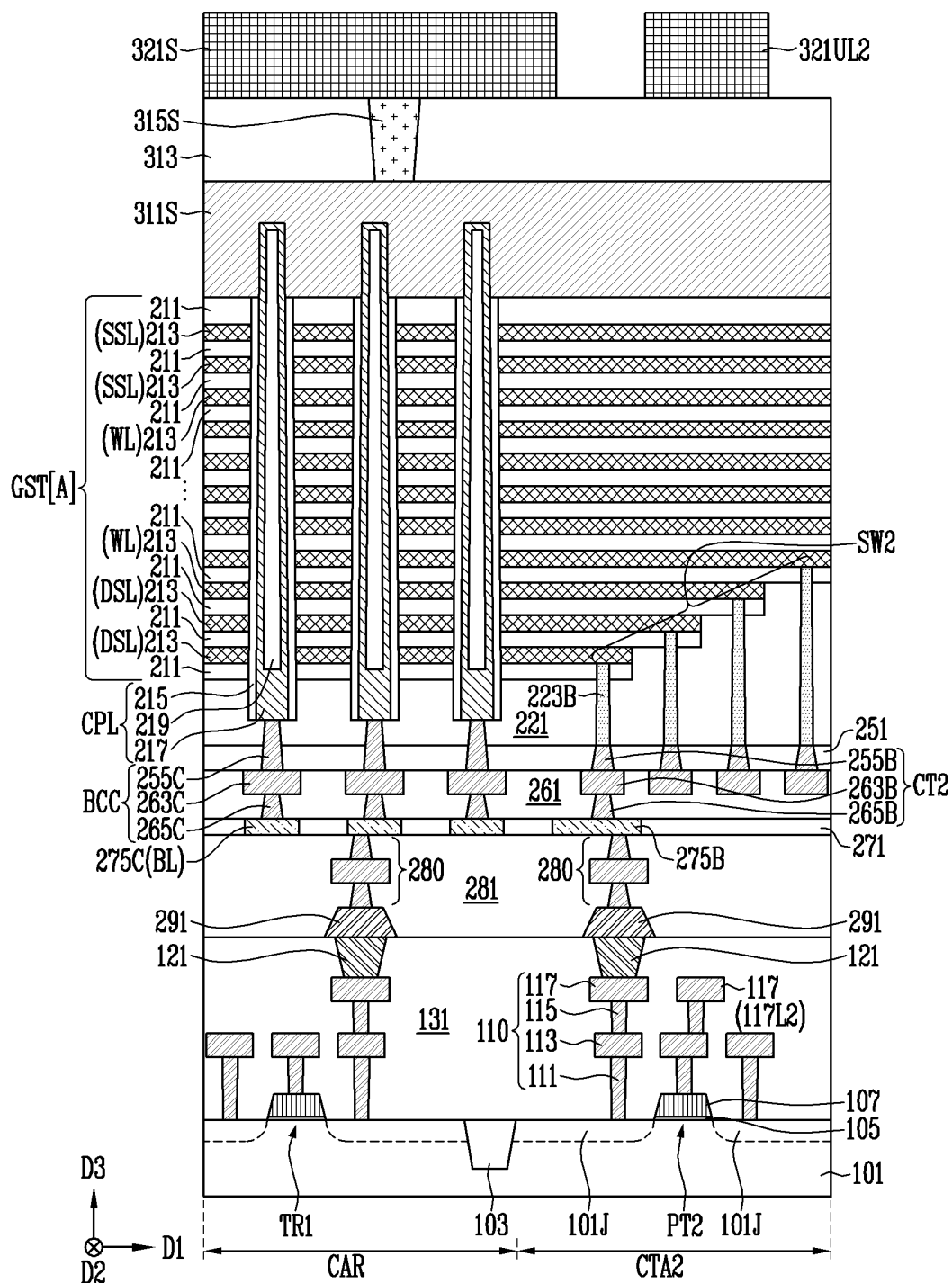


FIG. 5C

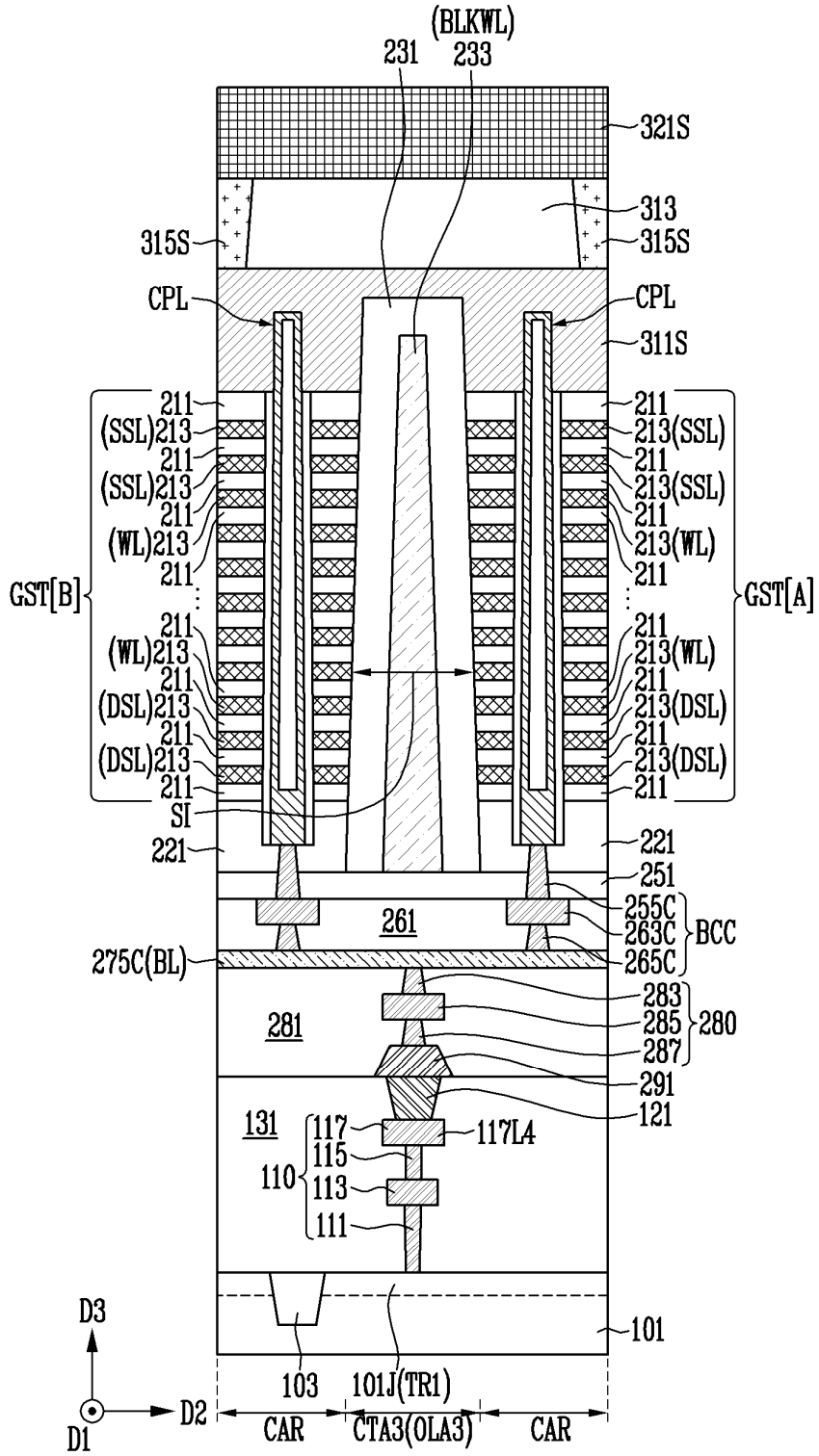


FIG. 5D

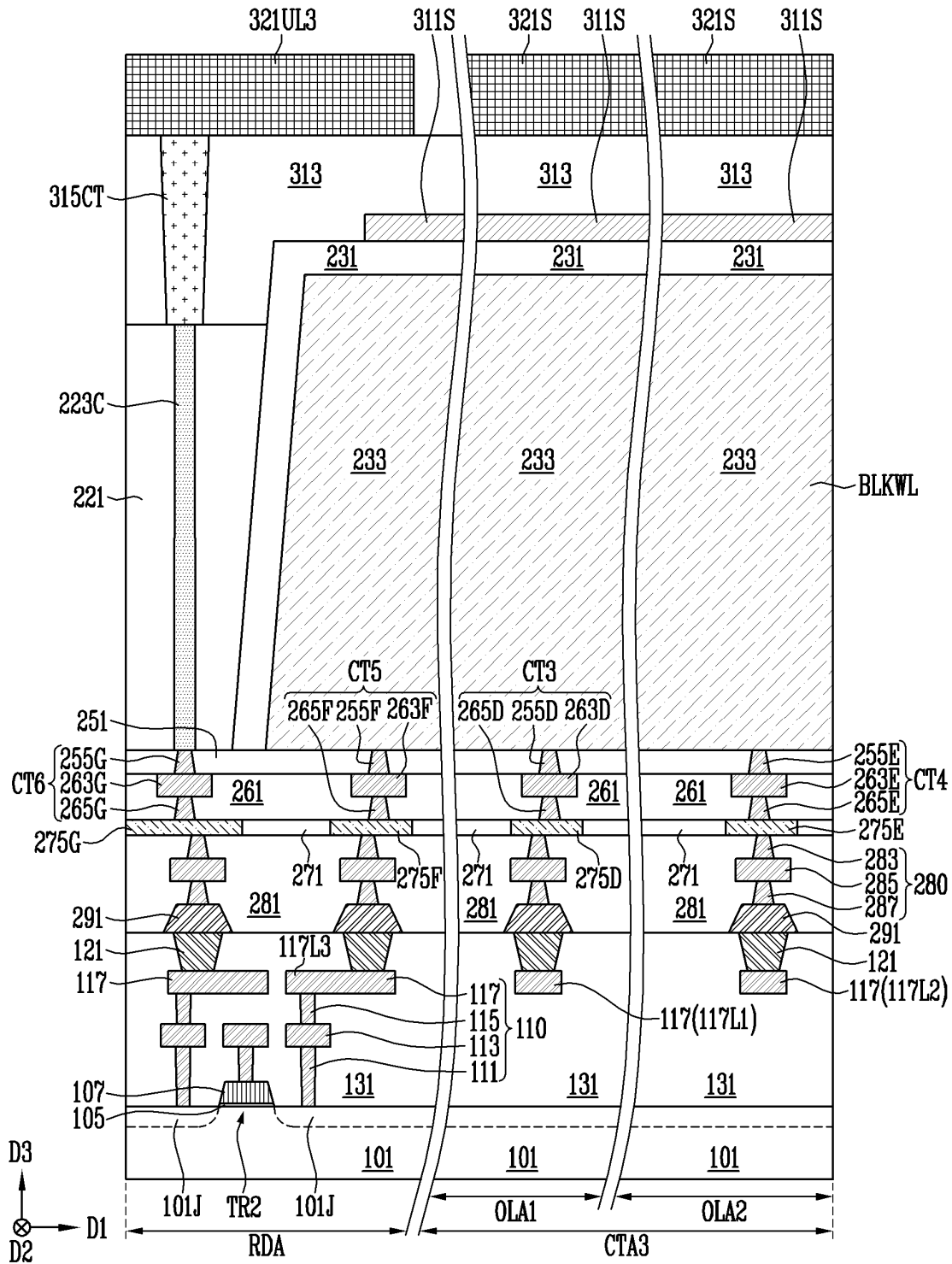


FIG. 6A

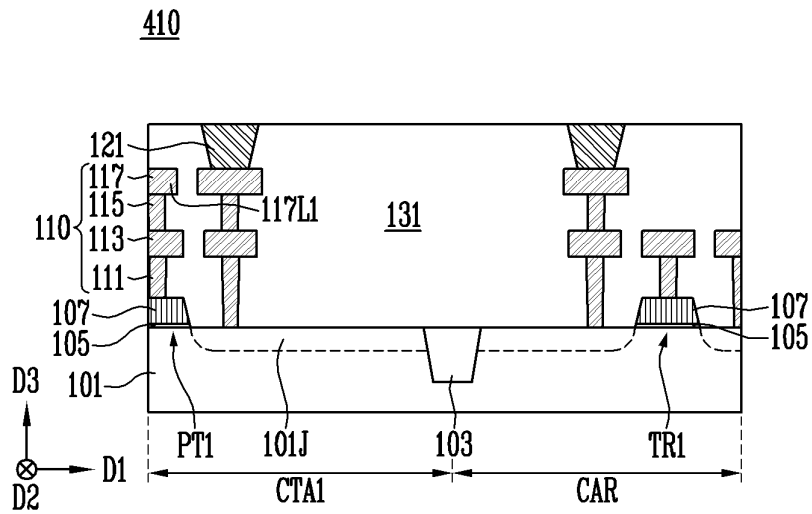


FIG. 6B

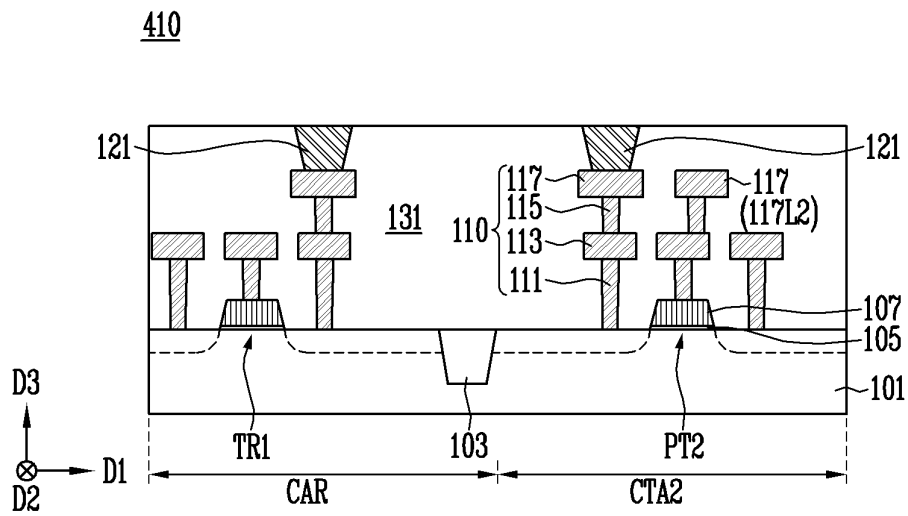


FIG. 6C

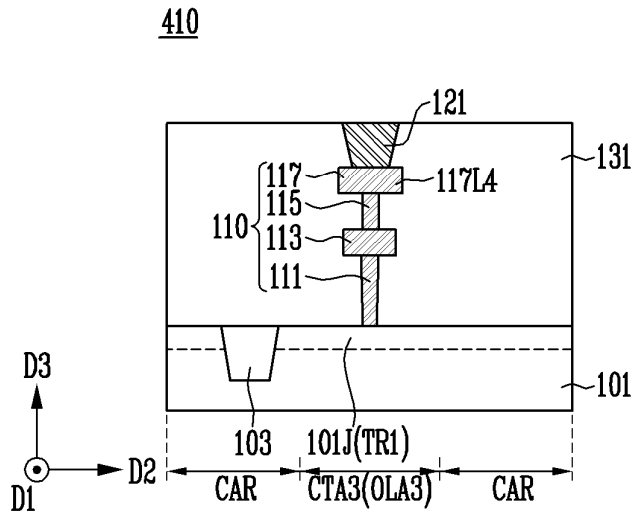


FIG. 6D

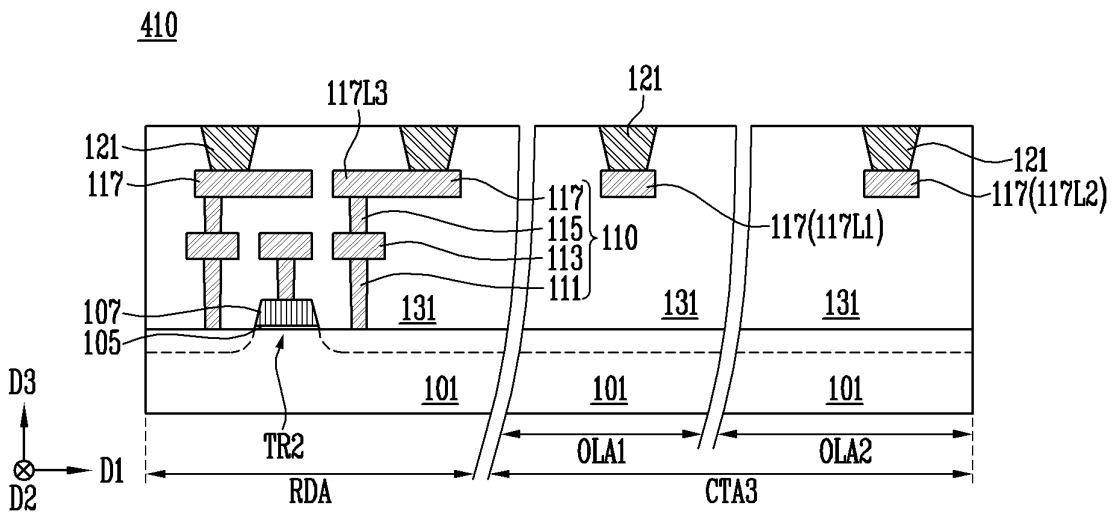


FIG. 7A

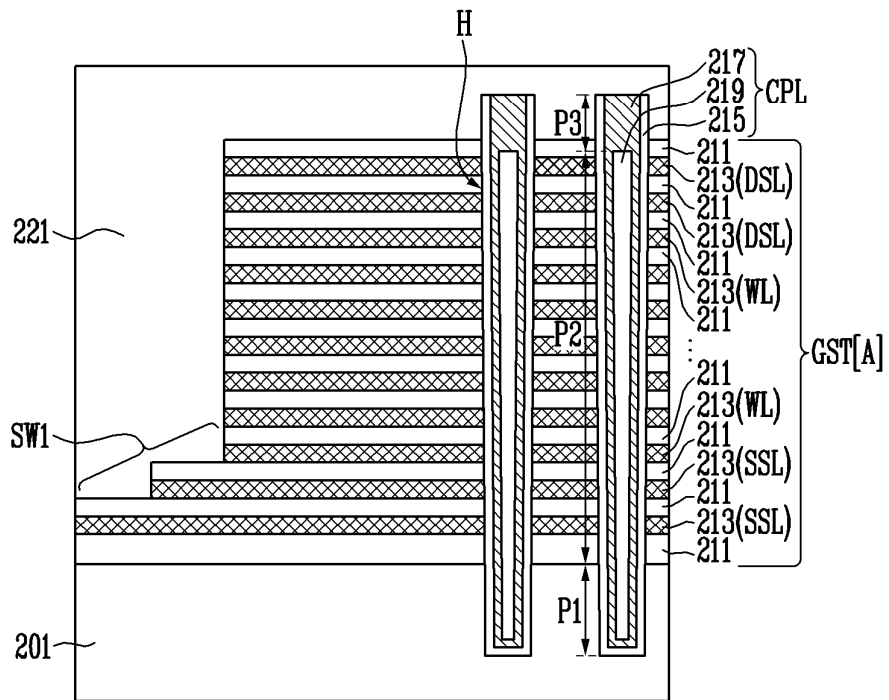


FIG. 7B

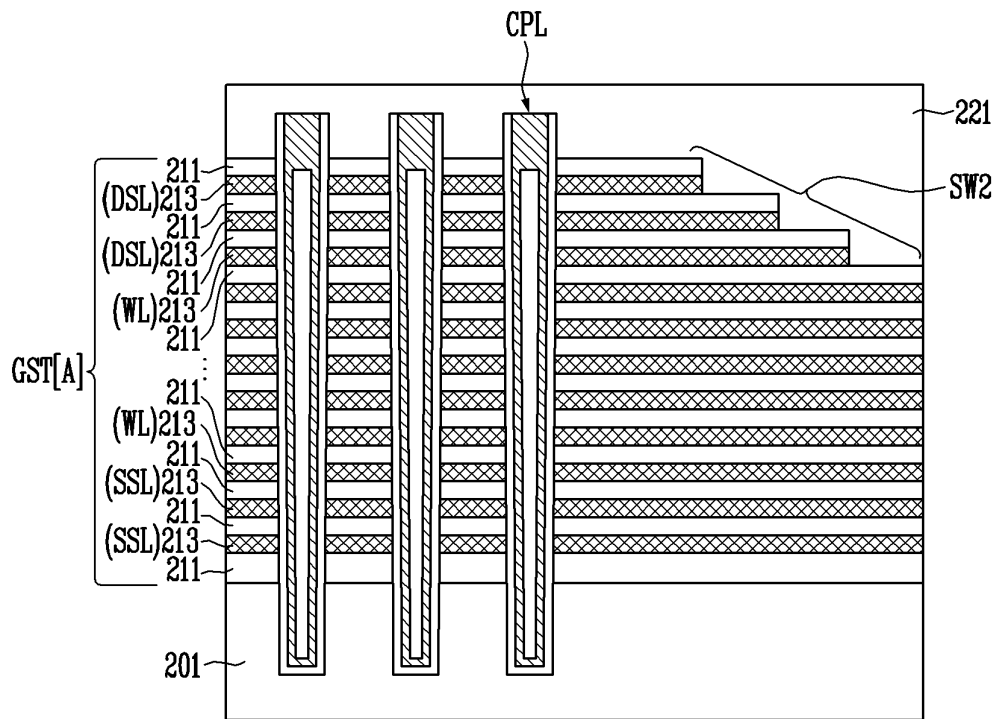


FIG. 7C

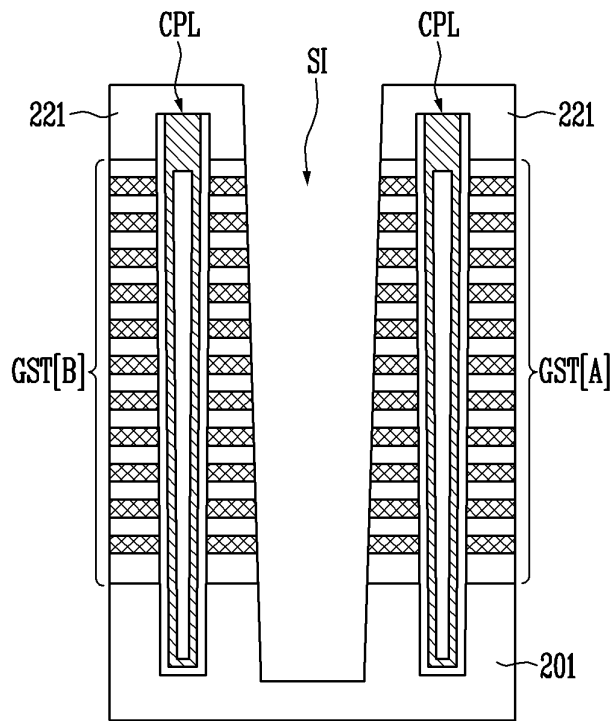


FIG. 7D

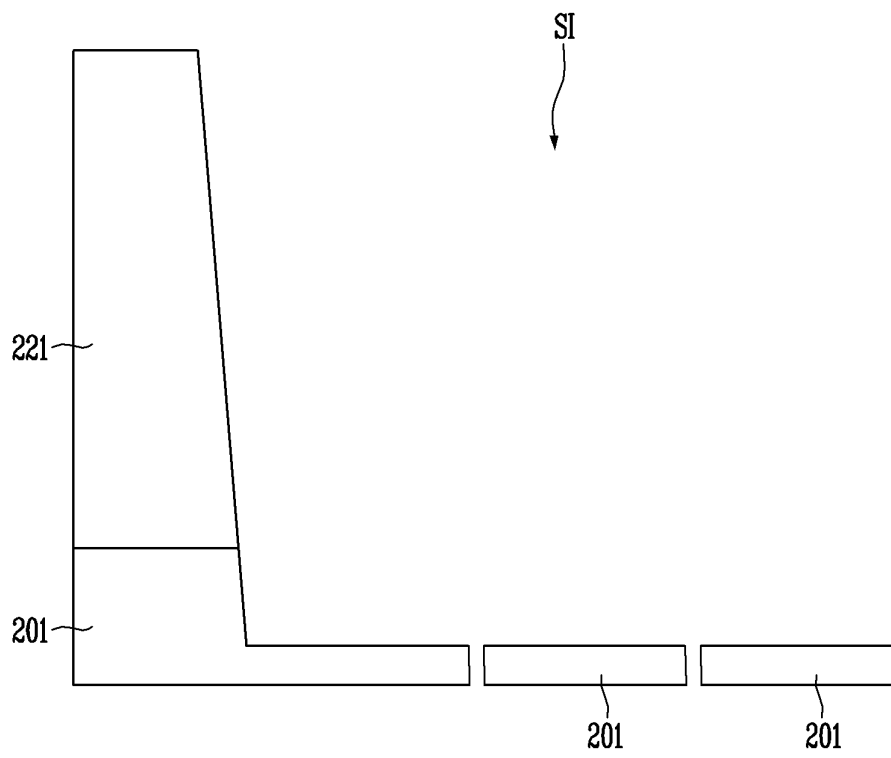


FIG. 8A

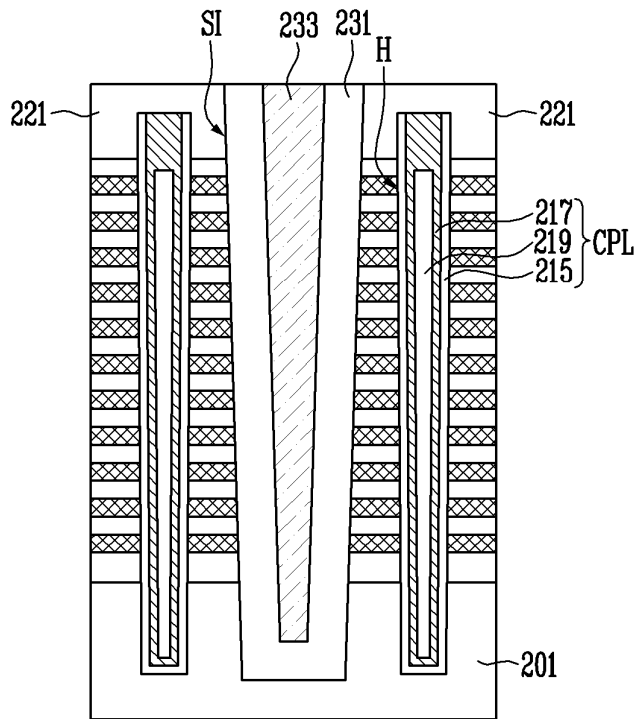


FIG. 8B

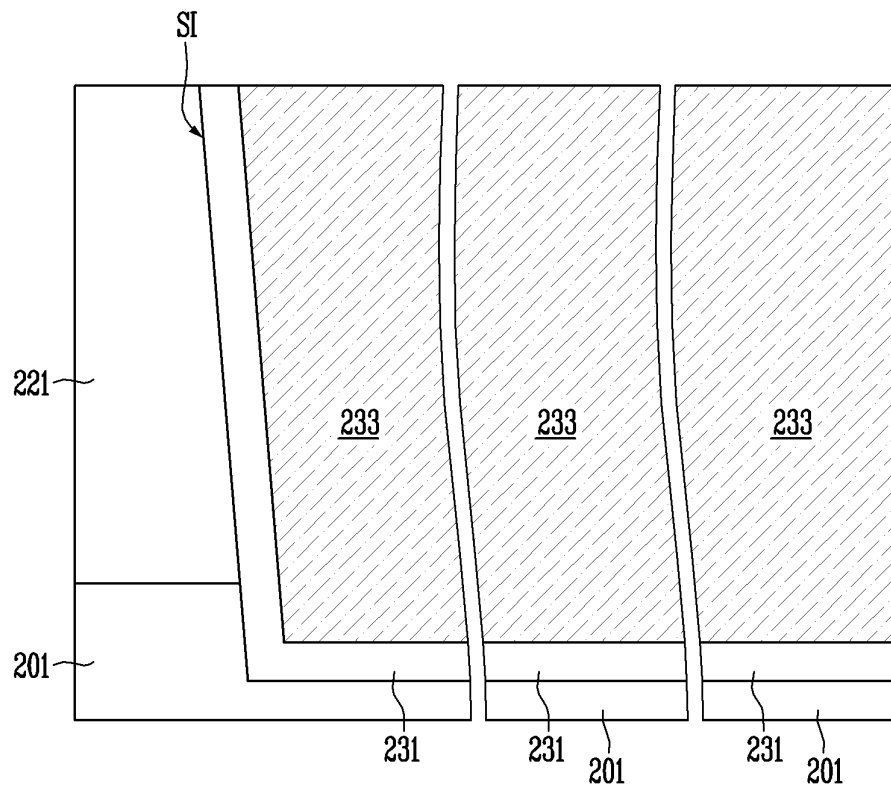
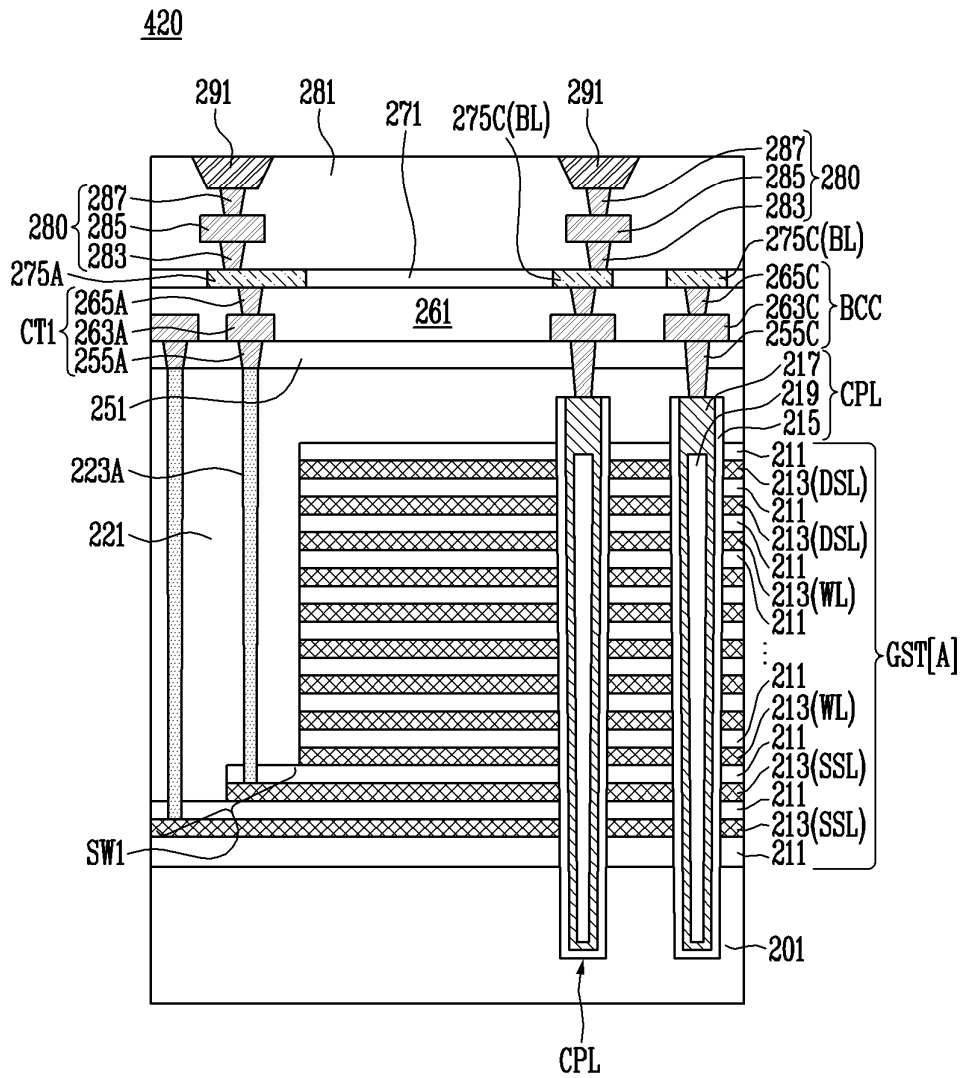


FIG. 9A



This cross-sectional view illustrates a semiconductor device structure. At the bottom is a substrate or base layer labeled 201. Above it is a stack of layers, including a bottom conductive layer (CPL) and a series of alternating layers: GST[A], (DSL), (WL), (SSL), and another (SSL). Vertical structures (221, 223B) are formed through these layers. The top of the device features a stack of layers including 251, 261, 263B, 265B, 265C, 271, 275B, and 281. Various conductive contacts and interconnects are labeled with numbers 201 through 291, including a central contact 261 and side contacts 263B and 265B. The topmost layer is labeled 281.

FIG. 9C

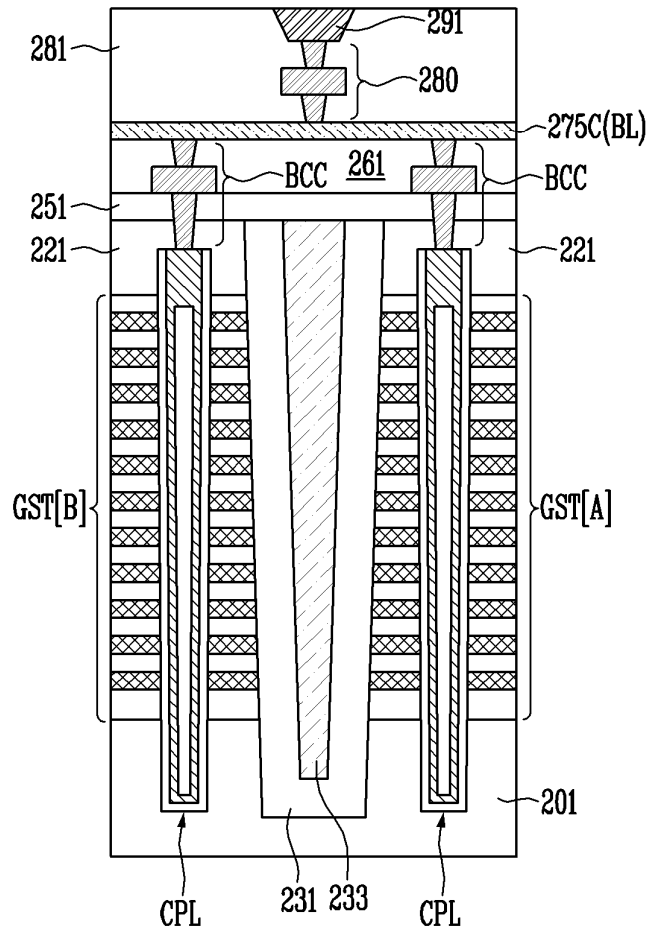
420

FIG. 9D

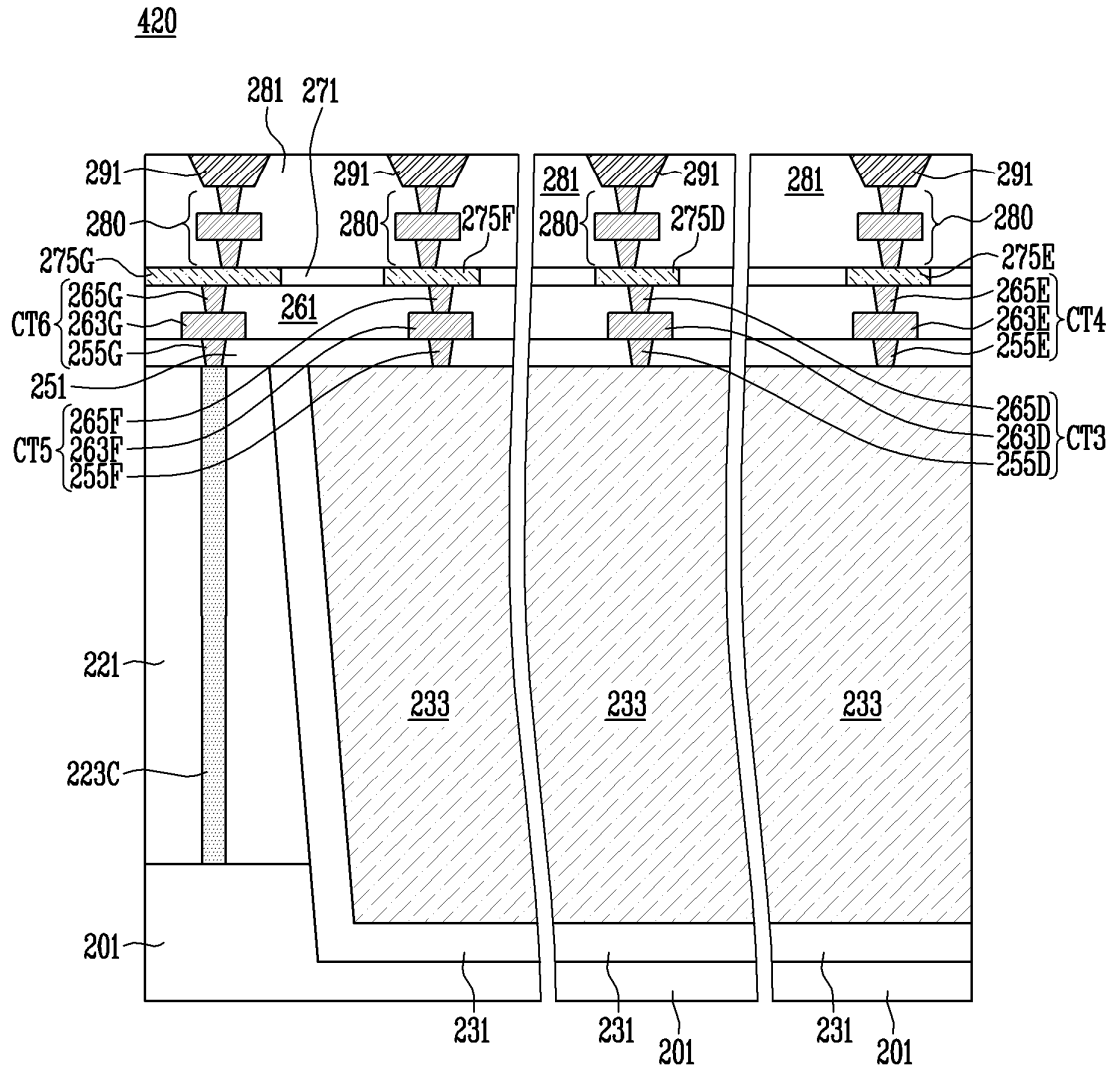


FIG. 10A

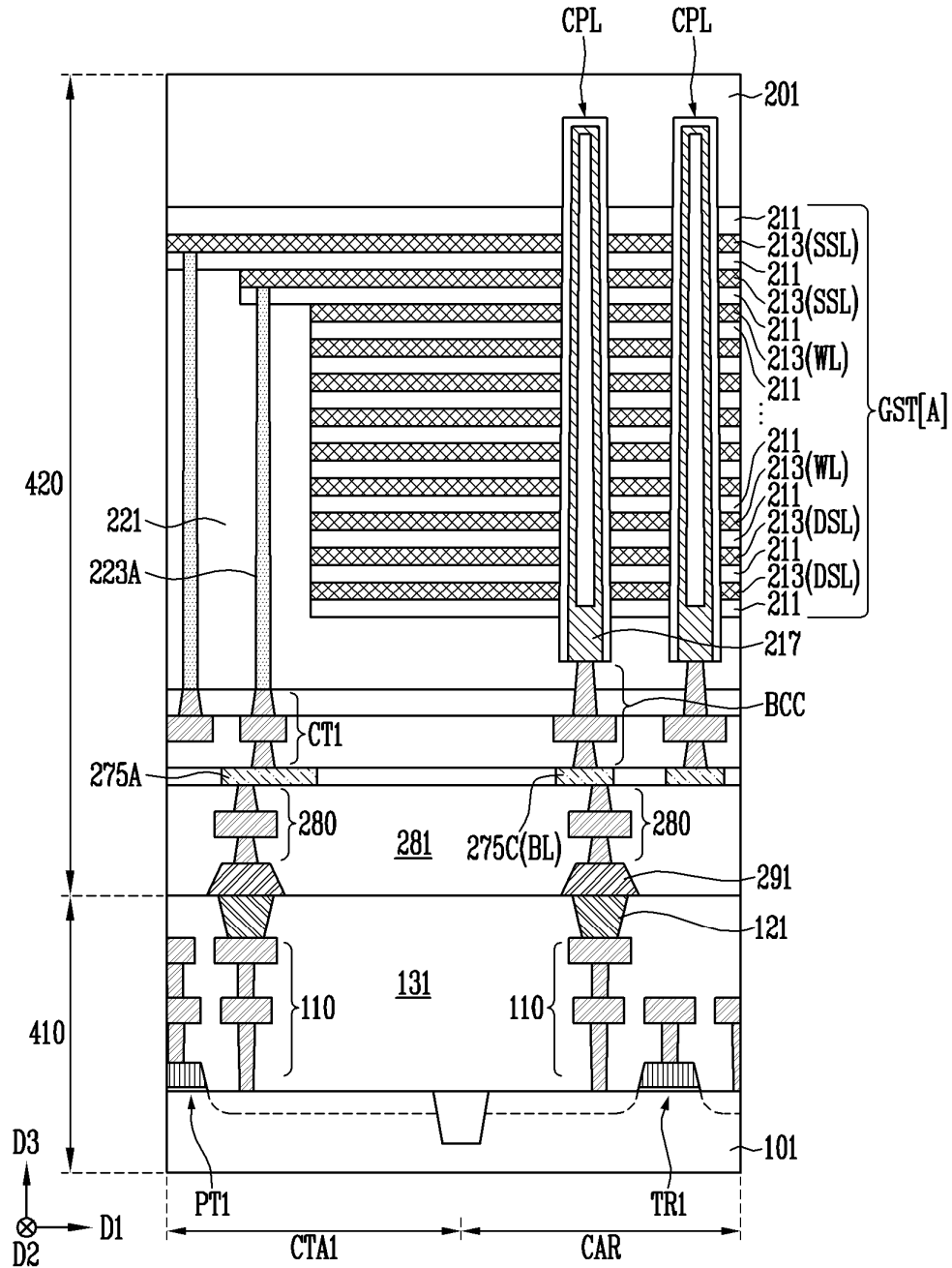


FIG. 10B

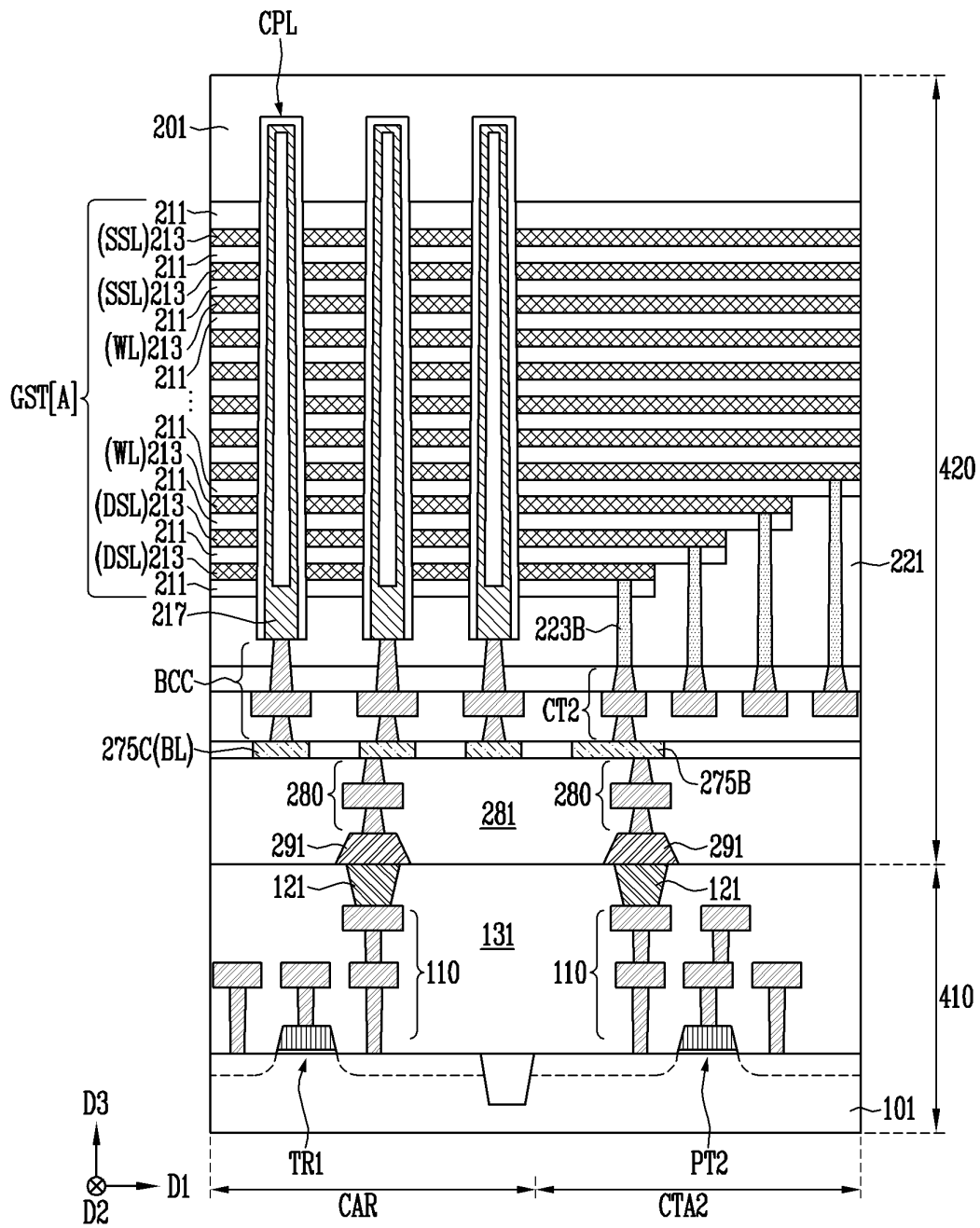


FIG. 10C

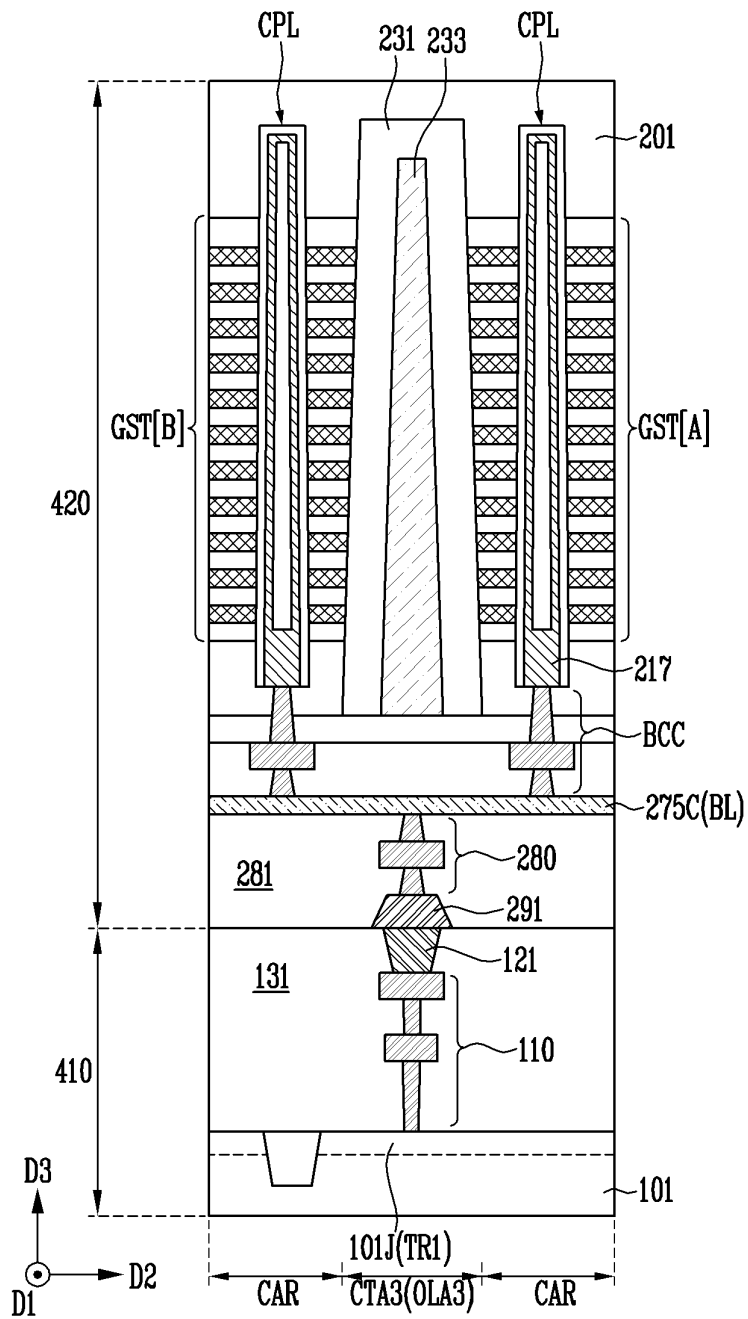


FIG. 10D

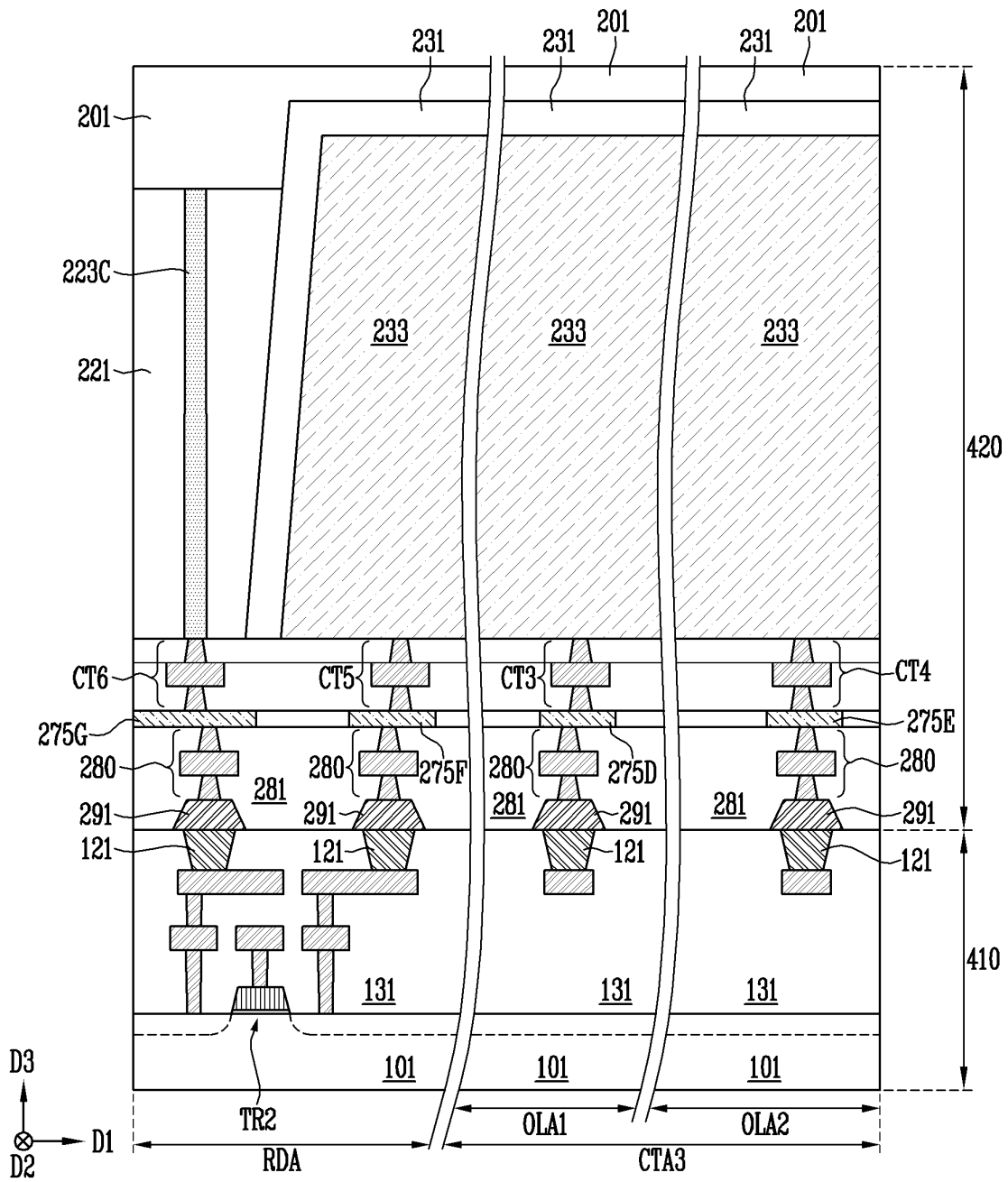


FIG. 11A

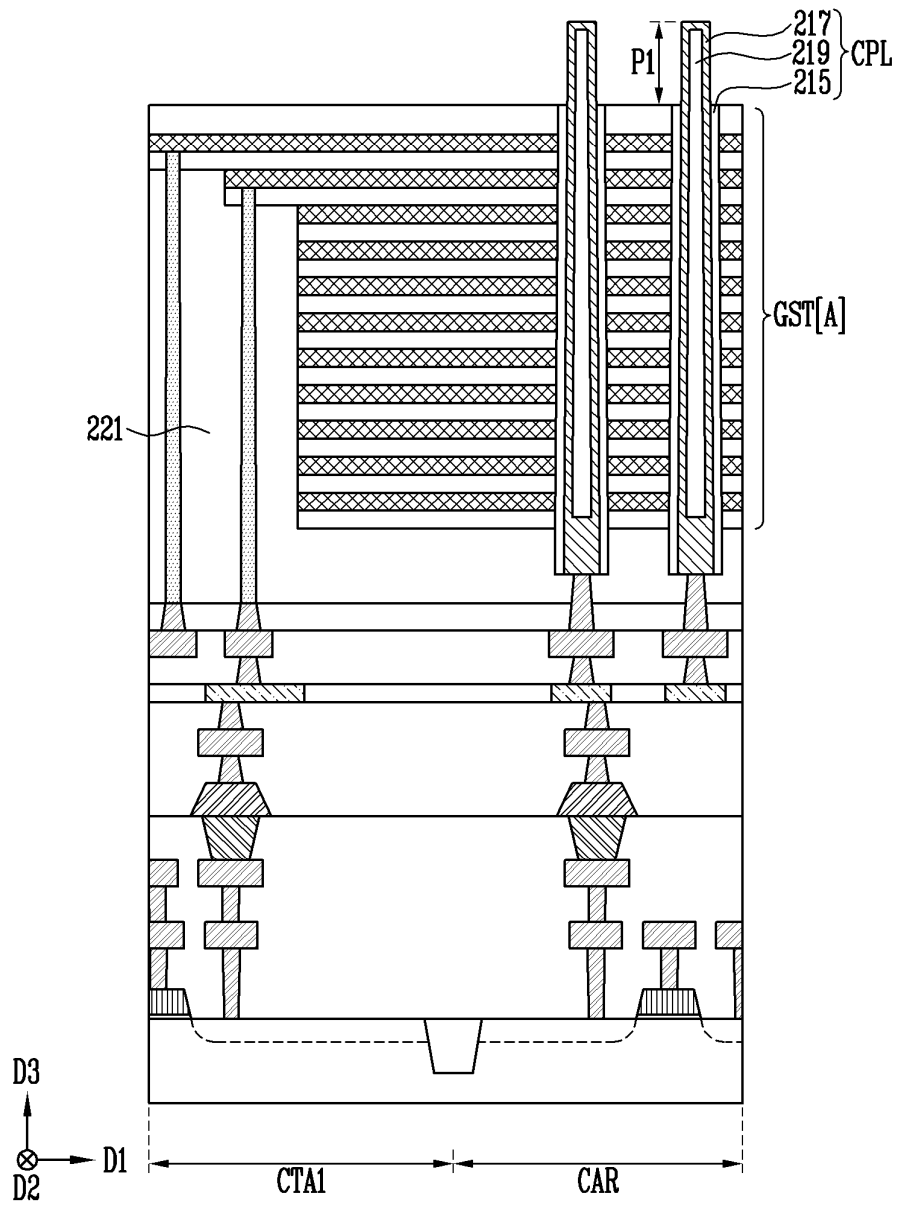


FIG. 11B

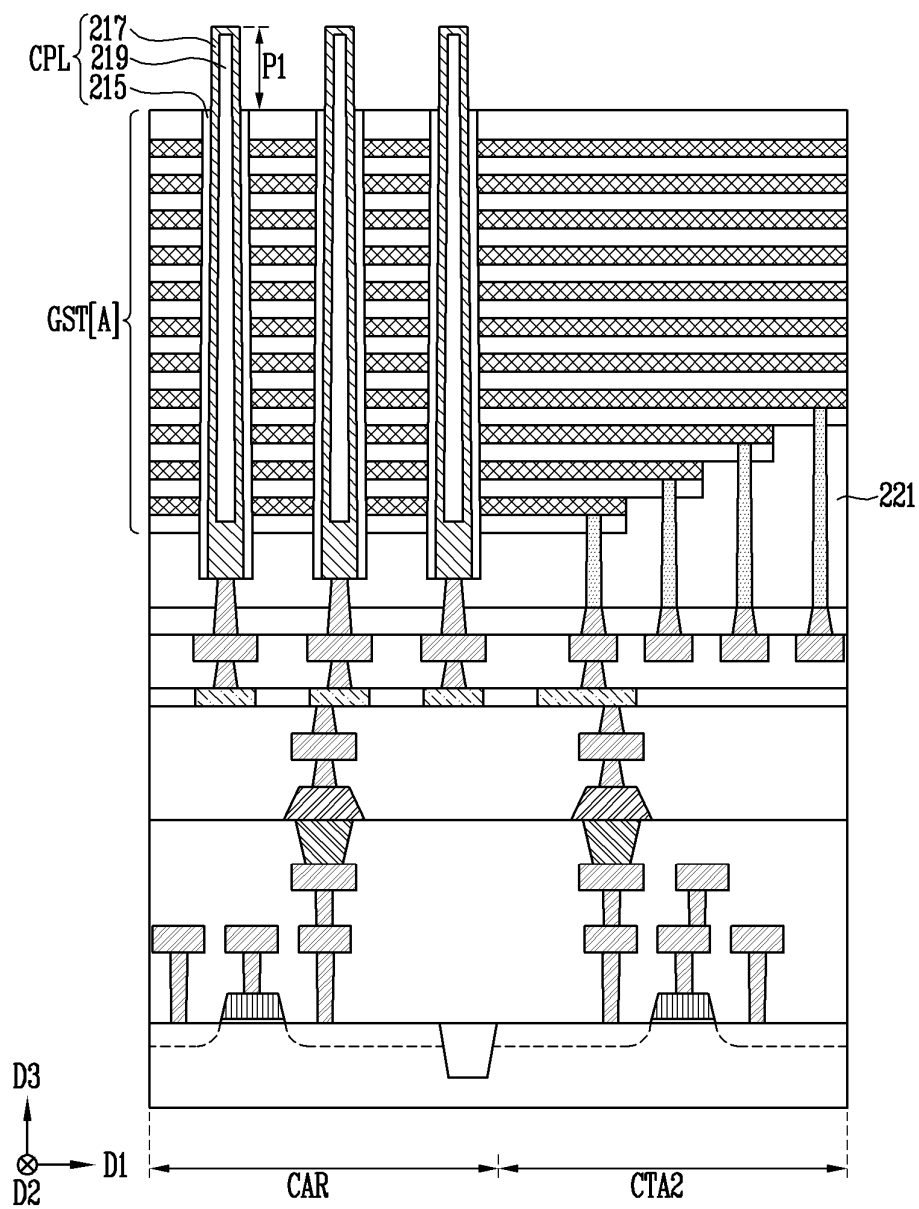


FIG. 11C

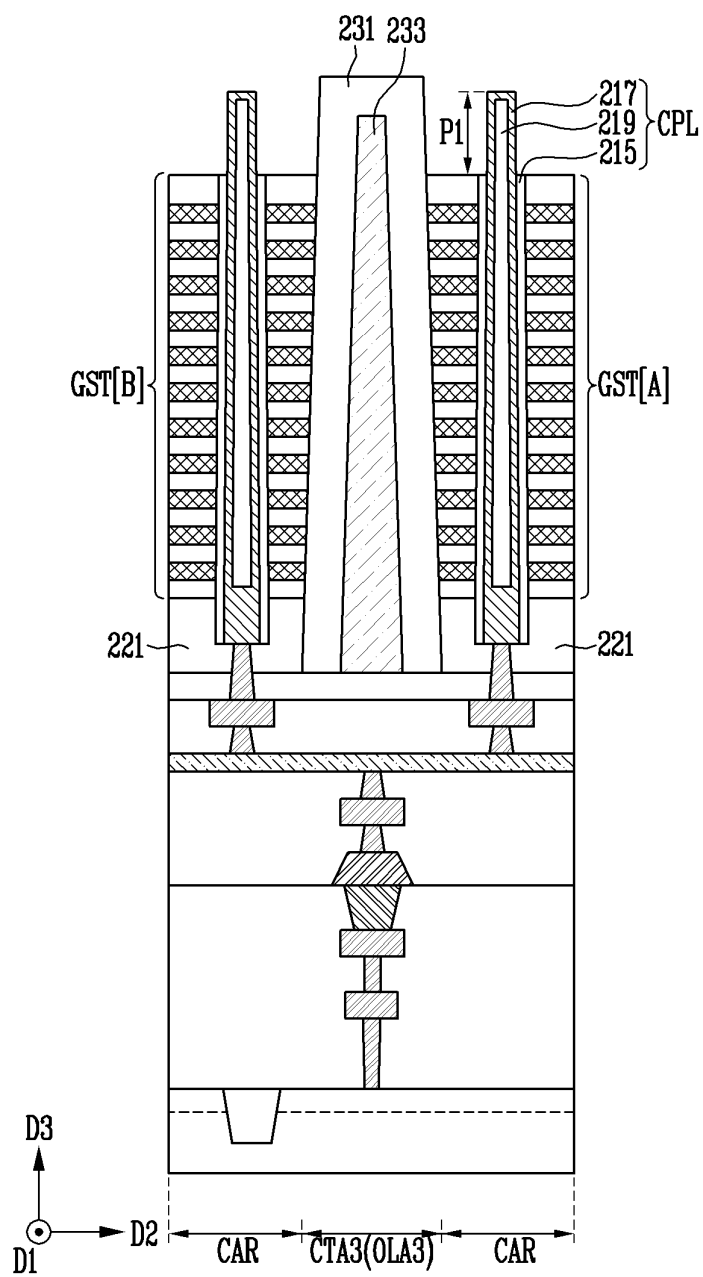


FIG. 11D

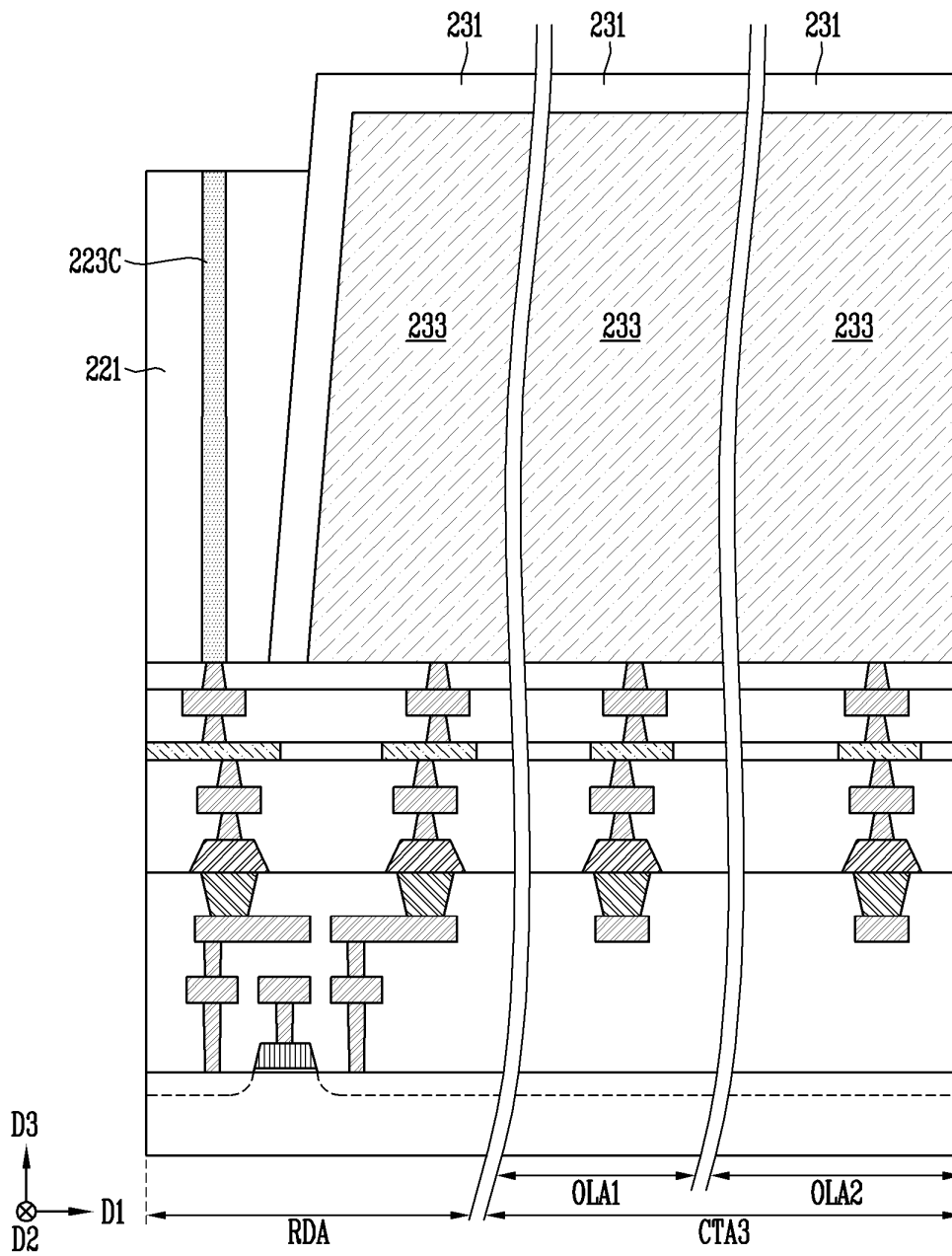


FIG. 12A

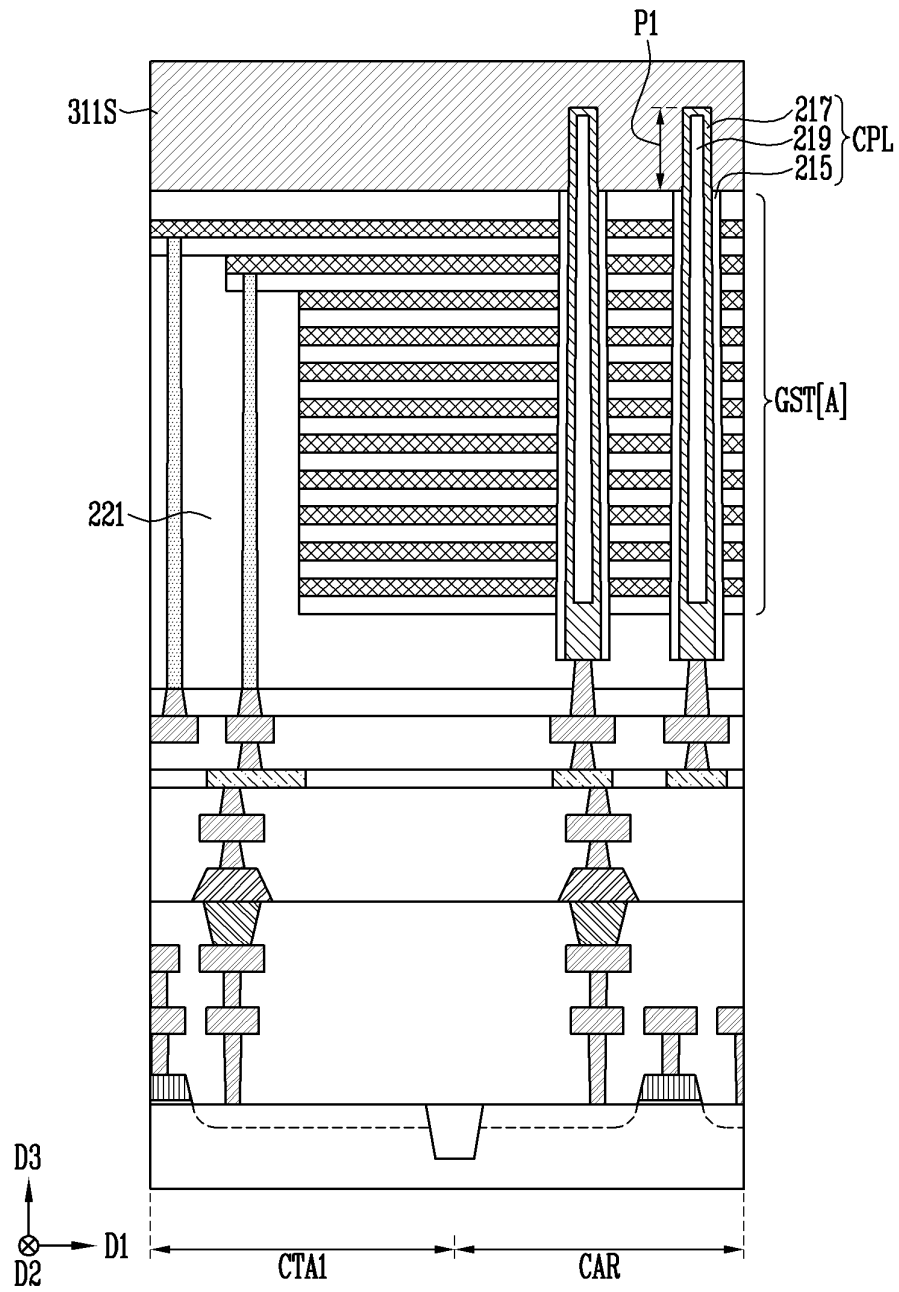


FIG. 12B

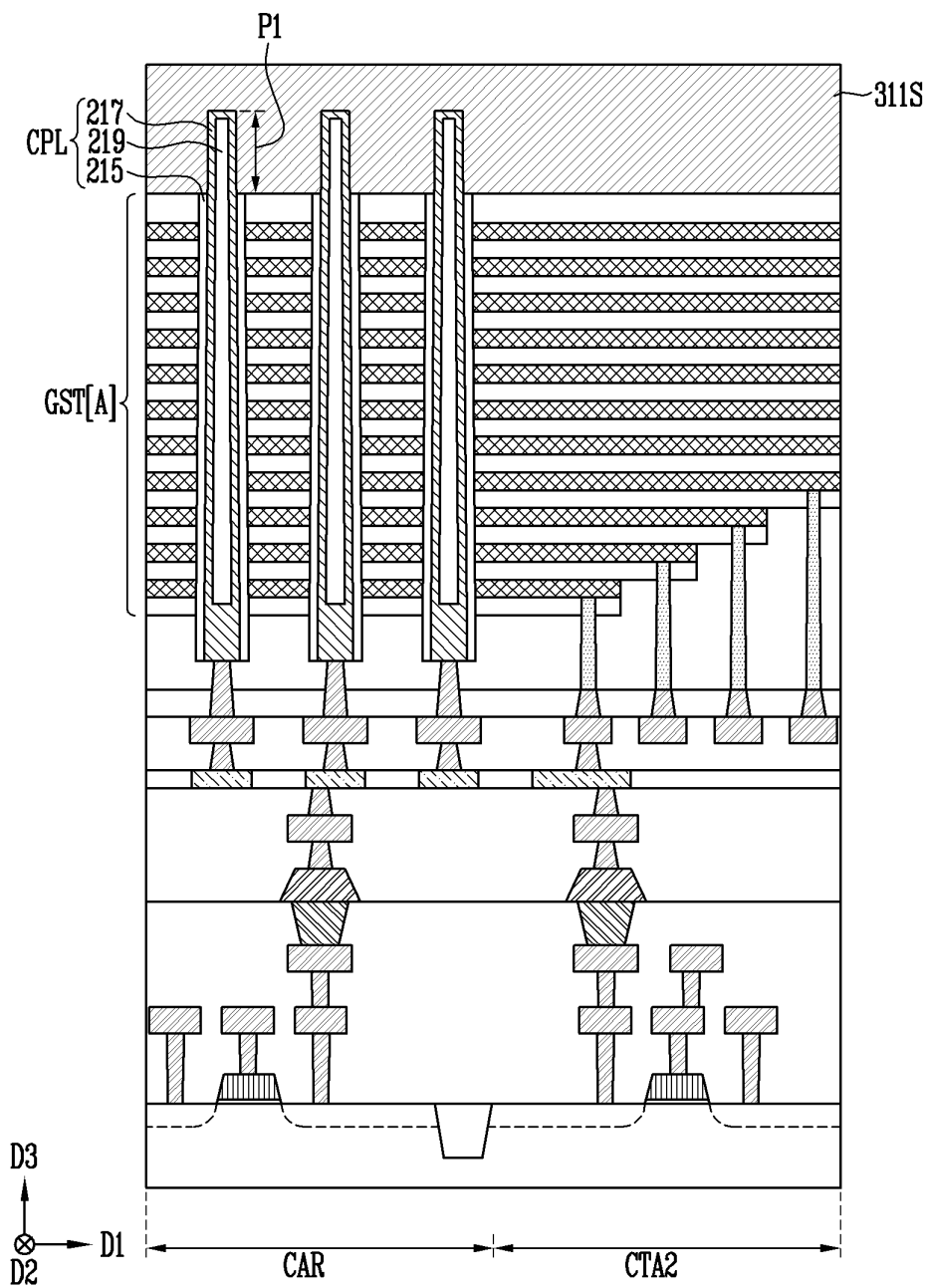


FIG. 12C

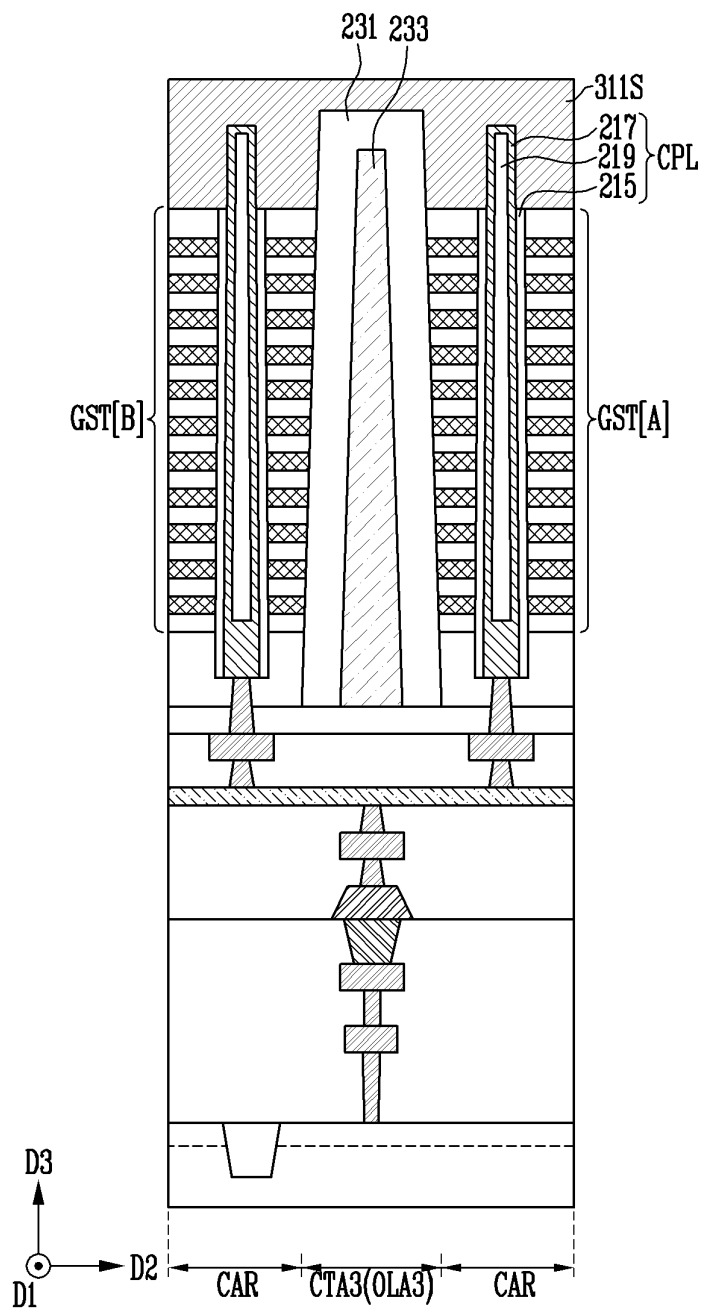


FIG. 12D

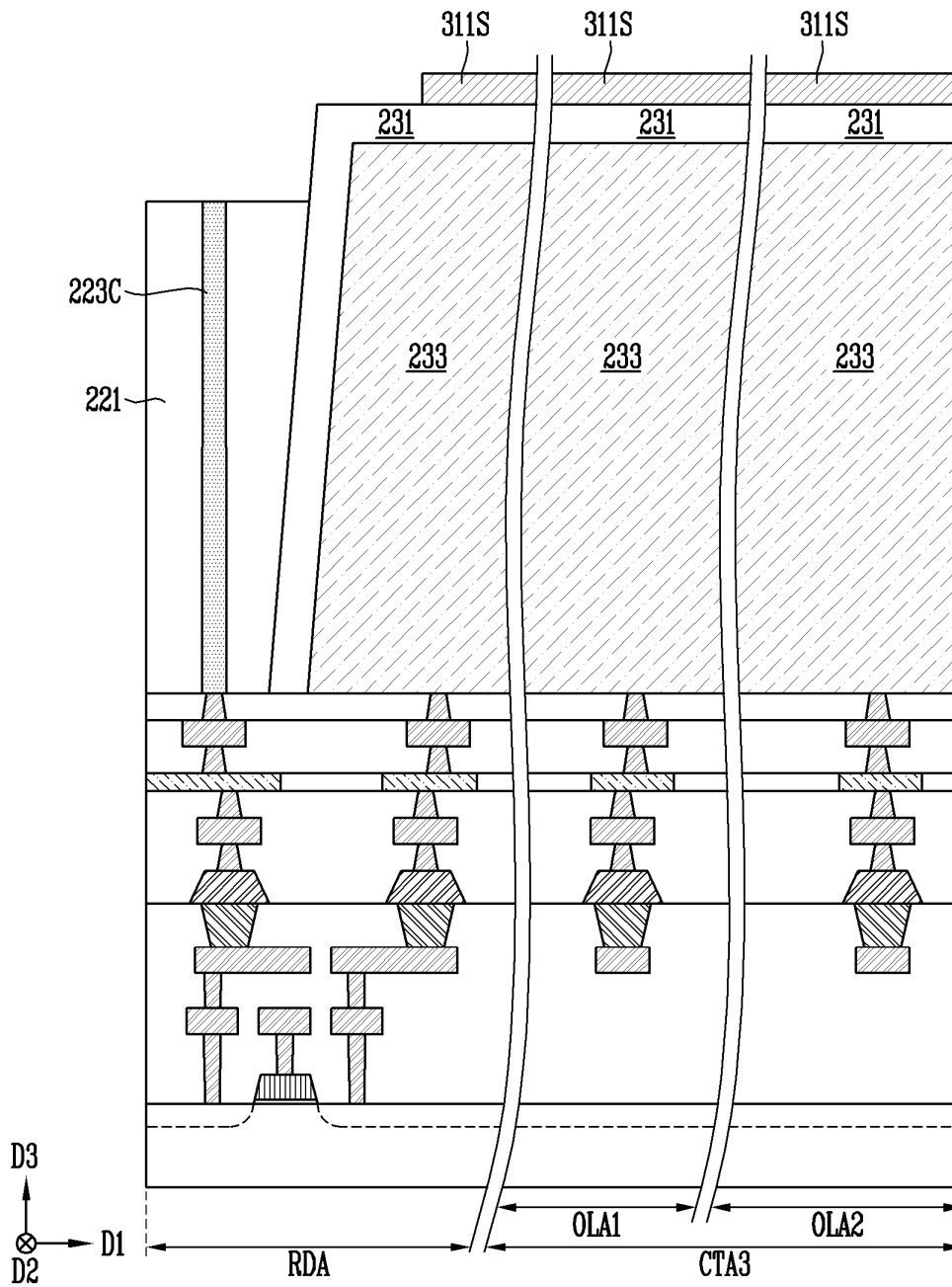


FIG. 13

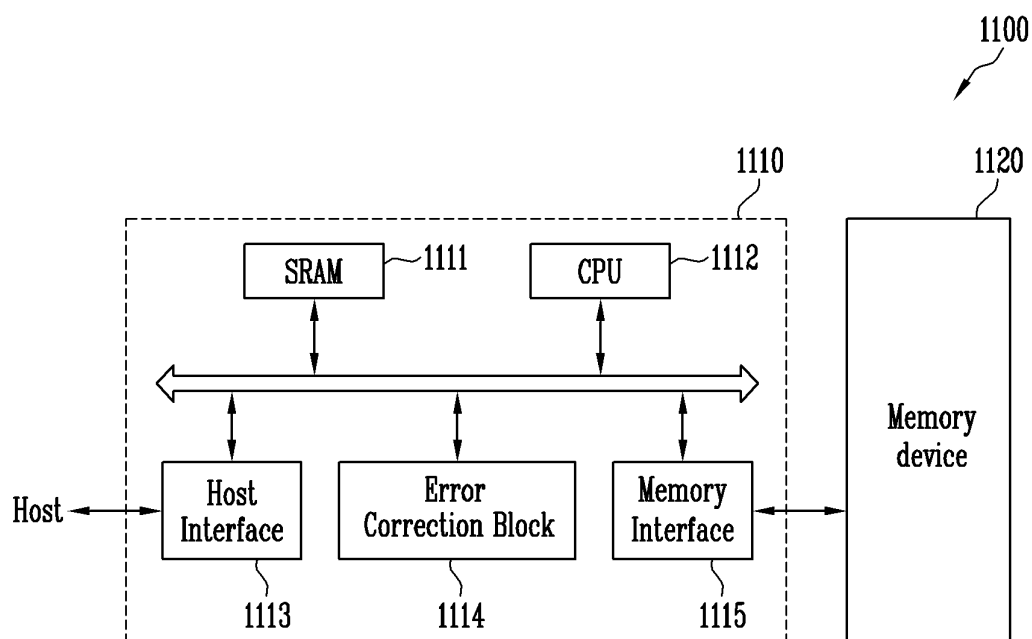


FIG. 14

