

1/15

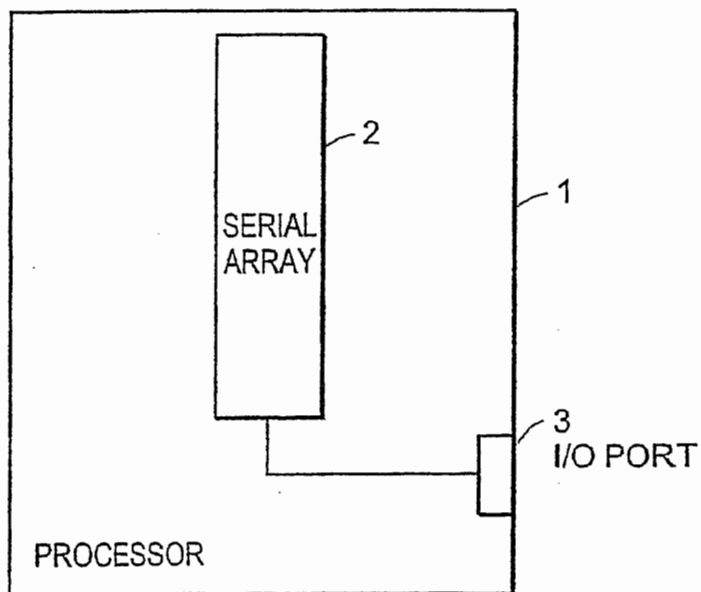


FIG. 1
PRIOR ART

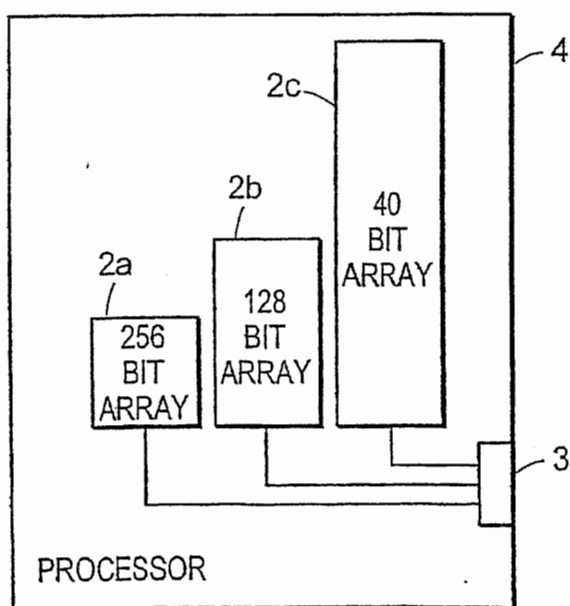


FIG. 2
PRIOR ART

PIPELINE PROCESSOR

ARRAY ARRAY

6a 6b

6c

ARRAY

LOGIC CIRCUIT

PORT

9 7

The diagram shows a system architecture. On the left is a large vertical rectangle labeled "ARRAY" with reference numeral 6a. To its right is a narrower vertical rectangle labeled "PROCESSOR ARRAY" with reference numeral 11. Inside the "PROCESSOR ARRAY", there are several horizontal rectangular blocks. The top two are connected to output lines labeled 8^n and 8^{n-1} . Below them are vertical ellipsis dots. Further down, three more blocks are connected to output lines labeled 8^3 , 8^2 , and 8^1 . A line labeled 9 originates from the bottom of the "ARRAY" block. This line splits: one branch goes through a break symbol (two parallel wavy lines) to an "I/O PORT" block (3), and the other branch goes to a "LOGIC CIRCUIT" block (7). The "I/O PORT" block (3) is also connected to the "LOGIC CIRCUIT" block (7).

FIG. 3B

3/15

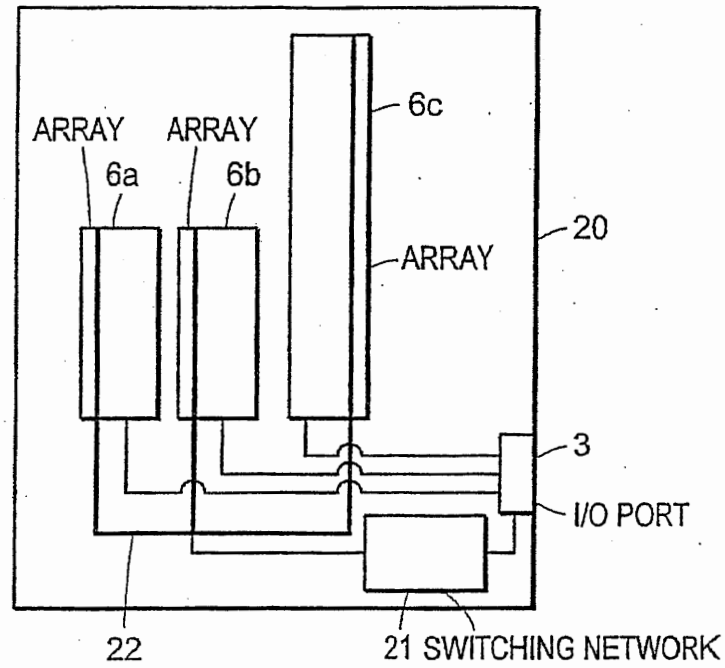


FIG. 4A

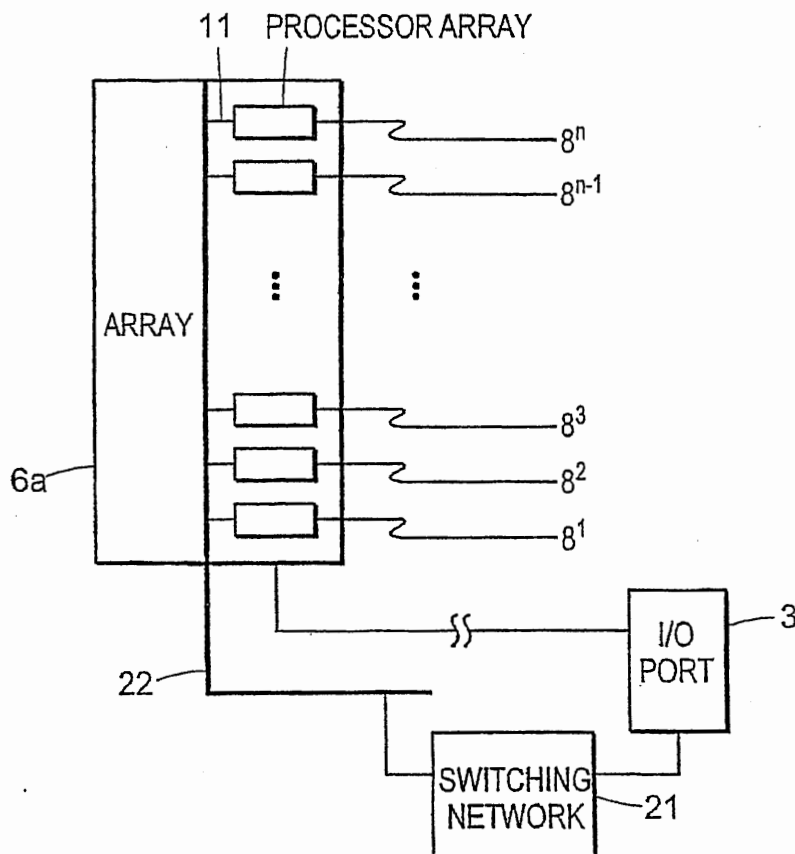


FIG. 4B

4/15

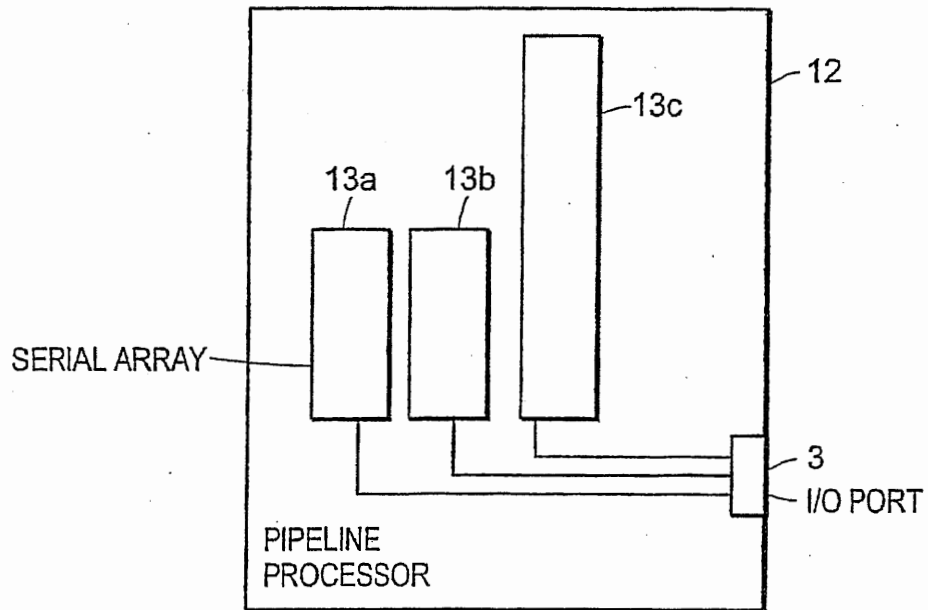


FIG. 5A

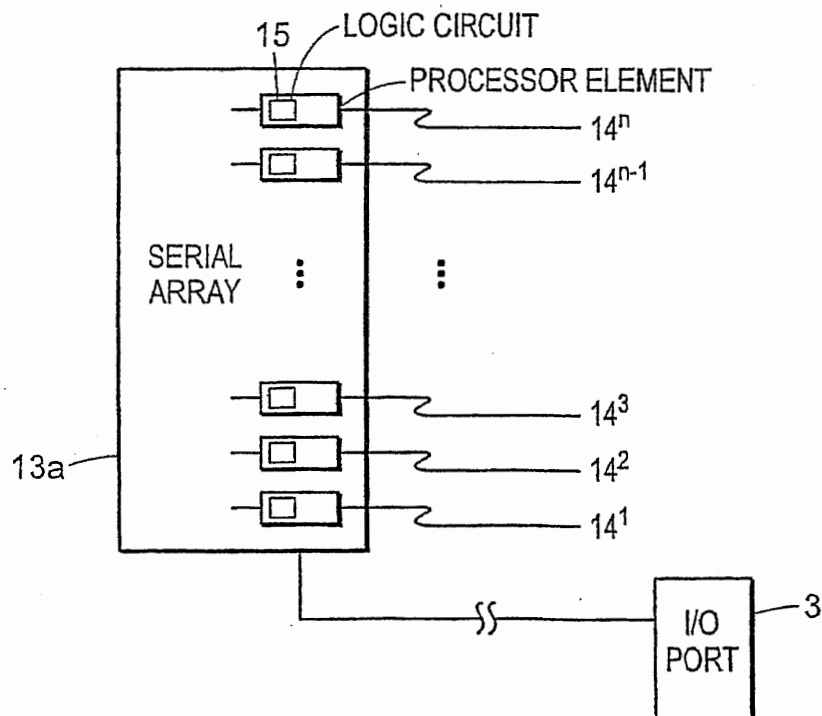


FIG. 5B

5/15

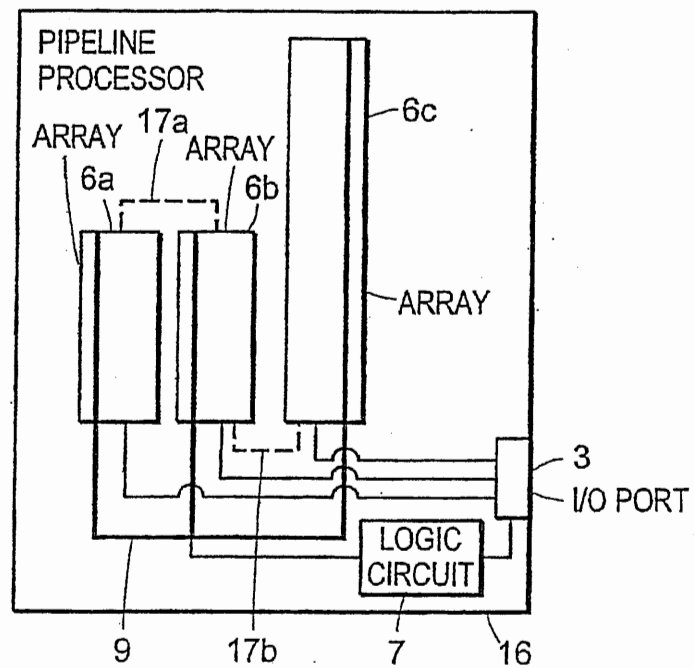


FIG. 6

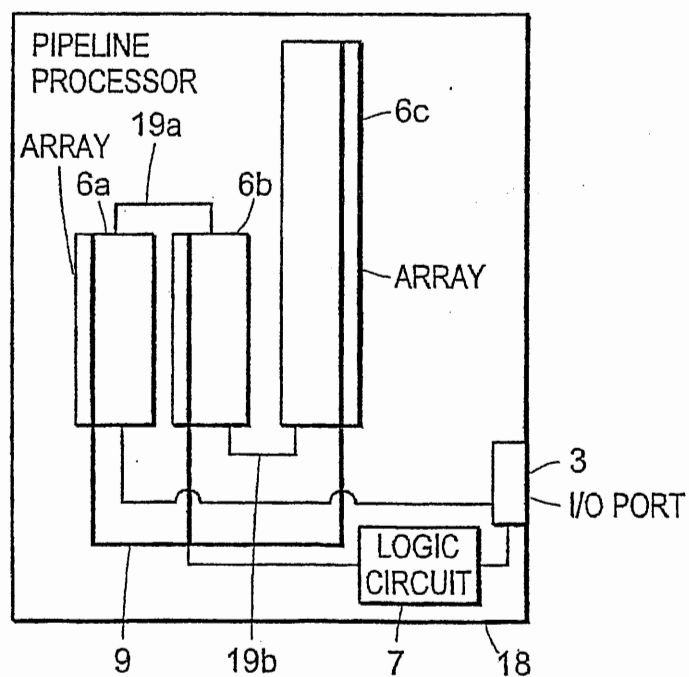


FIG. 7

6/15

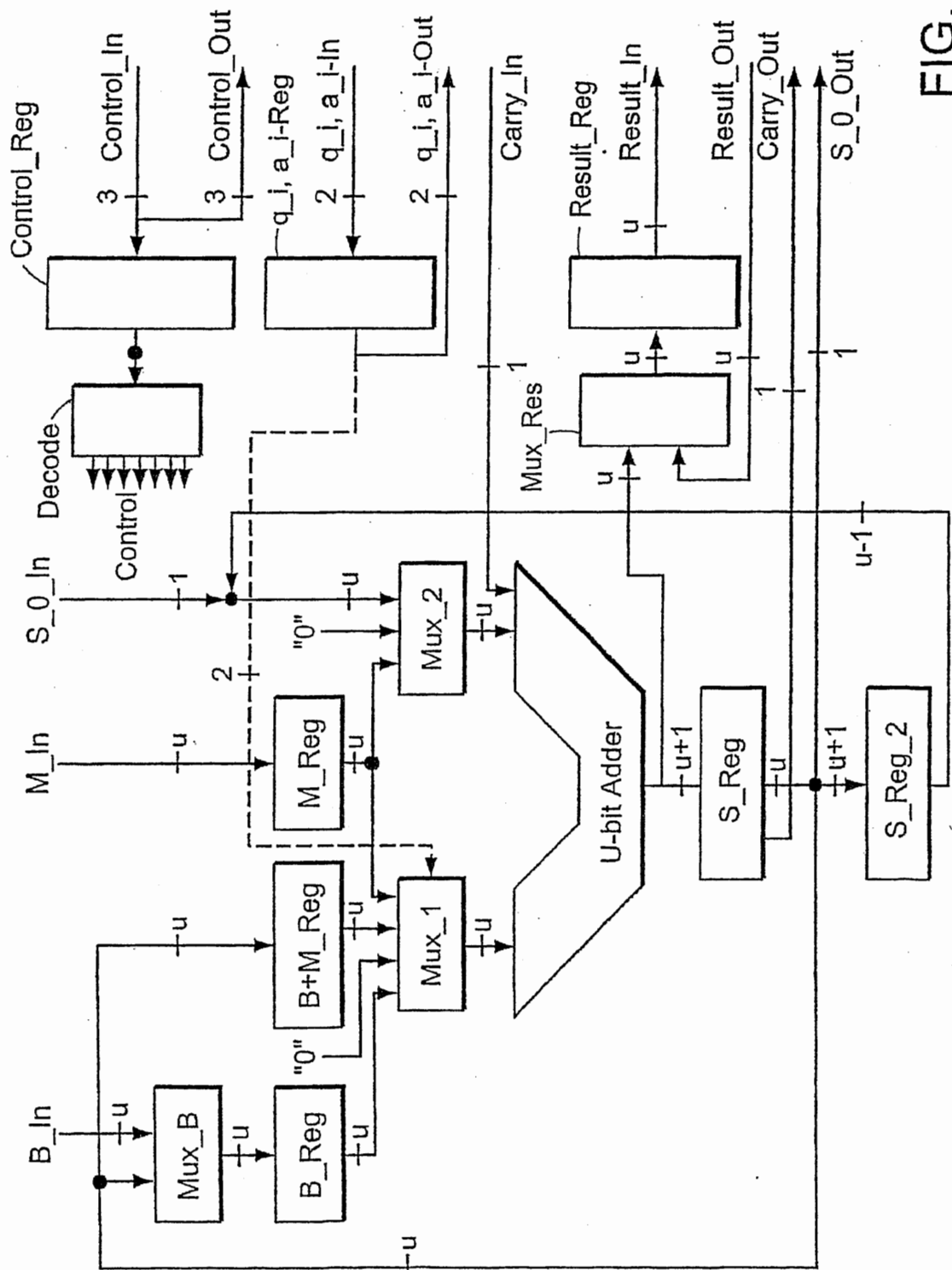


FIG. 8

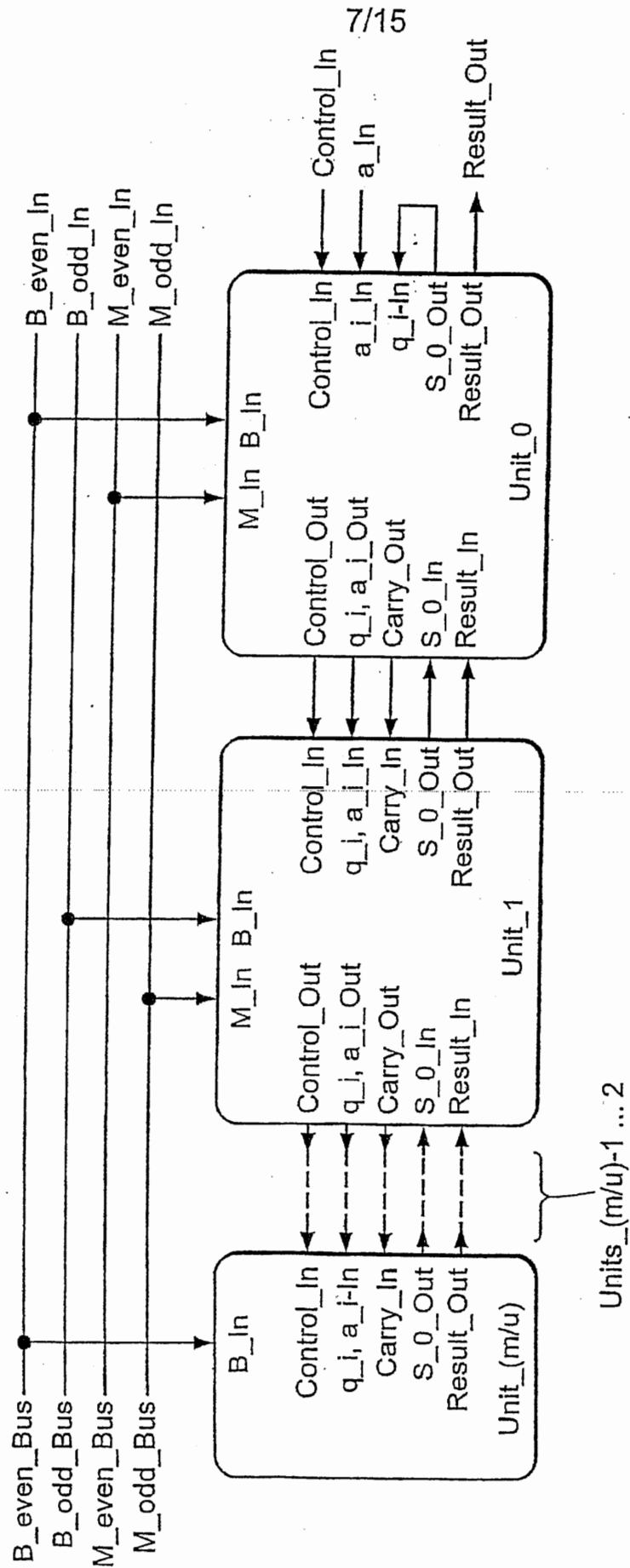


FIG. 9

8/15

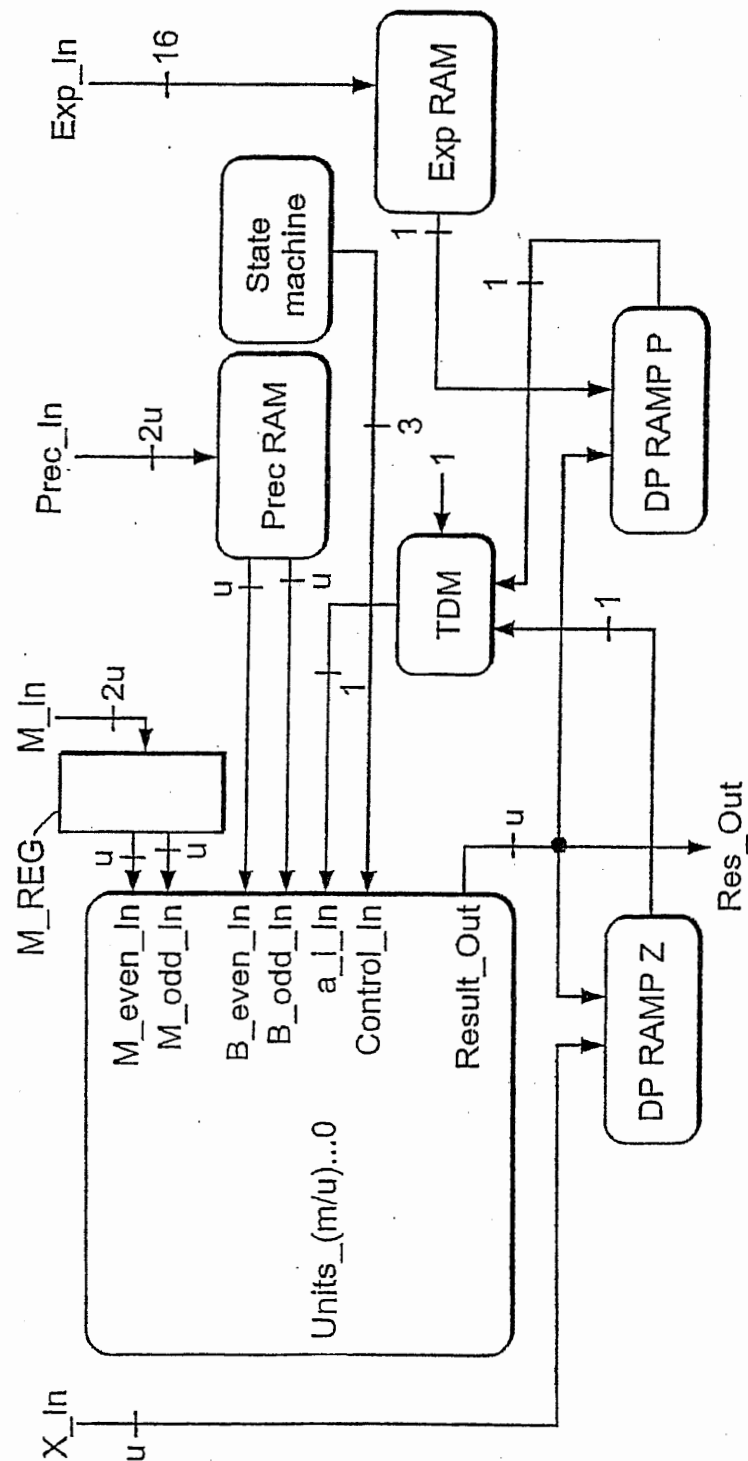


FIG. 10

9/15

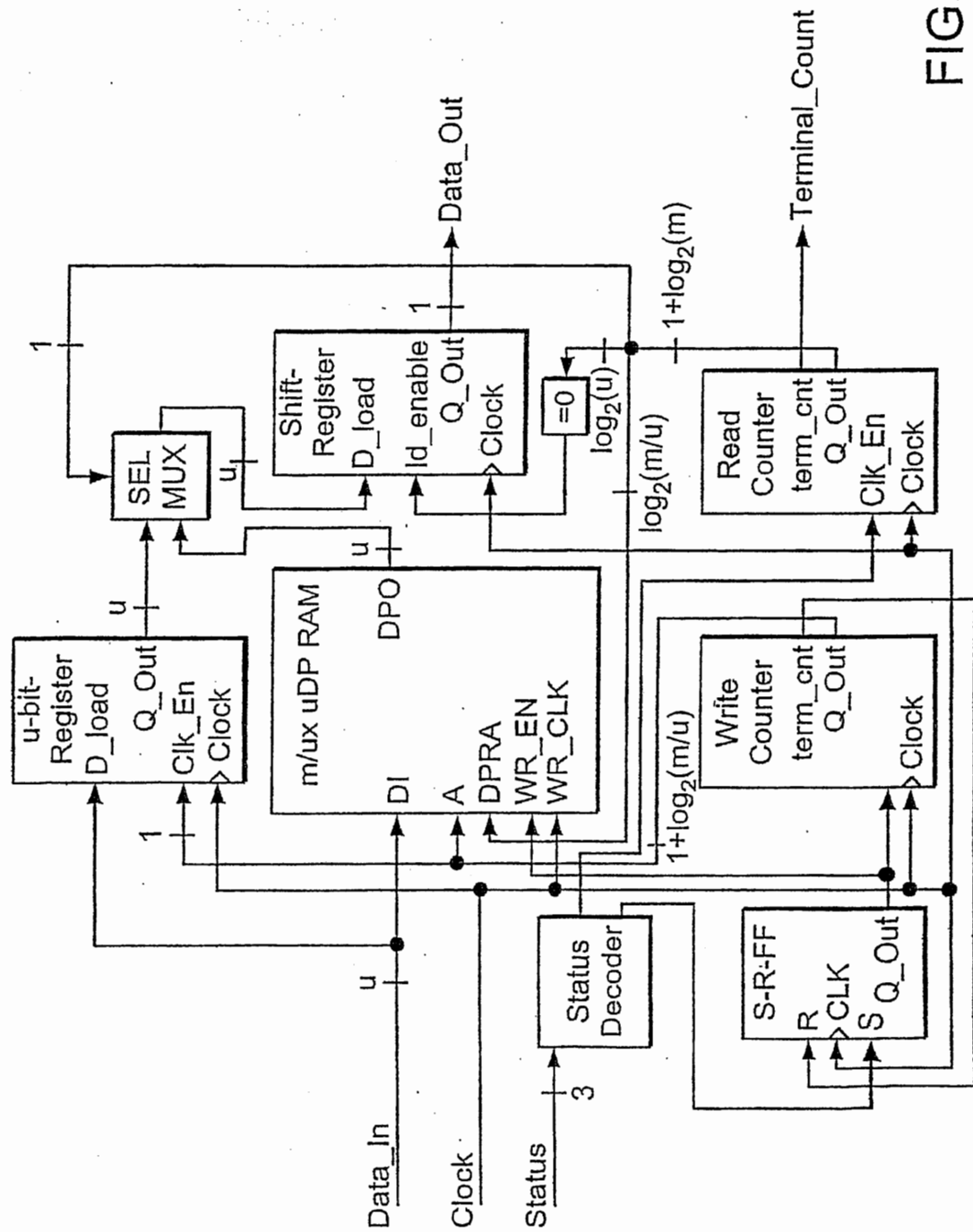


FIG. 11

10/15

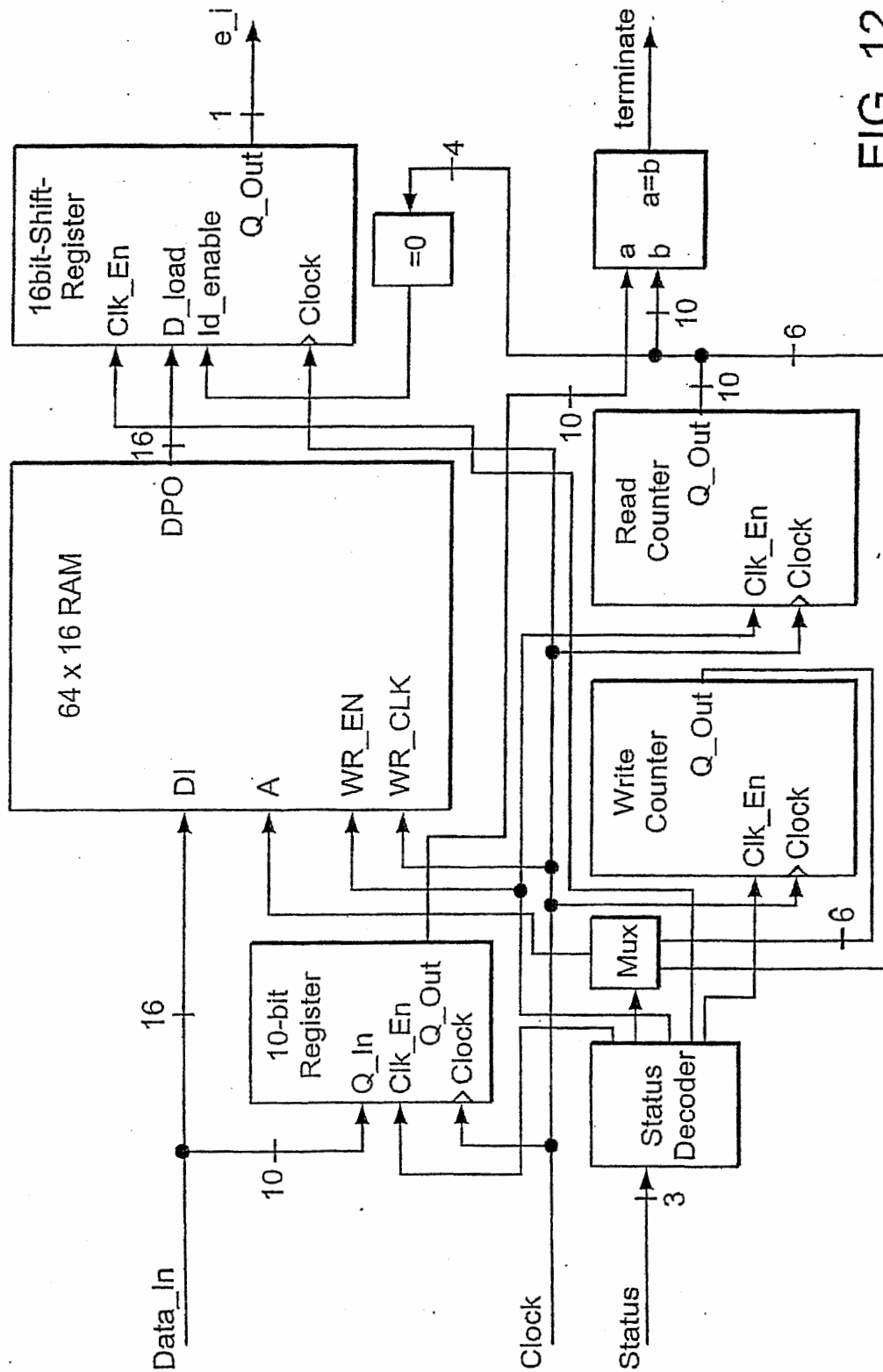


FIG. 12

11/15

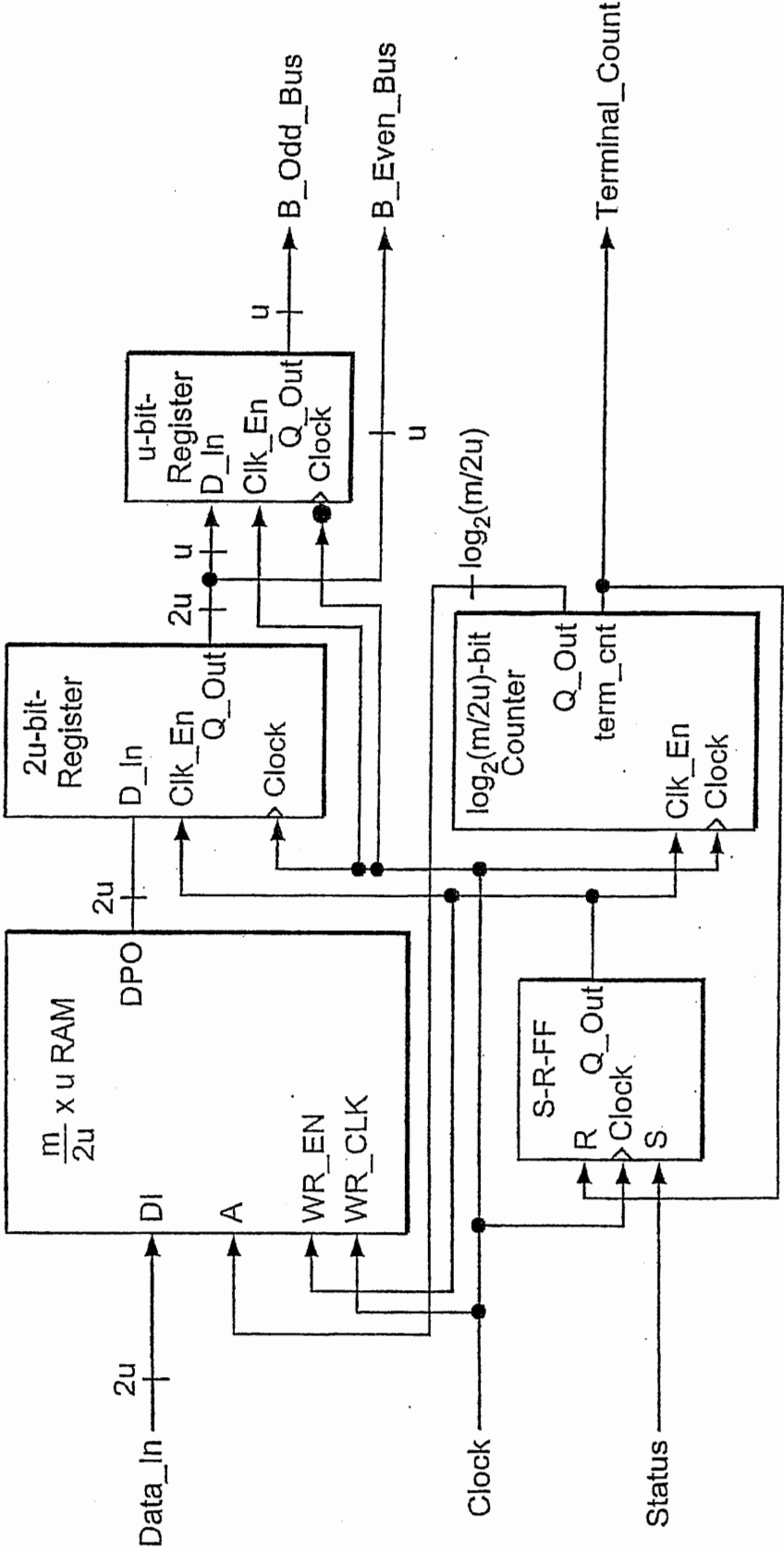


FIG. 13

12/15

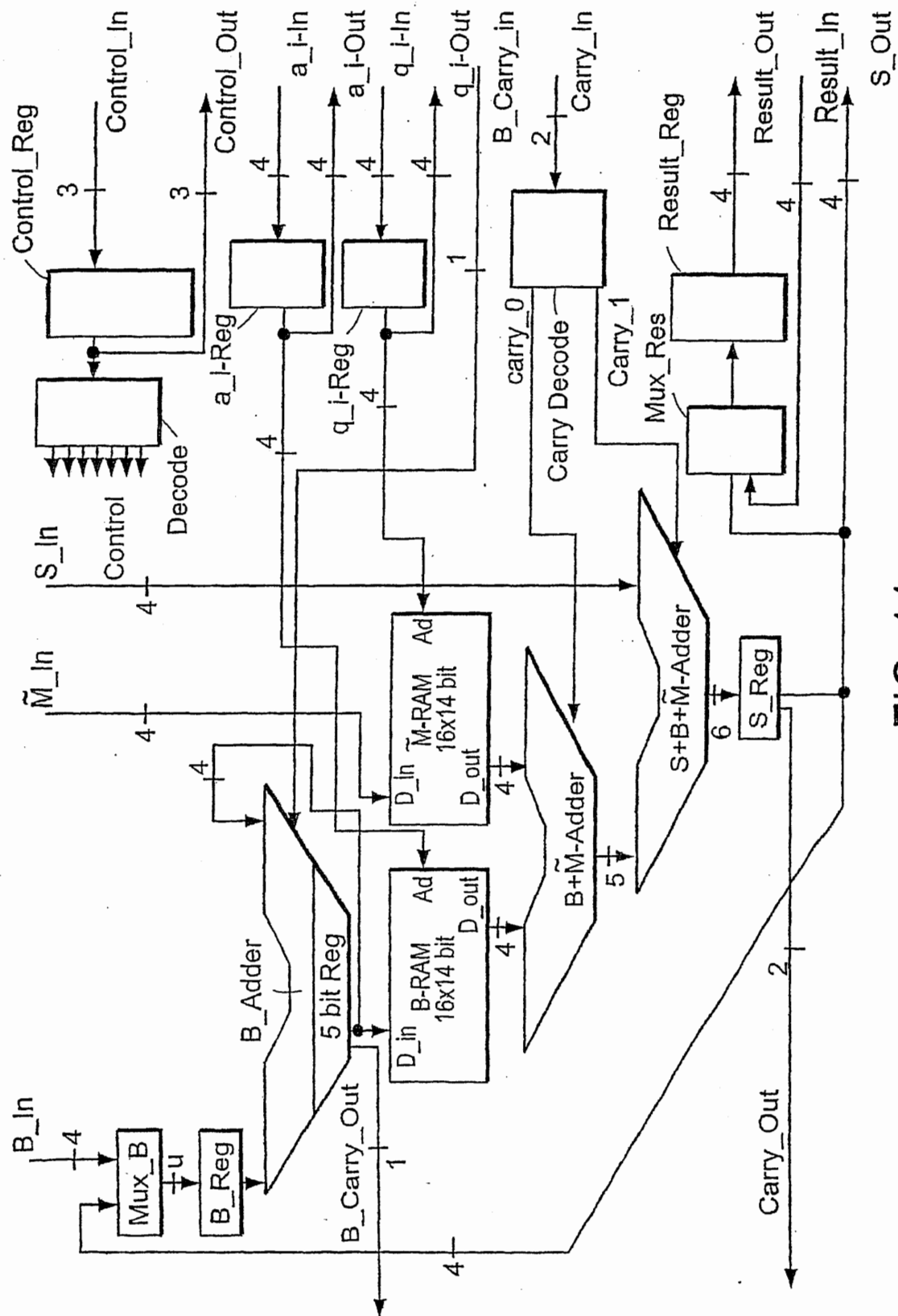


FIG. 14

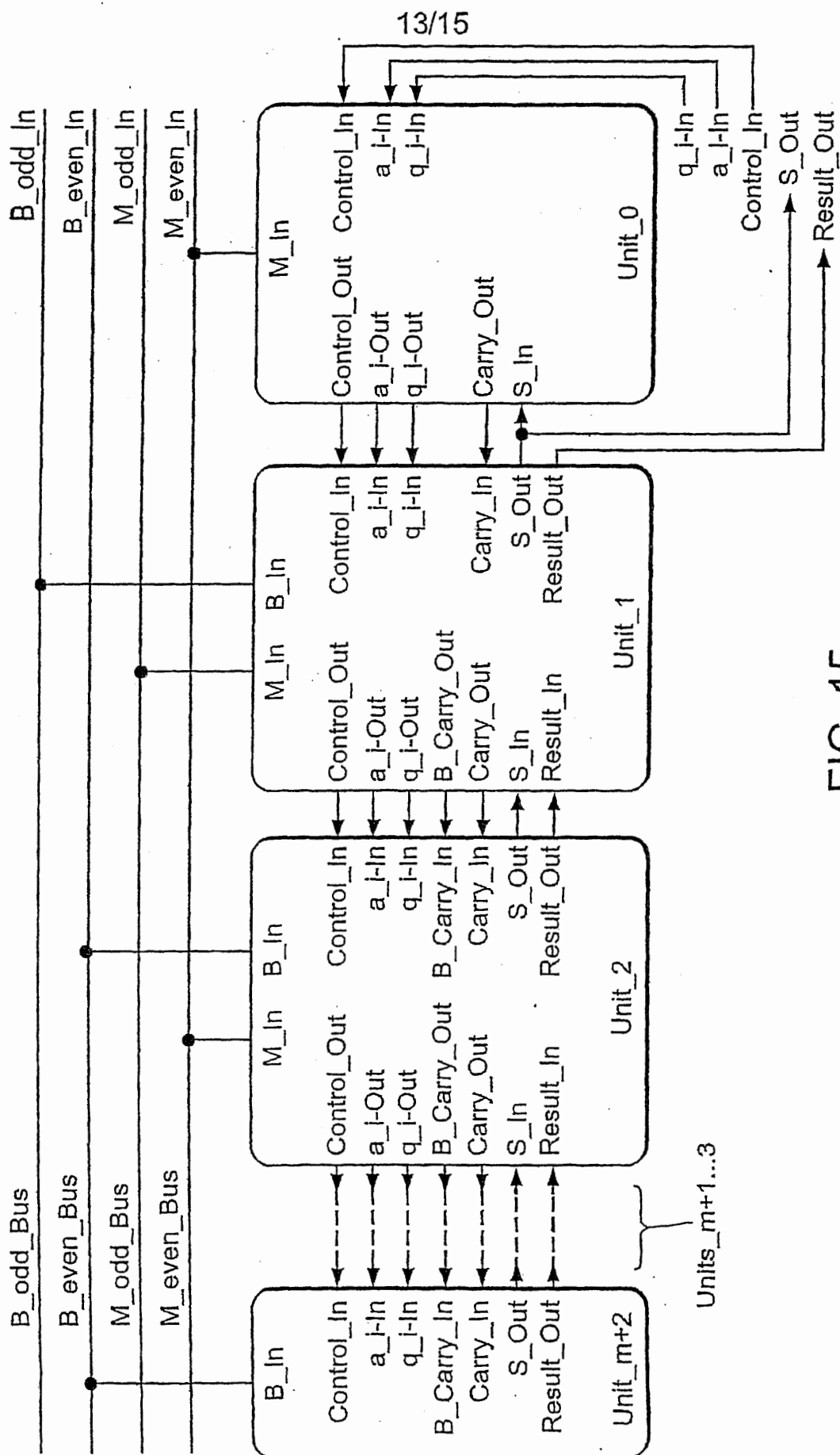


FIG. 15

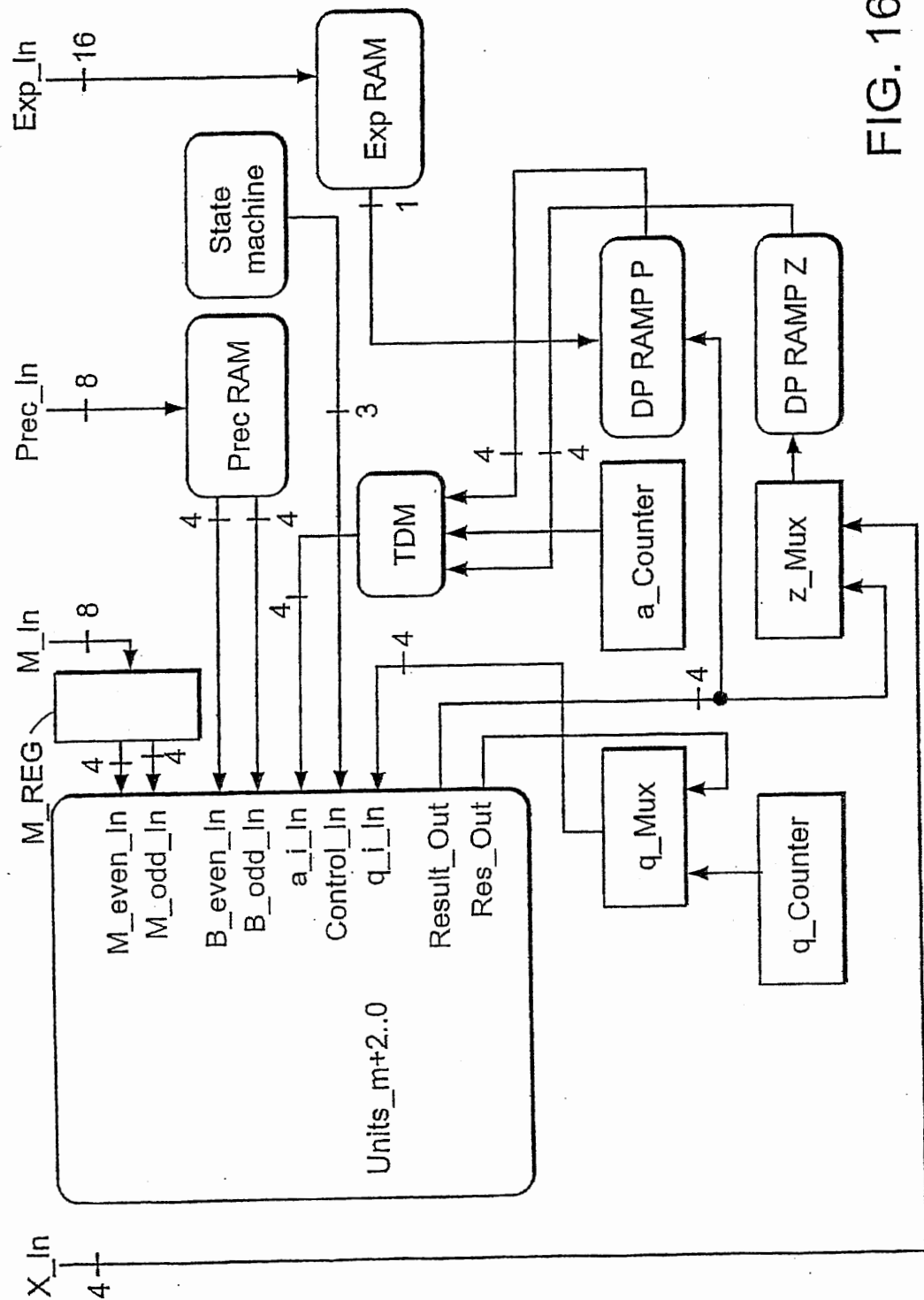


FIG. 16

15/15

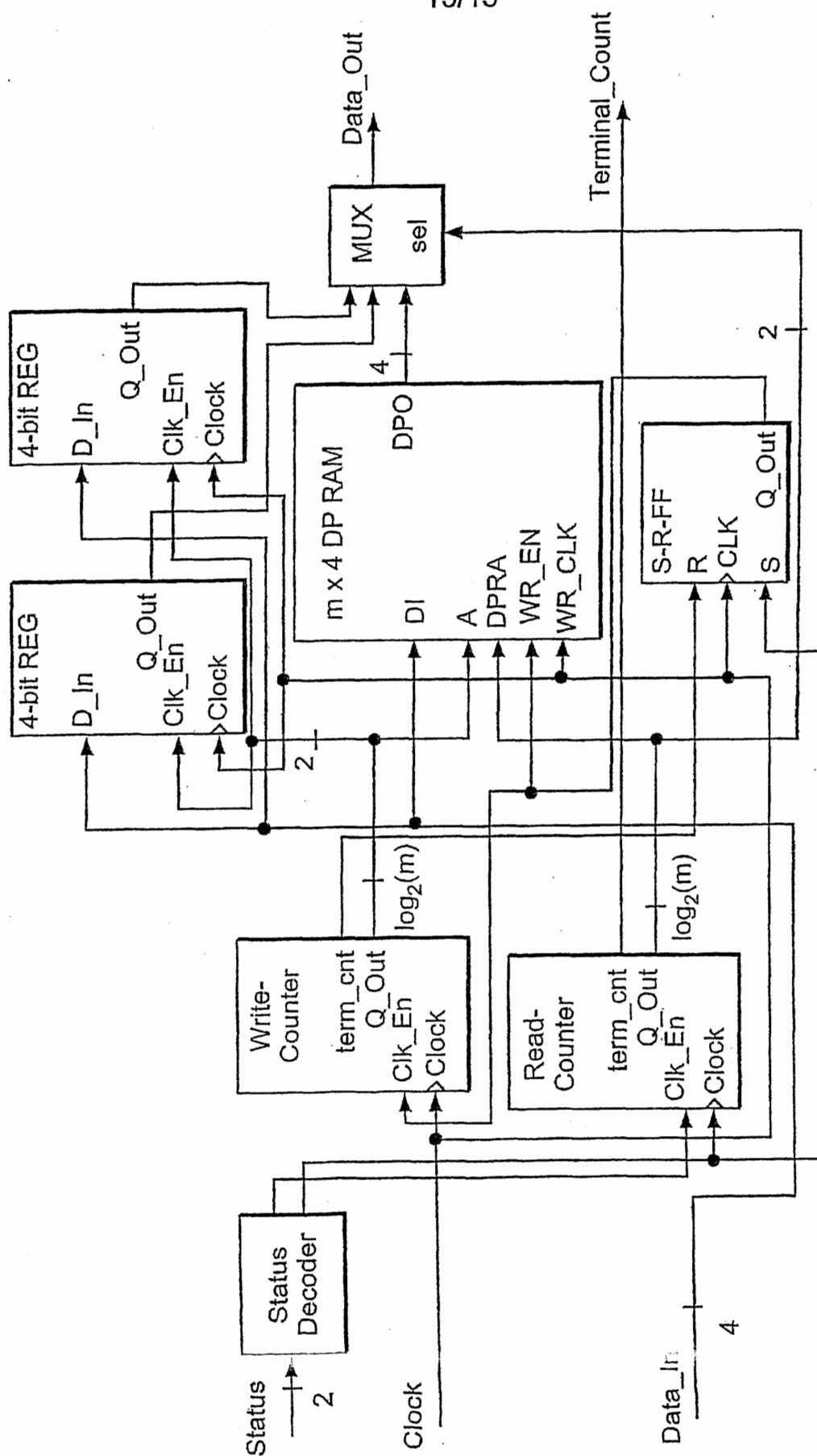


FIG. 17