

This invention relates to an analogue electronic watch having two motors, one for driving the time display, the other for driving means for displaying the day of the month. It relates more particularly to a watch comprising, in addition, a perpetual-calendar circuit. This circuit includes day, month and year counters and issues a date-representing signal to a control circuit which activates the second motor and causes it to move forward by a number of steps such that the display of the day of the month may be made to correspond to the contents of the day counter, and thus agree with the indication shown by a perpetual calendar.

Such watches are known and a form of embodiment thereof is described in US Patent Specification 4300222. The watch described in this specification comprises a perpetual calendar displaying the day of the month and, possibly, the day of the week. Although the calendar is reliable when the watch operates normally, a change of cell causes the counters to be in states that are in no way related to the date since the calendar circuit is no longer able to generate correct signals.

After a change of cell, the counters, the day of the month display and of course the time display of the watch need to be corrected. The operation of correcting the day of the month display is done in the usual way. However, correcting the counters is hardly possible for the user or for a watch-repairer not having the required equipment. Indeed, on the other hand, to diminish the duration of operations, each counter must be corrected separately and this involves complex manipulations. On the other hand, for such correction to be possible, the contents of the counters must be known and this information is not displayed by the watch.

A change of cell can therefore only be performed in the factory or in an after-sales service centre and this places an undesirable

constraint in the use of an otherwise most practical watch.

An object of the invention is to overcome this drawback by providing a watch having a perpetual calendar that only involves, after a change of cell, an easy correction of the day of the month display by the bearer of the watch.

To this end, the watch provided by the invention comprising :

- a time-keeping circuit able to generate a time base signal and a rapid advance signal having a higher frequency than the time base signal;
- a first motor arranged to be activated off the time base signal;
- a daily contact arranged to be activated by the first motor at the end of each day to issue a daily signal;
- analogue time display means arranged to be driven by the first motor;
- a corrector member having an inoperative position and an operative position in which the indications given by said time display means may be modified;
- means coupled with the corrector member and arranged to generate a logic positioning signal, with one level of said signal being representative of the inoperative position of said member and the other level being representative of the operative position of said member;
- a perpetual calendar circuit including day, month and year counters connected in series and activatable by the daily signal, and means responsive to the state of the month and year counters to put the day counter, at the end of 31-day months, in a state corresponding to the first day of the following month, in which state the day counter is arranged to generate a monthly signal;
- a second motor;
- analogue day of the month display means arranged to be

driven by the second motor;

- means activatable by the second motor to generate a day of the month signal whenever the day of the month is the first day of a month;

- a circuit for controlling the second motor and arranged to issue to the latter, in response to the daily signal, to the monthly signal, to the day of the month signal and to the rapid advance signal, a control signal to enable the second motor to alter, at the frequency of the rapid advance signal, the day of the month display by a number of days such as to make up to 32 the state of the day counter; and

- a cell for energizing the electronic circuitry;

is characterized in that it further comprises :

- a reprogrammable non-volatile memory;

- a first transmission circuit coupled to the month and year counters to transfer into the non-volatile memory the contents of said counters at the end of each month and of each year respectively;

- a detection circuit arranged to generate a detection signal upon replacement, on a replacement date, of the cell that caused the watch to stop on a stoppage date;

- a second transmission circuit for transferring, in response to the detection signal, the contents of the non-volatile memory into the month and year counters; and

- an initialization circuit arranged to receive the detection signal, the day of the month signal, the positioning signal, the rapid advance signal and the signal that is representative of the contents of the day counter and to issue, in response to the positioning signal generated by the motion of the corrector member from its operative to its inoperative positions after setting the date

of the watch , a discrimination signal to the month counter such as to increment the latter by one unit when the day of the month on which the cell is replaced is less than the day of the month on which the watch stopped whereby the month counter may indicate the correct month should the cell be replaced within twenty-seven, twenty-eight,

twenty-nine or thirty days reckoned from the date of stoppage of the watch.

One advantage of the invention is that, after a change of cell, inasmuch as it is performed within one month from the date of stoppage of the watch, It is sufficient to so that the perpetual calendar circuit may be made to operate again correctly

one ordinary calendar-watches.

Another advantage of the invention is that it does not require the contents of the day counter in the non-volatile memory to be memorized, thereby enabling the area of the memory to be reduced, its consumption to be decreased and its life to be increased.

Other properties and advantages of the invention will appear from the following description of a non-limiting embodiment of such a time-piece in connection with the accompanying drawings in which Figures 1, 2 and 3 show the block diagrams of a embodiment of the watch provided by the invention, references a, b, c, ..., m indicating cross-over points between conductors extending from one figure to another.

The illustrated watch comprises a time-keeping circuit 1 which supplies a clock signal S1 to a first motor 2 which, via a control mechanism 3, drives a time display 4 having hour, minute and second hands.

Time-keeping circuit 1 includes an oscillator 10 that generates a signal of e.g. 32768 Hz and whose frequency is stabilized by a quartz resonator 11, a two-input AND gate 12 having one input connected to the output of the oscillator, a frequency divider 13 having a first input connected to the output of AND gate 12, a two-input AND gate 104 having one input connected to a first output of divider that issues a 1 Hz signal, and a drive circuit 14 which receives the 1 Hz signal from the output of AND gate 104 and issues signal S1 on its own output.

Frequency divider 13 further has a second output which issues a rapid advance or retrieval signal S13 having a frequency of about 10-Hz, and a reset input R which allows the reset of the final stages of the divider. This input R is connected to the output of an inverter 15 whose input is connected to the second input of AND gate 12.

First motor 2 may for instance be a stepping motor that rotates in one direction only. It drives, in control mechanism 3, a first gear-train, not shown, which causes the hands of display 4 to move forward. This gear-train also actuates a first, daily contact X, causing it to close when the watch moves on to the next day, _____

analogue watch that operates as follows. When crown 16 is in its inner, neutral position, with signal Sy high, AND gate 12 lets the signal from oscillator 10 through to frequency divider 13. The reset input R of divider 13 being low, the circuit issues the 1 Hz signal to the input of drive circuit 14 via AND gate 104 whose other input is assumed to be high for the time being. Circuit 14 in turn issues clock signal S1 to first motor 2. Motor 2 drives, via the first gear-train, the hands of time display 4 and actuates contact X by means of this gear-train. The daily signal Sx generated by contact X switches at midnight from low to

high and returns shortly afterwards to low where it remains until the beginning of the following day.

In the outer, correction position 16' of crown , signal Sy is low, thus blocking AND gate 12 and resetting via inverter 15 frequency divider 13 which, in these conditions, receives no signal. The same applies to motor 2, which remains idle. The hands of display 4 can then only be moved by the crown which, in this position , is connected to the gear-train to enable accurate time-setting of the watch. When the hands, driven by the crown, go through the midnight point, contact X is of course actuated as if the hands were driven by the first motor.

The watch further comprises a perpetual day of the month indicator giving the number of each day of a month. This information is provided by a day of the month display 20 embodied in the usual way by a disc bearing numbers 1 to 31. In the drawing, display 20 is separate from display 4, but in practice the day of the month will appear in an aperture 21 of time display 4.

Display 20 further actuates a day of the month contact Z on the first day of each month, as by means of a cog 22 provided on the disc opposite number 1.

This contact generates a day of the month signal Sz which goes high at the start of the first day of each month and which reverts to low one day later so to remain till the beginning of the next month.

The jump of the display is achieved by a second unidirectional motor 23 which drives disc 20 via a second gear-train 24 . Motor 23 is activated by a control signal S25 generated by a control circuit 25.

Circuit 25 comprises a three-input AND gate 26, a two-input OR gate 27 having one input connected to the output of AND gate 26, and a drive circuit 28 connected to the output of gate 27 and which issues on its output, control signal S25. One input of AND gate 26 receives rapid advance signal S13, a second receives day of the month signal Sz, and a third receives a monthly signal Sm, described later. The second input of OR gate 27 receives daily signal Sx.

The watch further comprises a perpetual calendar

circuit 30 having a five-bit day counter 31 which counts in thirty-ones, a four-bit month counter 32 which counts in twelves, and two-bit year counter 33 which counts in fours. The input of counter 33 is connected to the output of counter 32 and it will be assumed for the time being that the input of counter 32 is directly connected to the output of counter 31. Counter 31 receives on its counting input daily signal Sx and issues on one output, at the beginning of each month, monthly signal Sm to counter 32 which, in turn, issues at the beginning of each year an annual signal Sa to counter 33. Signal Sx is applied to counter 31 via a two-input OR gate 108, one input being connected to contact X and the other being assumed to be low for the time being. Each counter further issues, on another output, a signal indicative of its contents, i. e. S31 for counter 31, S32 for counter 32 and S33 for counter 33. Additionally, counter 32 issues a signal Smc indicative of short months of less than thirty-one days and counter 33 issues a signal Sab indicative of a leap year in a four-year cycle.

Circuit 30 further has a correction circuit 34 which receives signals Smc and Sab. Circuit 34 generates, from signals Smc and Sab, a correction signal S34 for counter 31 to set its contents to 1 when the calendar switches from a short month to the following month. In this way, the contents of counter 31 will always agree with what is shown by a perpetual day of the month indicator.

The switch to 1 of the contents of counter 31 generates signal Sm. It will be assumed that this signal is normally low and goes high at midnight, when the calendar circuit moves from one month to the next, and reverts to low at the latest one day later.

Signals S31, S32 and S33 together make up an eleven bit calendar signal S30 representative of the date in counters 31, 32 and 33. Each of these counters further has an input E for setting them, with a logic signal, to a given day, month and year respectively. This date setting can however only be done at the factory.

Circuit 30 will not be described in detail since such circuits are known and a form of embodiment is described in the US patent

specification referred to earlier.

Monthly signal Sm is applied to the third input of AND gate 26 in control circuit 25 via a two-input OR gate 106, one input receiving signal Sm and the other receiving a logic signal which will be assumed for the time being to be low. Under these conditions circuit 25 operates as follows. Assuming disc 20 and calendar circuit 30 have been set to the correct date, daily signal Sx, which reaches at midnight the input of drive circuit 28 via OR gate 27, causes disc 20 to move forward by one day. This same signal also increments by one unit day counter 31. If the disc and day counter 31 show a day other than the last day of a month, signals Sz and Sm will respectively be high and low. Rapid advance signal S13 will in this case be blocked by AND gate 26 through signal Sm. Disc 20, having rotated through one step, will thus remain in this position until contact X is closed again. But if disc 20 shows the 30th day of a thirty-day month, signal Sx at midnight will cause the disc rotate to 31 and the contents of day counter to switch to 1. Signal Sm then goes high, which is the same logic level as signal Sz since contact Z is closed for this position of the disc. It is assumed that rapid advance signal S13 is made up of pulses and has a frequency of say 8 Hz. This signal can, under these conditions, transit through AND gate 26 and OR gate 27 and reach the input of circuit 28. In response to each pulse of signal S13, circuit 28 generates a signal that causes the disc move forward by one day. In the present case, with the disc indicating 31, a single pulse of signal S13 is sufficient to move the disc to 1 and to bring it into agreement with the contents of counter 31. In this new position of disc 20, contact Z is open and signal Sz is low. This causes signal S13 to be blocked by AND gate 26. The disc will therefore remain in this position until the next daily signal Sx, which will cause disc 20 and the contents of counter 31 to go to 2. In these states of disc 20 and of counter 31, signal Sz is high, contact Z being closed, and signal Sm is low. Signal Sm thus causes signal S13 to be blocked by AND gate 26 until the contents of counter 31 again are 1.

The same thought process would show that at the end of a

twenty-nine day month of February in a leap year, AND gate 26 of control circuit 25 would allow two consecutive pulses of rapid advance signal S13 to go through, causing the disc to rotate rapidly, at the frequency of this signal, from 30 to 1. And at the end of a twenty-eight day month of February, three pulses of the rapid advance signal S13 would cause the disc to rotate from 29 to 1.

Besides the above described function of contact Z, the latter further enables, in the event of a malfunction of the disc, to synchronize the latter with the contents of day counter 31 on the first day of each month. This is due to the fact that, whatever indication is provided by disc 20 when the contents of day counter 31 are 1 and monthly signal Sm is high, AND gate 26 will allow the required number of pulses of rapid advance signal S13 to transit through it in order rapidly to rotate the disc to the first day of the month.

Drive circuit 28 issues on its output control signal S25 whenever a signal issues on the output of OR gate 27. The duration of this latter signal therefore does not affect control signal S25. Thus, if a pulse of rapid advance signal S13 is interrupted and shortened through contact Z being opened, the disc will still rotate normally.

To move disc 20 by one day, control signal S25 may contain only one pulse causing motor 23 to rotate one step. However, to reduce the torque that needs to be supplied by the motor and lower its consumption, it is preferred for the disc to be rotated by driving motor 23 through N steps in response to a control signal S25 made up of a series of N consecutive pulses. The triggering of one pulse of a series automatically generates the other pulses in the series, such that the disc can only move through whole days.

Control circuit 25 can also be designed to generate the control signal S25, that causes the disc to advance by the required number of days at the end of a month of less than thirty-one days, on the basis of the information supplied by signals Smc and Sab, instead of that supplied by signal Sz. An embodiment of such a circuit is described, for example, in the US patent specification mentioned earlier.

Contact Z then serves no purpose. This arrangement however has the drawback of not enabling disc 20 in the case of a malfunction of the latter to be synchronized with the contents of counter 31 on the first day of each month.

The circuits of the described watch are supplied with energy by a cell not shown. After initially time and date setting the watch the latter will carry on showing the correct time so long as the voltage of the cell remains above a critical threshold.

After a while, as the cell runs out, its voltage drops below the critical threshold and the watch will stop on a date D_A . This stoppage entails the loss, and this is important, of the date contained in counters 31, 32 and 33 of calendar circuit 30 since these counters form a memory which is cleared when it no longer receives sufficient energy. Replacement of the used cell by a new cell does not, of course, enable this date to be recovered since the counters are then in random states, or in a state in no way related with the date on which the watch stopped, such date continuing however to appear on disc 20.

When the cell is replaced on a date D_R , the counters thus need to be reprogrammed. This is a complex operation requiring the watch to be sent back to the factory, a major inconvenience.

To avoid this drawback, the watch further comprises a first transmission circuit 40, a reprogrammable non-volatile memory 41 also referred to as EEPROM and which retains its contents even in the absence of a supply voltage, a second transmission circuit 42, a voltage detection circuit 43 and an initialisation circuit 100.

Transmission circuits 40 and 42 can, for instance, be made up of transmission gates which are known electronic components, while non-volatile memory 41, with its interface circuits that enable items of information to be entered and read, can with advantage be of the FAMOS type, also known. The use of such a memory in the watchmaking art is known as for instance in Swiss Patent Specification 534913 which describes a frequency correction logic circuit wherein the content of the non-volatile memory governs the operation of a watch. It should

however be noted that the area occupied by a non-volatile memory with its interface elements in a horological circuit is quite substantial, that its energy consumption when entering and reading data is not negligible and, above all, that the duration of memorization decreases rapidly with the number of entries and readings made.

The purpose of the non-volatile memory is to safeguard the contents of the counters in calendar circuit 30 when a cell runs out. The best way would be to transfer to this memory the content of day counter 31 at the end of each day, the content of month counter 32 at the end of each month and the content of year counter 33 at the end of each year. However, the part of the non-volatile memory that is connected to the day counter would then have to work at too high a frequency for the watch to have a sufficiently long life.

To overcome this difficulty, only the contents of the month and year counters are periodically transferred into the non-volatile memory in the present embodiment, this has the added advantage of reducing the capacity of the memory from 11 bits to 6 bits and hence of reducing its area by nearly half.

The purpose of first transmission circuit 40 is to transfer the contents of the counters 32 and 33 from calendar circuit 30 to non-volatile memory 41 in response to a transfer signal. To this end, circuit 40 comprises a first series 45 of four transmission gates. These gates are connected, firstly, to the output of counter 32 so as to receive the four-bit signal S32 and, secondly, to the input of a first, four-bit section 48 of memory 41. These gates are controlled by the transfer signal which in this case is monthly signal Sm.

Thus, at the end of each month when the content of counter 32 changes, the new value of counter 32 is transferred to section 48 of memory 41, in which it remains memorized irrespective of the voltage of the cell.

Second transmission circuit 42 has the same structure as circuit 40. It thus also has a first series 51 of four transmission gates. These gates are connected, firstly, to the output of section 48 of

memory 41 so as to receive signal S32 and, secondly, to the input E of counter 32.

When changing the cell on date D_R , circuit 43, which is a monostable flip-flop of a known type, generates a detection signal S43 which indicates that the voltage across the terminals of the circuits is again at least equal to the critical threshold. This signal is taken as the transfer signal for second transmission circuit 42. Thus, at that instant, when the state of counter 32 is indefinite, counter 32 receives on its input E the signal S32 that existed at the time the watch stopped on date D_A .

Circuit 40 further comprises a second series 46 of two transmission gates for transferring, at the end of each year in response to signal Sa, the content of counter 33 to a second, two-bit section 49 of memory 41. Circuit 42 also comprises a second series 52 of two transmission gates which are connected, firstly, to the output of section 49 and, secondly, to input E of counter 33, signal S43 being taken as the transfer signal for these gates as with the gates of series 51.

Thus, just after changing the cell on date D_R , month counter 32 and year counter 33 are reset, by signal S43 and with the aid of circuit 42, in the state they were in when the watch stopped on date D_A , whereas the state of day counter 31 becomes indefinite. Disc 20 remains of course in the position it was in on date D_A .

In order for the watch's calendar again to display the correct date after a change of cell, month counter 31 must first be put into agreement with day of the month display disc 20, whereupon counter 31 and disc 20 are set manually to the day of the month of date D_R .

Counter 31 and disc 20 are brought into agreement with one another automatically with the aid of initialisation circuit 100 after the change of cell. This circuit also ascertains whether the new cell was put in during the same month the watch stopped or the month after and, in the latter event, it increments counter 32 by one unit so that its content should reflect the correct month.

In bringing day counter 31 into agreement with disc 20, initialisation circuit 100 plays a part similar to that of a hypothetical, additional, five-bit section for non-volatile memory 41, which, by means of transmission gates, would memorize the content of counter 31 when the watch stops and would transfer this information to this counter after the change of cell. Circuit 100, which is made up of conventional logic circuits, has however the advantage over a five-bit non-volatile memory of taking up less room, of needing less energy and of having no life limitation.

Whether the watch comprises a non-volatile memory that safeguards the content of the day counter or an initialisation circuit, the operation of manually date setting the watch is similar in both cases. This operation consists in rotating the hour hand with the crown in correction position 16' as many times 24 hours as is needed for the numerical indication of the day of the month to tally with date D_R . As such a date setting operation can be rather time consuming, a faster way will be described later. The watch must then, of course, be time set in the usual way.

Initialisation circuit 100, which will now be described, only becomes operative in the watch when changing a cell; the rest of the time it is in a wait condition. This circuit comprises a two-input AND gate 105, a two-input OR gate 118, a sequential circuit 119 that generates logic control signals and a discrimination circuit 120 that produces a discrimination signal S_{120} when the cell is changed during the month after the watch has stopped.

One input of AND gate 105 is connected to the output of day counter 31 so as to receive monthly signal S_m . The output of gate 105 is connected to one input of OR gate 118 whose output is connected to the counting input of month counter 32. The other input of AND gate 105 receives logic signal $\bar{S}_{102}$ from circuit 119 and the other input of OR gate 118 receives a discrimination signal S_{120} from circuit 120. Signal $\bar{S}_{102}$ is also applied to the other input of AND gate 104. When the watch is working normally, signal $\bar{S}_{102}$ is high and signal S_{120} is

low. This being so, signal S_m is able to proceed through gates 105 and 118 from the output of counter 31 to the input of counter 32 and the output signal of divider 13 is able to proceed to the input of drive circuit 14 through gate 104, as was assumed earlier.

Sequential circuit 119 contains a bistable flip-flop RS 101, whose set input S is connected to the output of circuit 43 so as to receive detection signal S_{43} and whose reset input R is connected to contact Z via an inverter 110 so as to receive a signal $\bar{S}_z$ that is the inverse of day of the month signal S_z . The output Q of flip-flop 101 issues a signal S_{101} which is applied to one input of a two-input AND gate 107, the other input of this gate receiving rapid advance signal S_{13} . The output of AND gate 107 issues a signal S_{107} which is applied to the other input of OR gate 108 whose output, which issues a signal S_{108} , is connected to the input of counter 31. Signal S_{101} is also applied to the other input of OR gate 106 and to the input of a monostable flip-flop 111 that is responsive to a dropping edge of this signal. The output of circuit 111 is connected to one input of two-input OR gate 103 through a delay circuit that is here made up of a pair of series-connected inverters 112a and 112b. The other input of OR gate 103 receives detection signal S_{43} . The output of gate 103 issues a signal S_{103} which is applied to an input of day counter 31 that enables the content of this counter to be set to 1.

Circuit 119 further comprises a second bistable RS flip-flop 102 whose input S is connected to the output of circuit 43 and whose input R is connected to the output of a monostable flip-flop 114. Positioning signal S_y is applied to the input of flip-flop 114 which is responsive to a rising edge of the signal. A two-input AND gate 116, with one input connected to the direct output Q of flip-flop 102 and the other input connected to the output of flip-flop 114, issues on its output a signal S_{116} . And inverse output $\bar{Q}$ of flip-flop 102 issues signal $\bar{S}_{102}$ referred to earlier.

Discrimination circuit 120 contains a memory register 109 which receives signal S_{31} on one input and signal S_{101} on a clock input Ck.

When signal S101 switches from high to low, the register memorises the number that is representative of the content of counter 31 at that time. The output of register 109 is connected to the input of a subtractor 113 which generates a signal S113 that is representative of the difference between number 33 and the number memorised by the register. Signal S113 is applied to one input, A, of a two-input comparator 115, the other input, B, receiving signal S31. The comparator generates a signal S115 which is low when the number corresponding to signal S113 is less than or equal to the number that corresponds to signal S31, and which is high otherwise.

Circuit 120 further comprises a two-input AND gate 117 which receives signals S115 and S116 and applies discrimination signal S120 to one input of OR gate 118.

After the watch stops working on date D_A , disc 20 carries on displaying the day of the month of that date and non-volatile memory 41 continues to contain the month and year data. The content of day counter 31 is however definitely lost.

The primary purpose of initialisation circuit 120 is to bring counter 31 into agreement again with disc 20 after the change of cell on date D_R . This circuit operates as follows:

Immediately after fitting in the new cell, with the crown in its inner, neutral position, circuit 43 generates detection pulse S43 which contains a short pulse. This signal, on activating transmission circuit 42, transfers the month and year data from the non-volatile memory 41 to month counter 32 and year counter 33 which are thus thus reset in the state they were in on date D_A . Signal S43, on passing through OR gate 103, also sets day counter to 1 a first time. Signal S43 also sets flip-flops 101 and 102, a state in which their Q outputs are high.

The high logic level of signal S101, resulting of setting flip-flop 101, is also to be found at the output of OR gate 106 and opens AND gate 26 to signal S13 provided signal Sz is also high, such being the case when disc 20 is not displaying the first day of a month. This state of signal S101 also opens AND gate 107 to signal S13 and register 109 to signal S31.

But signal $\bar{S}102$ is low thereby blocking time base signal S1 by closing AND gate 104 to the output signal of divider 13, and preventing signal Sm from reaching the input of counter 32 by blocking AND gate 105.

Under these conditions, motor 2 and counter 32 do not receive any signal whereas signal S13, on passing through AND gate 26 and OR gate 27, activates motor 23 to rotate disc 20 through N steps, from the position that corresponds to stoppage date D_A to position 1 in which contact Z, on opening, causes signal Sz to switch from high to low. Signal S13 also goes through AND gate 107 and OR gate 108 to increment counter 31 whose content increases from 1 to $1+N$. This latter value is introduced into register 109 since its Ck input is high. Had signal Sz initially been low, with disc 20 displaying 1 on date D_A , this would simply have amounted to the case $N=0$.

With signal Sz going low on opening contact Z, signal S13 is prevented from going through AND gate 26 and disc 20 is blocked in the 1 position. Signal Sz, on going through inverter 110, also resets flip-flop 101, thereby causing signal S101 to switch from high to low. This transition of signal S101 causes signal S13 to be blocked by AND gate 107, value $1+N$ to be memorised in register 109, whose Ck input goes low, and a signal containing a short pulse, to be generated by monostable flip-flop 111. The signal generated by flip-flop 111, on passing through OR gate 103, sets day counter 31 to 1 a second time so as to agree with disc 20. This signal is however sufficiently delayed by inverters 112a and 112b for the setting to 1 of counter 31 to occur after its content $1+N$ has been memorised in register 109. The quantity $1+N$ is transferred to the input of subtractor 113 which calculates the number $32-N$ that corresponds to the day of the month of stoppage date D_A . The signal S113 that is generated by subtractor 113 and which is representative of the day of the month thus calculated is applied to input A of comparator 115.

After the change of cell, the crown must be moved from its neutral position 16 to its correction position 16'. This operation causes contact Y to open and signal Sy to switch from high to low. This in turn

causes AND gate 12 to be blocked to the signal that issues from oscillator 10 and the resetting of the final stages of frequency divider 13.

The crown being now in correction position 16', the watch must then be set to date D_R . This is done by turning the crown thereby to actuate contact X which generates signal S_x , a signal that is made up of a succession of pulses. Each pulse, on passing through OR gate 27, causes disc 20 to move forward one day and, on passing through OR gate 108, increments day counter 31 by one unit. Disc 20 and counter 31 thus remain in agreement. Contact X must be actuated as many times as is needed to rotate disc 20 from position 1 to the position that corresponds to the day of the month in date D_R . The content of counter 31 then also corresponds to this day of the month and this information is conveyed by signal S_{31} to input B of comparator 115.

It will be assumed hereinafter that the cell was changed at latest during the month that follows the month in which the watch stopped, on a day having a lesser number than that of the stoppage day. This means that the cell must be changed within a time interval of 27, 28, 29 or 30 days reckoned from the stoppage day, the actual length of the interval depending on the number of days in the month of date D_A . Thus, if the number of the day of the month of date D_A is less than or equal to the day of the month of date D_R , this means that the cell was changed in the same month as the watch's stoppage month and that signal S_{115} at the output of comparator 115 is low. But if the day of the month of date D_A is greater than that of date D_R , this means that the cell was changed during the month that followed the stoppage month, with signal S_{115} being high.

The watch is then time set in the usual way. This in no way affects disc 20 or counter 31.

The watch being now both time and date set, the crown may be moved from its correction position 16' to its neutral position 16.

This operation closes contact Y and hence causes signal S_y to switch from low to high. With signal S_y now high OR gate 12 is opened to the signal issued by oscillator 10 and monostable flip-flop 114 is

activated which monostable flip-flop in producing a pulse on the R input of flip-flop 102 resets the latter. A short pulse is produced at the input of AND gate 116 while the R input of flip-flop 102 is high and its Q output is not yet low. This pulse goes through AND gate 117, to increment counter 32 by one unit and set it to the correct month, only when signal S115 is high, i.e. when the cell was changed during the month that followed the stoppage of the watch. Resetting flip-flop 102 also causes signal $\bar{S}102$ to switch from low to high. This firstly causes AND gate 104 to open to the signal issuing from frequency divider 13 thereby enabling time-keeping circuit 1 to generate time-base signal S1, and secondly causes AND gate 105 to open to monthly signal Sm issuing from counter 31.

Moving the crown back to its neutral position 16, thereby restoring time-base signal S1, enables the watch to be started again and calendar circuit 30 to work normally again since counter 32 is again receiving monthly signal Sm.

The watch described above may usefully further comprise a known time-zoning device involving magnetic positioning. Crown 16 must then be able to move into a second correction position, not shown, in which it can act on part of the first gear-train to move, by an integral number of hours, only the hour hand and to activate contact X, each time the hour hand moves past midnight. Disc 20 moves forward by one whole day and counter 31 is incremented by one unit. In the second correction position of the crown contact Y remains closed to enable the watch to carry on working normally.

The time-zoning device, besides the function for which it is designed, further enables, after a change of cell, to date set the watch much more quickly than with conventional time setting. If the watch is provided with a time-zoning device that enables the hour hand to be rotated in both directions, the second motor 23 should also be able to rotate in both directions, i.e. be bidirectional. Control mechanism 3 should then have means, not shown but known, e.g. contacts, that are associated with a circuit and which apply a logic signal that discrimi-

nates between the directions of rotation of the crown to an input not shown of circuit 28, and to an input not shown of counters 31, 32 and 33. One logic level of this signal would correspond to forward rotation of the motor, causing the disc to advance, and to incrementation of the counters, whereas the other logic level would correspond to backward rotation of the motor and to decrementation of the counters. The day of the month displayed by disc 20 would, under the above conditions, always agree with the contents of counter 31, whatever the direction of rotation of the hour hand at the time contact X is actuated, in response to rotation of crown 16 while in a correction position.

With bidirectional motor 23 it is best to use an initialisation circuit that enables the watch, after a change of cell, to be date set in the most direct way, i. e. by rotating crown 16 in the direction that involves the least number of jumps for the disc.

The watch could also be time set electronically, instead of mechanically, by signals generated by a time setting circuit, not shown but known, that activates first motor 2 in response to rotation of crown 16. To facilitate this operation, motor 2 should also be bidirectional.

Of course, the watch that has been described can be further modified and have different embodiments obvious to those skilled in the art without departing from the scope of the present invention.



CLAIMS

1. Electronic watch which comprises :

- a time-keeping circuit (1) for generating a time base signal (S1) and a rapid advance signal (S13) having a frequency greater than that of the time base signal (S1);
- a first motor (2) activatable off the time base signal (S1);
- a daily contact (X) activatable by the first motor (2) at the end of each day to generate a daily signal (Sx);
- analogue time display means (4) arranged to be driven by the first motor (2);
- a corrector member (3) having an inoperative position (16) and an operative position (16') in which the indications given by said time display means (4) may be modified;
- means (Y) coupled with said corrector member (3) and arranged to generate a logic positioning signal (Sy), with one level of said signal being representative of the inoperative position (16) of said member (3) and the other level of said signal being representative of the operative position (16') of said member;
- a perpetual calendar circuit including day, month and year counters (31, 32, 33) connected in series and activatable by the daily signal (Sx), and means (34) responsive to the state of the month and year counters (32, 33) to put the day counter (31), at the end of months comprising less than 31 days, in the state corresponding to the first day of the following month, in which state the day counter (31) is arranged to generate a monthly signal (Sm);
- a second motor (23);
- analogue day of the month display means (20) arranged to be driven by the second motor (23);
- means (Z) activatable by the second motor (23) to generate a day of the month signal (Sz) whenever the day of the month is the first day of a month;
- a circuit (25) for controlling the second motor (23) and arranged to issue to the latter, in response to the daily signal (Sx), to the monthly signal (Sm), to the day of the month signal (Sz) and to the rapid advance signal (S13), a control signal (S25) to enable the second motor to alter, at the frequency of the rapid



advance signal (S13), the day of the month display by a number of days such as to make up to 32 the state of the day counter (31); and

- a cell for energizing the electronic circuitry; characterized in that it further comprises :

- a reprogrammable non-volatile memory (41);
- a first transmission circuit (40) coupled to the month and year counters (32, 33) to transfer into the non-volatile memory (41) the contents of said counters (32, 33) at the end of each month and of each year respectively;
- a detection circuit (43) arranged to generate a detection signal (S43) upon replacement, on a replacement date (D_R), of the cell that caused the watch to stop on a stoppage date (D_A);
- a second transmission circuit (42) for transferring, in response to the detection signal (S43), the contents of the non-volatile memory (41) into the month and year counters (32, 33); and
- an initialization circuit (100) arranged to receive the detection signal (S43), the day of the month signal (Sz), the positioning signal (Sy), the rapid advance signal (S13) and the signal representative of the contents of the day counter (31), and arranged to issue, in response to the positioning signal (Sy) generated by the motion of the corrector member (3) from its operative position (16') to its inoperative position (16) after setting the date of the watch, a discrimination signal (S120) to the month counter (32) such as to increment the latter (32) by one unit when the day of the month (D_R) on which the cell is replaced is less than the day of the month (D_A) on which the watch stopped whereby the month counter (32) may indicate the correct month should the cell be replaced within twenty-seven, twenty-eight, twenty-nine or thirty days reckoned from the date of stoppage of the month.

2. Watch according to claim 1, characterized in that the initialization circuit comprises :

- a sequential circuit (119) arranged to receive the detection signal, the date of the month signal, the positioning signal and the rapid advance signal and to generate control signals (S101, S103, S107, S116); and



- a discrimination circuit (120) connected to the sequential circuit and to the day counter and arranged to issue said discrimination signal to the month counter.

3. Watch according to claim 2, characterized in that the discrimination circuit comprises :

- a register (109) connected to the day counter and able to memorize a number representative of the day of the month on which the watch stopped in response to a control signal (S101) from the sequential circuit triggered by the day of the month signal;

- a subtractor (113) connected to the output of the register and arranged to work out the day of the month on which the watch stopped;

- a comparator (115) connected firstly to the subtractor and secondly to the day counter and arranged to generate, after setting the date of the watch to correspond to the cell replacement date, a logic signal (S115) having one logic state when the day of the month in the cell replacement date has a lower number than the day of the month of the watch stoppage date, and another logic state when the day of the month in the cell replacement date has a higher number or a number that is equal to the day of the month in the watch stoppage date; and

- means (117) arranged to receive a control signal (S116) from the sequential circuit and the signal from the comparator and to issue said discrimination signal to the month counter.