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(21) International Application Number: PCT/US98/24630 (22) International Filing Date: 20 November 1998 (20.11.98) (30) Priority Data: 08/977,779 25 November 1997 (25.11.97) US (71) Applicant: ATMEL CORPORATION [US/US]; 2325 Orchard Parkway, San Jose, CA 95131 (US). (72) Inventors: PATHAK, Jagdish; 12998 Robleda Road, Los Altos Hills, CA 94022 (US); PATHAK, Saroj; 12998 Robleda Road, Los Altos Hills, CA 94022 (US); ROSENDALE, Glen, A.; 680 Forest Avenue, Santa Clara, CA 94301 (US). PAYNE, James, E.; 214 Crows Nest Drive, Boulder Creek, CA 95005 (US); HANGZO, Nianglamching; 1079 Gruwell Place, San Jose, CA 95129 (US). (74) Agent: SCHNECK, Thomas; Law Offices of Thomas Schneck, P.O. Box 2-E, San Jose, CA 95109-0005 (US).		(81) Designated States: CA, CN, JP, KP, KR, NO, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report. With amended claims and statement.
(54) Title: ZERO POWER POWER-ON-RESET CIRCUIT (57) Abstract A power-on-reset circuit includes a first charging stage (162) for building up a charge during power up. The rising voltage of the first charging stage is sensed and used to control means (122) for charging up a second charging stage (164). When the second charging stage reaches a first voltage level, a circuit (130) is tripped to pull the potential of the first to ground. The grounding of the first charging stage (162) is fed back to the charging means (122) which shuts off its power burning components and maintains the first voltage level at the second charging stage (164).		