CLAIMS

1. A method, comprising:

during a first time period, transferring first charge carriers from a first charge storage region to a second charge storage region; and

during a second time period:

receiving second charge carriers at the first charge storage region; and

reading out the first charge carriers from the second charge storage region.

2. The method of claim 1, wherein:

the first and second charge carriers are generated in a photodetection region in response to arrival of incident photons at the photodetection region;

before the first time period, the first charge carriers are received at the first charge storage region from the photodetection region; and

during the second time period, the second charge carriers are received at the first charge storage region from the photodetection region.

3. The method of claim 2, wherein:

over multiple sub-periods within the second time period, the second charge carriers are received at the first charge storage region; and

each sub-period within the second time period follows a respective excitation of a sample that causes the sample to emit the incident photons.

4. The method of claim 2 or 3, wherein:

the second charge carriers are received at the first charge storage region from the photodetection region via a first charge transfer channel that connects the photodetection region to the first charge storage region; and

the first charge carriers are transferred from the first charge storage region to the second charge storage region via a second charge transfer channel that connects the first charge storage region to the second charge storage region.

5. The method of any one of claims 1-4, wherein reading out comprises transferring the first charge carriers from the second charge storage region to a readout region to be sampled.

6. An integrated circuit controllable to perform the method of any one of claims 1-5, the integrated circuit comprising:

a photodetection region configured to generate charge carriers in response to receiving incident photons;

a first charge storage region electrically coupled to the photodetection region to receive charge carriers; and

a second charge storage region electrically coupled to the first charge storage region to receive charge carriers.

7. The integrated circuit of claim 6, wherein the integrated circuit is controllable to induce a potential barrier between the first and second charge storage regions while the first charge storage region receives charge carriers from the photodetection region and the second charge storage region reads out charge carriers.

8. The integrated circuit of claim 7, further comprising a first transfer gate positioned, at least in part, between the first and second charge storage region and configured to receive a first control signal that causes the first transfer gate to control the potential barrier between the first and second charge storage regions while the first charge storage region receives charge carriers from the photodetection region and the second charge storage region reads out charge carriers.

9. The integrated circuit of claim 8, further comprising:

a first charge transfer channel connecting the first charge storage region to the second charge storage region and configured to be biased by the first transfer gate to control the potential barrier between the first and second charge storage regions.

10. The integrated circuit of claim 9, further comprising:

a drain region electrically coupled to the photodetection region to receive charge carriers from the photodetection region;

a second transfer gate positioned, at least in part, between the photodetection region and the first charge storage region and configured to receive a second control signal that causes the second transfer gate to control a potential barrier between the photodetection region and the first charge storage region while the drain region receives charge carriers from the photodetection region; and

a second charge transfer channel connecting the photodetection region to the first charge storage region and configured to be biased by the second transfer gate to control the potential barrier between the photodetection region and the first charge storage region.

11. The integrated circuit of any one of claims 6-10, wherein the photodetection region and the first and second charge storage regions are configured to induce an intrinsic electrical field in a first direction from the photodetection region to the first charge storage region and from the first charge storage region to the second charge storage region.

12. The integrated circuit of claim 11, wherein:

the photodetection region has a first intrinsic electric potential level; and

the first charge storage region has a second intrinsic electric potential level that is different from the first intrinsic electric potential level.

13. The integrated circuit of claim 11, wherein:

the photodetection has a first pinning voltage;

the first charge storage region has a second pinning voltage that is different from the first pinning voltage; and

the second charge storage region has a third pinning voltage that is different from the first and second pinning voltages.

14. The integrated circuit of claim 11, wherein:

the photodetection region has a first dopant concentration of a first conductivity type;

the first charge storage region has a second dopant concentration of the first conductivity type that is higher than the first dopant concentration; and

the second charge storage region has a third dopant concentration of the first conductivity type that is higher than the second dopant concentration.

15. A system, comprising:

the integrated circuit of any one of claims 6-14; and

a control circuit configured to control the integrated circuit to perform the method of any one of claims 1-5.