A METAL GATE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD

BACKGROUND

[0001] This disclosure relates generally to semiconductor manufacturing, and more particularly to a method for manufacturing a metal gate.

[0002] A gate dielectric integrity of metal-oxide-semiconductor field effect transistor (MOSFET) is associated with reliability and lifetime of MOSFET devices. As the gate dielectric thickness is reduced in technology scaling-down, gate leakage is induced, increasing power consumption and reducing device performance.

[0003] High K materials, which include materials with K values larger than approximately 5, such as SiON, HfO_xSi_y, or HfO_2, are implemented to realize thicker gate dielectric layers for minimized leakage current and equivalent oxide thickness (EOT). Also, a metal gate electrode can be used to reduce gate resistance. In addition, the metal gate can also reduce gate leakage that is induced by boron penetration from polysilicon gate electrodes.

[0004] On metal gate formation, problems include many processing issues such as chemical mechanical polishing ending point detection, spacer and liner loss, and poly gate loss. On source and drain contact formation, problems include shallow trench isolation loss and spacer oxide liner loss. In general, the process involves complex steps that increase cost.

[0005] Accordingly, it would be desirable to provide an improved method for manufacturing a metal gate absent the disadvantages found in the prior methods discussed above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a cross sectional view illustrating a substrate with a dielectric and a gate electrode located on the substrate;

[0007] Figure 2 is a cross sectional view illustrating an offset spacer adjacent the gate electrode and a light doping drain implanted in the substrate;

[0008] Figure 3 is a cross sectional view illustrating a first spacer adjacent the gate electrode and a second spacer adjacent the first spacer;

[0009] Figure 4 is a cross sectional view illustrating a source and a drain implanted in the substrate;

[0010] Figure 5 is a cross sectional view illustrating the first spacer etched so that its top surface is substantially even with the bottom surface of the second spacer;

[0011] Figure 6 is a cross sectional view illustrating a metal layer deposited on the device and in the space left after etching the first spacer;

[0012] Figure 7 is a cross sectional view illustrating the result of reacting the metal layer with the device to form a metal gate and a contact for the source and the drain, and then etching the unreacted metal layer;

[0013] Figure 8 is a cross sectional view illustrating a contact etch stop layer formed over the device;

[0014] Figure 9 is a cross sectional view illustrating a plurality of gates made of different materials formed on a substrate, each gate having substantially the same dielectric thickness;

[0015] Figure 10 is a cross sectional view illustrating a plurality of first gates made of different materials formed on a substrate, each gate having substantially the same dielectric thickness, and a second gate made of the same material one of the first gates formed on the substrate, the second gate have a dielectric thickness different than that of the first gates;

[0016] Figure 11 is a cross sectional view illustrating a plurality of first gates made of different materials formed on a substrate, each gate having substantially the same dielectric thickness, and a second gate made of a different material than either one of the first gates formed on the substrate, the second gate have a dielectric thickness different than that of the first gates;

DETAILED DESCRIPTION

[0017] In one embodiment, a semiconductor device 100, FIG. 1, begins its manufacture with a substrate 102. Substrate 102 can be of a variety of materials, including but not limited to bulk silicon and silicon on insulator (SOI), SiGe, and other proper semiconductor materials. A gate dielectric 104 and a gate electrode 106 are formed on substrate 102. The dielectric 104 can be of a variety of materials, including but not limited to oxides and high K materials, which include materials with K values larger than approximately 5, such as SiON, HfO_xSi_y, or HfO_2, or a combination thereof. The gate electrode 106 may be a variety of materials, including but not limited to polysilicon. To create the gate electrode 106 on dielectric 104 on substrate 102 configuration shown in FIG. 1, the gate electrode 106 and dielectric 104 are patterned using conventional photolithographic and etching processing of suitable methods known in the art. For example, one method is by patterning the surface of underlying material with a sequential process, including photoresist patterning, dry etching, and photoresist stripping. Further, photoresist patterning includes processing steps of photoresist coating, softbaking, mask aligning, pattern exposing, photoresist development, and hard baking.

[0018] Once the gate electrode 106 and the dielectric 104 are formed, an offset spacer 108, FIG. 2, is formed. Offset spacer 108 can be of a variety of materials, including but not limited to oxides such as SiO_2. Offset spacer 108 can be formed using suitable methods known in the art, such as chemical vapor deposition followed by etching. Following the formation of offset spacer 108, an implantation may be used to form light doping drain (LDD) 110 in substrate 102. Light doping drain 110 is offset by a length, A, from gate electrode 106 and dielectric 104 due to offset spacer 108. For clarity, light doping drain 110 is omitted from subsequent figures.

[0019] A spacer 112, FIG. 3, is then formed on the substrate 102 adjacent gate electrode 106 and gate dielectric 104. Spacer 112 can be formed over offset spacer 108, resulting in offset spacer becoming part of spacer 112. A spacer 114 is formed adjacent spacer 112. Spacer 112 can be a variety of materials, including oxides such as SiO_2. Spacer 114 can be a variety of materials, including but not limited to SiON, Si_3N_4, SiC, or a composite made of a combination of two or more of the aforementioned materials. Spacer 112 and 114 can be formed using suitable methods known in the art, such as chemical vapor deposition followed by dry etching.

[0020] Following spacer formation, a source 116, FIG. 4, and a drain 118 may be formed by doping such as implantation in substrate 102 and then annealing device 100.

[0021] Spacer 112 is now etched, FIG. 5, removing portions of spacer 112 that were adjacent to gate electrode 106 and spacer 114, and forming spacer 112'. In this embodiment, spacer 112 has been etched to be substantially even with a bottom surface 120 of spacer 114.

[0022] A metal layer 122, FIG. 6, is then deposited on device 100. Metal layer 122 may be a metal or a metal alloy, including but not limited to Ni, Co, Mo, W, Ti, Ta or other similar alloys. Metal layer 122 can be deposited using suitable methods known in the art, such as chemical vapor deposition or physical vapor deposition. The amount of metal layer 122 deposited on device 100 must be sufficient to react with the gate electrode 106 in order to form a metal gate.

[0023] The temperature of device 100 is then raised for a period of time, which causes metal layer 122 to react with gate electrode 106 to form a metal silicide gate ("metal gate") 106', FIG.

7. Temperature and time requirements will depend on the metal layer 122 and gate electrode 106 used. For a Ni metal layer and a polysilicon gate electrode, a temperature of 350 C – 600 C for 10 seconds to 5 minutes is sufficient to form a NiSi gate. Metal layer 122 may also react with substrate 102 to form a contact 126 for source 116 and drain 118. Then unreacted metal may be etched away.

[0024] After formation of metal gate 106', a layer 128, FIG. 8, is formed on device 100. Layer 128 can be made of a variety of materials, including but not limited to Si_3N_4, SiON, or a composite layer made of a combination of the aforementioned materials, and can be used as a contact etch stop layer. Layer 128 is formed using suitable methods known in the art, such as chemical vapor deposition.

[0025] With metal gate 106' and layer 128 formed, FIG. 8, device 100 includes metal gate 106' located on substrate 102, with gate dielectric 104 between metal gate 106' and substrate 102, and spacer 112' located on the substrate and adjacent metal gate 106'. Spacer 114 is adjacent spacer 112', surrounds metal gate 106', and is spaced apart from metal gate 106' so as to form a region 130 between metal gate 106' and spacer 114. Layer 128 is located inside region 130 and outside region 130, covering the device 100.

[0026] The metal gate manufacturing method allows gate electrodes of different materials with different gate dielectric thicknesses to be formed. This allows high performance core devices, which can use thinner gate dielectrics to increase the performance, to be manufactured with other core devices and input/output devices, which can use thicker gate dielectrics that reduce gate leakage. A combination of different gate electrode materials and different gate dielectric thickness may be tuned to optimize the performance of NMOS and PMOS.

[0027] In one embodiment, FIG. 9, a substrate 200 has a gate electrode 202 and a gate electrode 204 located on its surface. Substrate 200 can be made of a variety of materials, including but not limited to silicon or silicon on insulator. Each gate electrode 202 and 204 has a corresponding source 116 and drain 118 in the substrate 200. Gate electrode 202 has a dielectric 206a located between the gate electrode 202 and substrate 200. Gate electrode 204 has a

dielectric 206b located between the gate electrode 204 and substrate 200. Dielectrics 206a and 206b can be made of a variety of materials, including but not limited to oxides and high K materials, which include materials with K values larger than approximately 5, such as SiON, HfO_xSi_y, or HfO_2. For clarity spacers, contacts, and other structures on the device have been omitted. Dielectrics 206a and 206b have substantially the same gate dielectric thickness H. Gate electrode 202 is made of a material A, which includes but is not limited to a variety of materials such as polysilicon, metal, a metal alloy, a metal silicide, or a composite layer made of a combination of two or more of the aforementioned materials. Gate electrode 204 is made of a material B, which is different from that of material A, and includes but is not limited to a variety of materials such as polysilicon, metal, a metal alloy, a metal silicide, or a composite layer made of a combination of two or more of the aforementioned materials.

[0028] In another embodiment, FIG. 10, a substrate 200 has a gate electrode 202, a gate electrode 204, and a gate electrode 206 located on its surface. Substrate 200 can be made of a variety of materials, including but not limited to silicon or silicon on insulator. Each gate electrode 202, 204, and 206 has a corresponding source 116 and drain 118 implanted in the substrate 200. Gate electrode 202 has a dielectric 208a located between the gate electrode 202 and substrate 200. Gate electrode 204 has a dielectric 208b located between the gate electrode 204 and substrate 200. Gate electrode 206 has a dielectric 210 located between the gate electrode 206 and substrate 200. Dielectrics 208a, 208b, and 210 can be made of a variety of materials, including but not limited to oxides and high K materials, which include materials with K values larger than approximately 5, such as SiON, HfO_xSi_y, or HfO_2. For clarity spacers, contacts, and other structures on the device have been omitted. Dielectrics 208a and 208b have substantially the same gate dielectric thickness H. Dielectric 210 has a gate dielectric thickness I that is greater than that of gate dielectric thickness H. Alternatively, gate dielectric thickness I may be less than that of gate dielectric thickness H. Gate electrode 202 is made of a material A, which includes but is not limited to a variety of materials such as polysilicon, metal, a metal alloy, a metal silicide, or a composite layer made of a combination of two or more of the aforementioned materials. Gate electrode 204 is made of a material B, which is different from that of material A, and includes but is not limited to a variety of materials such as polysilicon,

metal, a metal alloy, a metal silicide, or a composite layer made of a combination of two or more of the aforementioned materials. Gate electrode 206 is made of either material A or material B.

[0029] In another embodiment, FIG. 11, a substrate 200 has a gate electrode 202, a gate electrode 204, and a gate electrode 206 located on its surface. Substrate 200 can be made of a variety of materials, including but not limited to silicon or silicon on insulator. Each gate electrode 202, 204, and 206 has a corresponding source 116 and drain 118 implanted in the substrate 200. Gate electrode 202 has a dielectric 208a located between the gate electrode 202 and substrate 200. Gate electrode 204 has a dielectric 208b located between the gate electrode 204 and substrate 200. Gate electrode 206 has a dielectric 210 located between the gate electrode 206 and substrate 200. Dielectrics 208a, 208b, and 210 can be made of a variety of materials, including but not limited to oxides and high K materials, which include materials with K values larger than approximately 5, such as SiON, HfO_xSi_y, or HfO_2. For clarity spacers, contacts, and other structures on the device have been omitted. Dielectrics 208a and 208b have substantially the same gate dielectric thickness H. Dielectric 210 has a gate dielectric thickness I that is greater than that of gate dielectric thickness H. Alternatively, gate dielectric thickness I may be less than that of gate dielectric thickness H. Gate electrode 202 is made of a material A, which includes but is not limited to a variety of materials such as polysilicon, metal, a metal alloy, a metal silicide, or a composite layer made of a combination of two or more of the aforementioned materials. Gate electrode 204 is made of a material B, which is different from that of material A, and includes but is not limited to a variety of materials such as polysilicon, metal, a metal alloy, a metal silicide, or a composite layer made of a combination of two or more of the aforementioned materials. Gate electrode 206 is made of a material C, which is different from that of material A or B, and includes but is not limited to a variety of materials such as polysilicon, metal, a metal alloy, a metal silicide, or a composite layer made of a combination of two or more of the aforementioned materials.

[0030] Although only a few exemplary embodiments of this invention have been described in detail above, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and

advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention as defined in the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

a plurality of gate electrodes located on the substrate;

a gate dielectric located between each gate electrode and the substrate, the gate dielectrics being substantially the same thickness;

at least one of the gate electrodes made of a first material; and

at least one of the gate electrodes made of a second material which is different from the first material.

2. The semiconductor device of claim 1 wherein the substrate is silicon on insulator.

3. The semiconductor device of claim 1 wherein the first material is polysilicon.

4. The semiconductor device of claim 1 wherein the second material is selected from the group consisting of a metal, a metal alloy, a metal silicide, and a combination thereof.

5. The semiconductor device of claim 1 wherein the second material includes a plurality of materials.

6. The semiconductor device of claim 1 wherein at least one gate dielectric is an oxide.

7. The semiconductor device of claim 1 wherein at least one gate dielectric is a high K material.

8. A semiconductor device comprising:

a substrate;

a plurality of first gate electrodes located on the substrate;

a first gate dielectric located between each first gate electrode and the substrate, the first gate dielectrics being substantially the same thickness;

at least one of the first gate electrodes made of a first material;

at least one of the first gate electrodes made of a second material which is different from the first material;

at least one second gate electrode located on the substrate, the at least one second gate electrode being made of either the first material or the second material; and

a second gate dielectric located between each at least one second gate electrode and the substrate, the second gate dielectrics having a thickness different from that of the first gate dielectrics.

9. The semiconductor device of claim 8 wherein the substrate is silicon on insulator.

10. The semiconductor device of claim 8 wherein the first material is polysilicon.

11. The semiconductor device of claim 8 wherein the second material is selected from the group consisting of a metal, a metal alloy, a metal silicide, and a combination thereof.

12. The semiconductor device of claim 8 wherein the second material includes a plurality of materials.

13. The semiconductor device of claim 8 wherein at least one gate dielectric is an oxide.

14. The semiconductor device of claim 8 wherein at least one gate dielectric is a high K material.

15. A semiconductor device comprising:

a substrate;

a plurality of first gate electrodes located on the substrate;

a first gate dielectric located between each first gate electrode and the substrate, the first gate dielectrics being substantially the same thickness;

at least one of the first gate electrodes made of a first material;

at least one of the first gate electrodes made of a second material which is different from the first material;

at least one second gate electrode located on the substrate, the at least one second gate electrode being made of a third material which is different from the first and second material; and

a second gate dielectric located between each at least one second gate electrode and the substrate, the second gate dielectrics having a thickness different from that of the first gate dielectrics.

16. The semiconductor device of claim 15 wherein the substrate is silicon on insulator.

17. The semiconductor device of claim 15 wherein the first material is polysilicon.

18. The semiconductor device of claim 15 wherein the second material is a metal or metal alloy.

19. The semiconductor device of claim 15 wherein the third material is a metal silicide.

20. The semiconductor device of claim 15 further wherein the third material is a plurality of materials.

21. The semiconductor device of claim 15 wherein at least one gate dielectric is an oxide.

22. The semiconductor device of claim 15 wherein at least one gate dielectric is a high K material.

23. A semiconductor device comprising:

a substrate;

a metal gate electrode located on the substrate; and

a plurality of spacers, the plurality of spacers including a first spacer adjacent to the metal gate electrode and a second spacer adjacent to the first spacer.

24. The semiconductor device of claim 23 wherein the metal gate electrode is a metal silicide.

25. The semiconductor device of claim 23 wherein the first spacer or second spacer is selected from the group consisting of SiON, Si_3N_4, SiC, and a combination thereof.

26. A semiconductor device comprising:

a substrate;

a gate electrode located on the substrate;

a first spacer surrounding the gate electrode and spaced apart from the gate electrode to form a first region therebetween; and

a second spacer located both inside and outside of the first region.

27. The semiconductor device of claim 26 wherein the gate electrode is a metal silicide.

28. The semiconductor device of claim 26 wherein the first spacer or second spacer is selected from the group consisting of SiON, Si_3N_4, SiC, and a combination thereof.

29. A semiconductor device comprising:

a substrate;

a gate electrode located on the substrate;

a first spacer located on the substrate and adjacent to the gate electrode;

a second spacer located adjacent the first spacer, which surrounds the gate electrode and is spaced apart from the gate electrode to form a first region therebetween; and

a third spacer located both inside and outside of the first region.

30. The semiconductor device of claim 29 wherein the gate electrode is a metal silicide.

31. The semiconductor device of claim 29 wherein the first spacer is SiO_2.

32. The semiconductor device of claim 29 wherein the second spacer or third spacer is selected from the group consisting of SiON, Si_3N_4, SiC, and a combination thereof.

33. A method for manufacturing a metal gate on a semiconductor device comprising:

providing a substrate including a gate electrode located on the substrate;

forming a plurality of layers, including a first layer located on the substrate and the gate electrode and a second layer adjacent the first layer;

etching the layers to form a plurality of adjacent spacers, including a first spacer located on the substrate and adjacent the gate electrode and a second spacer adjacent the first spacer;

etching the first spacer;

forming a metal layer on the device immediately adjacent to the gate electrode; and

reacting the metal layer with the gate electrode.

34. The method of claim 33 wherein the gate electrode is polysilicon.

35. The method of claim 33 wherein the first layer and first spacer are SiO_2.

36. The method of claim 33 wherein the second layer and the second spacer are Si_3N_4.

37. The method of claim 33 wherein the plurality of layers are formed by chemical vapor deposition.

38. The method of claim 33 wherein the first spacer is etched so that its top surface is substantially the same height as the bottom surface of the second spacer.

39. The method of claim 33 wherein metal layer is Ni.

40. The method of claim 33 wherein reacting the metal layer with the gate electrode results in a NiSi gate electrode.

41. The method of claim 33 further comprising:

etching the layers to expose the substrate; and

doping the substrate to form a source and a drain.

42. The method of claim 41 further comprising:

reacting the metal layer with the substrate to form contacts for the source and the drain.

43. The method of claim 33 further comprising:

etching the unreacted metal layer;

forming a contact etch stop layer on the device.

44. The method of claim 43 wherein the contact etch stop layer is selected from the group consisting of SiON, Si_3N_4, and a combination thereof.

45. A method for manufacturing a metal gate on a semiconductor device comprising:

providing a substrate including a gate electrode located on the substrate;

forming an offset layer;

etching the offset layer to form an offset spacer adjacent to the gate electrode;

forming a plurality of layers, including a first layer located on the substrate and the gate electrode and a second layer adjacent the first layer;

etching the layers to form a plurality of adjacent spacers, including a first spacer located on the substrate and adjacent the gate electrode and a second spacer adjacent the first spacer;

etching the first spacer;

forming a metal layer on the device that is immediately adjacent to the gate electrode; and

reacting the metal layer with the gate electrode.

46. The method of claim 45 wherein the gate electrode is polysilicon.

47. The method of claim 45 wherein the first layer and first spacer are SiO_2.

48. The method of claim 45 wherein the second layer and the second spacer are Si_3N_4.

49. The method of claim 45 wherein the plurality of layers and the offset layer are formed by chemical vapor deposition.

50. The method of claim 45 wherein the first spacer is etched so that its top surface is substantially the same height as the bottom surface of the second spacer.

51. The method of claim 45 wherein metal layer is Ni.

52. The method of claim 45 wherein reacting the metal layer with the gate electrode results in a NiSi gate electrode.

53. The method of claim 45 further comprising:
etching the layers to expose the substrate; and
doping the substrate to form a source and a drain.

54. The method of claim 53 further comprising:
reacting the metal layer with the substrate to form contacts for the source and the drain.

55. The method of claim 45 further comprising:
etching the unreacted metal layer;
forming a contact etch stop layer on the device.

56. The method of claim 55 wherein the contact etch stop layer is selected from the group consisting of SiON, Si_3N_4, and a combination thereof.