

PATENT SPECIFICATION (11) 1 412 549

- (21) Application No. 40257/73 (22) Filed 24 Aug 1973
 (31) Convention Application No. 85270/72 (32) Filed 28 Aug 1972 in (19)
 (33) Japan (JA)
 (44) Complete Specification published 5 Nov 1975
 (51) INT CL² H03B 5/36
 (52) Index at acceptance
 H3T 1G3X 2C 2J 2T3F 2T4 3J
 3N 4D 5S



(54) "IMPROVEMENTS IN OR RELATING TO PIEZO-ELECTRIC CRYSTAL OSCILLATORS"

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese Company, of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:-

This invention relates to piezo-electric crystal oscillators in which the operating point is set in response to self bias generated during self oscillation. More specifically the invention relates to such oscillators of the kind comprising an odd number (including unity) of complementary inverter stages using MOS field effect transistors and in which output drain electrode voltage is fed back through a high value resistance to an input gate electrode. As will be more clearly seen later, the principal object of the invention is to provide improved oscillators of this kind which shall be such as to be able to be incorporated in a monolithic integrated circuit structure and shall be, at the same time, of good reliability, able to be manufactured relatively cheaply by mass production methods and of high stability of frequency despite changes of ambient temperature. Although the invention is not limited to its application thereto, it is primarily intended for, and of great practical advantage for, application to the time standard oscillators of electronic timepieces.

According to one aspect of the said preferred invention, there is provided a piezo-electric oscillator comprising an IG-FET inverter stage or an odd number sequence of cascaded complementary IG-FET inverter stages, a piezo-electric crystal connected in a feed back path across said inverter stage or inverter stage sequence, and a self-bias generating resistance also connected in a resistance feed back path across said inverter stage or across at least part of said inverter stage sequence and wherein said resistance is a resistance manifested by an IG-FET source-drain path. Where there is only one inverter stage, the first and last stage will, of course, be the same stage. A phase correcting

phase shifter may be included in series with said inverter stage or in series in or with said inverter stage sequence. A phase correcting phase shifter may be provided at the output side of said inverter stage or inverter stage sequence so that self-bias is applied through said phase shifter, in which case said phase shifter may comprise at least one MOS transistor, and preferably at least one pair of complementary MOS transistors. The aforesaid resistance feed back path may comprise at least one pair of complementary MOS transistors arranged to provide a resistance in said phase shifter.

According to another aspect of the invention there is provided an oscillator comprising a piezo-electric crystal, at least one pair of complementary MOS field effect transistors connected in an oscillation sustaining feed-back path across the crystal to sustain oscillation thereof, one of each pair being a P-channel transistor and the other an N-channel transistor and the crystal being connected between the output drain electrode terminal of the last pair and the input gate electrode terminal of the first pair; a capacitor connected between said output drain terminal and earth and/or a capacitor connected between said input gate terminal and earth; and a self-bias generating feed back circuit connected across the whole or part of said oscillation sustaining path and determining the operating point of the oscillator, said self-bias generating feed back circuit including at least one feed back field effect transistor with its source-drain path connected between a drain electrode output terminal of a transistor stage in said oscillation sustaining path and a gate electrode input terminal of a stage in said oscillation sustaining path.

According to another aspect of the invention a piezo-electric oscillator comprises at least one pair of complementary field effect transistors, a piezo-electric crystal, and MOS transistors the source-drain paths of which are utilised to provide feedback resistance and which are connected between an output terminal and an input terminal of said complementary field effect transistors, a capacitor and a resistor

being connected to said output terminal for phase control.

In this specification and in the claims which follow, the expression "pair of complementary field effect transistors" is used to mean a pair of field effect transistors of opposite conducting types with their input electrodes in parallel and their output electrodes in parallel and the expression "pair of MOS field effect transistors" is used to express a similar, corresponding meaning.

An oscillator in accordance with this invention is preferably constructed as a monolithic I.C. structure including the circuitry apart from the crystal, which is external to and connected to said structure.

The invention includes electronic timepieces having a time standard oscillator constituted by an oscillator in accordance with the invention. The invention is illustrated in and further described with reference to the accompanying drawings, in which:-

Figure 1 shows a known complementary inverter employing MOS field effect transistors (FET), one being an N-channel transistor and the other a P-channel transistor.

Figure 2 shows a known quartz oscillator circuit employing a plurality of inverter stages as represented in Figure 1.

Figure 3 is an explanatory graphical figure illustrating the drain current I_d - drain voltage V_d characteristic of an MOS-FET.

Figure 4 shows a preferred way of obtaining a high resistance used as a feed back resistance in an oscillator in accordance with this invention and

Figures 5 and 6 illustrate oscillator embodiments of this invention.

A general description of the references in the drawings will be of assistance as a preliminary to describing them in detail.

In Figure 1, Trp is a P-channel MOS-FET; Trn is an N-channel MOS-FET; Sp, Dp, Gp are, respectively, the source, drain and gate of Trp; and Sn, Dn, Gn are respectively the source, drain and gate of Trn.

In Figure 2, I_1 to I_n are cascaded inverters as shown in Figure 1 and consisting of complementary MOS-FETs; P.C. is a phase shifting phase adjusting circuit; G_0 is the input terminal of the first inverter stage; D_n is the output terminal of the last inverter stage; D_i is the output of an intermediate inverter stage; R_f is a feed-back resistance for setting the bias; C_g is an input capacitor; C_d is an output capacitor; and X is a quartz crystal vibrator.

In Figure 3, which shows the I_d - V_d characteristic of an MOS-FET, I_d is a drain current; V_d is drain voltage; V_{ge} is effective gate voltage; and R_e is effective resistance.

Figure 4 illustrates a preferred way of employing MOS-FETs to provide a feed-back resistance in an oscillator in accordance with this invention.

In Figure 5, which shows one form of quartz crystal oscillator in accordance with this

invention, Trpf is a P-channel MOS-FET operating as a feed-back resistance; and Trnf is an N-channel MOS-FET operating as a feed-back resistance.

Figure 6 shows another example of a quartz crystal oscillator in accordance with this invention wherein the invention is applied to a phase adjusting phase shifter in the oscillator. In Figure 6 Trpc is a phase compensating P-channel MOS-FET; Trnc is a phase compensating N-channel MOS-FET; and Cd is a drain parasitic capacitance.

Referring to Figure 1 this shows a complementary inverter I_1 (represented diagrammatically as a whole by the triangular representation shown to the left of the equals sign in the figure) which comprises (as shown in some detail to the right of the said equals sign) an MOS P-channel field effect transistor Trp and an MOS N-channel field effect transistor Trn. As shown in Figure 2 there is provided a cascaded sequence of such inverters I_1 to I_n . At some point in the sequence, i.e. between two successive stages, is inserted a phase adjusting phase shifter PC. The output terminal of the sequence in which the phase shifter is inserted is referenced D_i and the input terminal thereof is referenced G_0 . The drain electrode D_n of the MOS-FET in the last stage I_n is connected back to the gate electrode of the MOS-FET in the first stage I_1 through a quartz crystal vibrator X. In order to attain phase compensation, an output capacitor Cd is connected between the output drain terminal of the MOS-FET in the last stage I_n and an input capacitor C_g is connected between the input gate terminal of the MOS-FET in the first stage I_1 and earth. The operating point of the sequence of inverters is set by feed back through a resistance R_f back from the output drain electrode of a suitably chosen intermediate inverter stage to the input terminal G_0 . This intermediate stage is referenced I_i and the terminal from which this feed back is taken is referenced D_i . In this way self oscillation is generated in response to self-bias. In general, the resistance R_f will be several megohms or more, it being desirable to make it as high as possible consistent with its not materially influencing the relations in the circuit. This resistance is, in practice, either an externally connected resistance or constituted by a thin-film resistance forming part of an integrated circuit (I.C.) structure. In either case the provision and connection of the said resistance R_f involves an increase in the number of connection contacts necessary and this has the practical defect of diminishing reliability and increasing the liability to the occurrence of faults. It is therefore desirable to avoid these extra contacts and connections by employing a monolithic I.C. structure incorporating the resistance in question but if it is sought to do this by using a diffused layer for the resistance, the difficulty is encountered that consideration of specific resistance limits the value of resistance

attainable, and the fact that the area available for it in a monolithic I.C. structure is very small makes the production in this way of a resistance of the value required, very difficult or even impractical. If a polycrystalline silicon is employed for the resistance in order to avoid this difficulty, variations in ambient temperature, such as are likely to occur in practice, produce such changes in resistance as to be likely to cause instability of the frequency of oscillation.

The present invention seeks to avoid the above-mentioned defects and difficulties and, as will be seen later, it achieves this object by making use of the high value channel resistance, of an MOS field effect transistor. The relation between current and voltage in an MOS field effect transistor is, in general, as follows:-

$$\begin{aligned} 0 < V_d < V_{ge} \quad I_d &= \beta (V_{ge} \cdot V_d - 1/2 V_d^2) \\ V_{ge} < V_d \quad I_d &= 1/2 \beta V_{ge}^2 \end{aligned}$$

where, V_{ge} is the effective gate voltage, V_d is the drain voltage, I_d is the drain current, and β equals $\mu \cdot C_{ox} \cdot W/L$, where μ is the mobility on the channel surface, C_{ox} is the capacitance per unit area of the gate insulating film, and W/L is a ratio of width to length of the channel. The equivalent resistance R_e equals V_d/I_d , and it assumes the minimum R_{mini} when $V_d = 0$, as illustrated graphically in Figure 3, when:-

$$\begin{aligned} R_e = \frac{V_d}{I_d} &= \frac{1}{\beta (V_{ge} - 1/2 V_d)} \\ R_{mini} &= \frac{1}{\beta \cdot V_{ge}} \end{aligned}$$

It follows from the foregoing that at least several megohms of resistance can be easily obtained if the ratio W/L is chosen small enough because $\beta \propto W/L$. The foregoing assumes that the effective gate voltage V_{ge} is fixed. However if V_{ge} changes in response to changes in the drain voltage V_d , the effective resistance R_e is inversely proportional to W/L , i.e. the ratio of width to length of the channel. In fact, the mobility μ is about $600 \text{ cm}^2/\text{V sec}$ in the case of an N-channel FET and about $300 \text{ cm}^2/\text{V sec}$ in the case of a P-channel FET, and, with these figures, if the gate capacitance C_{ox} per unit area is $3 \times 10^{-8} \text{ F/cm}^2$ and the effective gate voltage V_{ge} is 0.5 V (with an N-channel FET) a minimum effective resistance of 5 megohms, can be easily obtained within a quite small area by making the ratio W/L not more than 0.02. In the case of a P channel FET a resistance of at least 5 megohms is attainable by making W/L not more than 0.075. As for the matter of temperature characteristics, a much better one is obtainable than if a polycrystalline silicon resistance is employed for the resistance because increase in a temperature reduces the

mobility μ and increase the effective gate voltage V_{ge} , so that these two effects act oppositely so as to tend to cancel one another out.

Figure 4 illustrates one way of attaining the required resistance R_f in carrying out this invention. The said resistance R_f is diagrammatically represented to the left of the equals sign in Figure 4 while to the right of this sign is shown the circuitry by which this resistance is manifested. In this part of Figure 4, Tr_n is an N-channel transistor and Tr_p is a P channel transistor having gate terminals G_n and G_p respectively. These transistors are connected effectively in parallel.

Figure 5 shows an embodiment of this invention in which, for simplicity of showing, there is only one complementary inverter stage. The voltages applied to the gates G_n and G_p of transistors Tr_{nf} and Tr_{pf} having effectively high resistance and feeding back from drain output to gate input are such as to turn these transistors ON alternately in successive half periods. For example, the positive side of a source voltage may be connected to the gate G_n of the N-channel transistor Tr_{nf} , and the negative side thereof, to the gate G_p . It is convenient to utilize the potential of the drain connecting terminal D_O and the gate connecting terminal G_O .

A resistance obtained in this way can be utilized for a resistance in a phase correcting phase shifting circuit, for phase compensation. This is illustrated in Figure 6 where utilisation is made of the drain parasitic capacitance C_d of an MOS field effect transistor. Here the gates G_{nc} and G_{pc} of transistors Tr_{nc} and Tr_{pc} in a phase shifting circuit operate in an equivalent way, so far as voltage is concerned, as do the gates in the feed-back transistors Tr_{nf} and Tr_{pf} .

Although the invention is of general application, it is primarily intended for and is of great advantage when used for the time standard quartz oscillator of an electronic timepiece. In such a case, if a capacitor is incorporated in the chip when the invention is used to provide such an oscillator the said oscillator can be constructed by a monolithic I.C. structure and only two externally connected elements are necessary, namely, a piece of quartz crystal and a small frequency adjusting or regulating capacitor. The resulting time standard oscillator is such as greatly to facilitate the production of a relatively low cost, relatively very small electronic timepiece of very good reliability and ease of manufacture by mass production methods.

WHAT WE CLAIM IS:-

1. A piezo-electric oscillator comprising an IG-FET inverter stage or an odd number sequence of cascaded complementary IG-FET inverter stages, a piezo-electric crystal connected in a feed back path across said inverter stage or inverter stage sequence, and a self-bias generating resistance also connected in a



attainable, and the fact that the area available for it in a monolithic I.C. structure is very small makes the production in this way of a resistance of the value required, very difficult or even impractical. If a polycrystalline silicon is employed for the resistance in order to avoid this difficulty, variations in ambient temperature, such as are likely to occur in practice, produce such changes in resistance as to be likely to cause instability of the frequency of oscillation.

The present invention seeks to avoid the above-mentioned defects and difficulties and, as will be seen later, it achieves this object by making use of the high value channel resistance, of an MOS field effect transistor. The relation between current and voltage in an MOS field effect transistor is, in general, as follows:-

$$0 < V_d < V_{ge} \quad I_d = \beta (V_{ge} \cdot V_d - 1/2 V_d^2)$$

$$V_{ge} < V_d \quad I_d = 1/2 \beta V_{ge}^2$$

where, V_{ge} is the effective gate voltage, V_d is the drain voltage, I_d is the drain current, and β equals $\mu \cdot C_{ox} \cdot W/L$, where μ is the mobility on the channel surface, C_{ox} is the capacitance per unit area of the gate insulating film, and W/L is a ratio of width to length of the channel. The equivalent resistance R_e equals V_d/I_d , and it assumes the minimum R_{mini} when $V_d = 0$, as illustrated graphically in Figure 3, when:-

$$R_e = \frac{V_d}{I_d} = \frac{1}{\beta (V_{ge} - 1/2 V_d)}$$

$$R_{mini} = \frac{1}{\beta \cdot V_{ge}}$$

It follows from the foregoing that at least several megohms of resistance can be easily obtained if the ratio W/L is chosen small enough because $\beta \propto W/L$. The foregoing assumes that the effective gate voltage V_{ge} is fixed. However if V_{ge} changes in response to changes in the drain voltage V_d , the effective resistance R_e is inversely proportional to W/L , i.e. the ratio of width to length of the channel. In fact, the mobility μ is about $600 \text{ cm}^2/\text{V sec}$ in the case of an N-channel FET and about $300 \text{ cm}^2/\text{V sec}$ in the case of a P-channel FET, and, with these figures, if the gate capacitance C_{ox} per unit area is $3 \times 10^{-8} \text{ F/cm}^2$ and the effective gate voltage V_{ge} is 0.5 V (with an N-channel FET) a minimum effective resistance of 5 megohms, can be easily obtained within a quite small area by making the ratio W/L not more than 0.02. In the case of a P channel FET a resistance of at least 5 megohms is attainable by making W/L not more than 0.075. As for the matter of temperature characteristics, a much better one is obtainable than if a polycrystalline silicon resistance is employed for the resistance because increase in a temperature reduces the

mobility μ and increase the effective gate voltage V_{ge} , so that these two effects act oppositely so as to tend to cancel one another out.

Figure 4 illustrates one way of attaining the required resistance R_f in carrying out this invention. The said resistance R_f is diagrammatically represented to the left of the equals sign in Figure 4 while to the right of this sign is shown the circuitry by which this resistance is manifested. In this part of Figure 4, Tr_n is an N-channel transistor and Tr_p is a P channel transistor having gate terminals G_n and G_p respectively. These transistors are connected effectively in parallel.

Figure 5 shows an embodiment of this invention in which, for simplicity of showing, there is only one complementary inverter stage. The voltages applied to the gates G_n and G_p of transistors Tr_{nf} and Tr_{pf} having effectively high resistance and feeding back from drain output to gate input are such as to turn these transistors ON alternately in successive half periods. For example, the positive side of a source voltage may be connected to the gate G_n of the N-channel transistor Tr_{nf} , and the negative side thereof, to the gate G_p . It is convenient to utilize the potential of the drain connecting terminal D_O and the gate connecting terminal G_O .

A resistance obtained in this way can be utilized for a resistance in a phase correcting phase shifting circuit, for phase compensation. This is illustrated in Figure 6 where utilisation is made of the drain parasitic capacitance C_d of an MOS field effect transistor. Here the gates G_{nc} and G_{pc} of transistors Tr_{nc} and Tr_{pc} in a phase shifting circuit operate in an equivalent way, so far as voltage is concerned, as do the gates in the feed-back transistors Tr_{nf} and Tr_{pf} .

Although the invention is of general application, it is primarily intended for and is of great advantage when used for the time standard quartz oscillator of an electronic timepiece. In such a case, if a capacitor is incorporated in the chip when the invention is used to provide such an oscillator the said oscillator can be constructed by a monolithic I.C. structure and only two externally connected elements are necessary, namely, a piece of quartz crystal and a small frequency adjusting or regulating capacitor. The resulting time standard oscillator is such as greatly to facilitate the production of a relatively low cost, relatively very small electronic timepiece of very good reliability and ease of manufacture by mass production methods.

WHAT WE CLAIM IS:-

1. A piezo-electric oscillator comprising an IG-FET inverter stage or an odd number sequence of cascaded complementary IG-FET inverter stages, a piezo-electric crystal connected in a feed back path across said inverter stage or inverter stage sequence, and a self-bias generating resistance also connected in a

- resistance feed back path across said inverter stage or across at least part of said inverter stage sequence and wherein said resistance is a resistance manifested by an IG-FET source-drain path.
2. An oscillator as claimed in claim 1 wherein a phase correcting phase shifter is included in series with said inverter stage or in series in or with said inverter stage sequence.
3. An oscillator as claimed in claim 1 wherein a phase correcting phase shifter is so provided at the output side of said inverter stage or inverter stage sequence so that self-bias is applied through said phase shifter.
4. An oscillator as claimed in claim 3 wherein said phase shifter comprises at least one MOS transistor.
5. An oscillator as claimed in claim 3 wherein said phase shifter comprises at least one pair of complementary MOS transistors.
6. An oscillator as claimed in claim 3, wherein said resistance feed-back path comprises at least one pair of complementary MOS transistors arranged to provide a resistance in said phase shifter.
7. An oscillator comprising a piezo-electric crystal; at least one pair of complementary MOS field effect transistors connected in an oscillation sustaining feed-back path across the crystal to sustain oscillation thereof, one of each pair being a P-channel transistor and the other an N-channel transistor and the crystal being connected between the output drain electrode terminal of the last pair and the input gate electrode terminal of the first pair; a capacitor connected between said output drain terminal and earth and/or a capacitor connected between said input gate terminal and earth; and a self-bias generating feed back circuit connected across the whole or part of said oscillation sustaining path and determining the operating point of the oscillator said self-bias generating feed back circuit including at least one feed-back effect transistor with its source drain path connected between a drain electrode output terminal of a transistor stage in said oscillation sustaining path and a gate electrode input terminal of a stage in said oscillation sustaining path.
8. A piezo-electric oscillator comprising at least one pair of complementary field effect transistors, a piezo-electric crystal, and MOS transistors the source-drain paths of which are utilised to provide feedback resistance and which are connected between an output terminal and an input terminal of said complementary field effect transistors, a capacitor and a resistor being connected to said output terminal for phase control.
9. Piezo-electric oscillators substantially as herein described with reference to Figures 4, 5 and 6 of the accompanying drawings.
10. An oscillator as claimed in any of the preceding claims and constructed as a monolithic I.C. structure including the circuitry apart from the crystal, which is external to and connected to said structure.
11. An electronic timepiece having a time standard oscillator as claimed in any of the preceding claims.
- J. MILLER & CO.
262 High Holborn,
London, WC1V 7EF

