

14 Feb 03

2003017456



162162

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
28 March 2002 (28.03.2002)

PCT

(10) International Publication Number
WO 02/025454 A3(51) International Patent Classification⁷: G11C 5/00

(21) International Application Number: PCT/US01/28627

(22) International Filing Date:
14 September 2001 (14.09.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/232,596 14 September 2000 (14.09.2000) US
09/666,528 18 September 2000 (18.09.2000) US

(71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): HALBERT, John [US/US]; 15045 SW Emerald Court, Beaverton, OR 97007 (US). BONELLA, Randy, M. [US/US]; 4122 SW Garden Home Road, Portland, OR 97219 (US).

(74) Agents: MAKUCH, Joseph, S.; Marger, Johnson & McCullough, 1030 S.W. Morrison Street, Portland, OR 97205 et al. (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

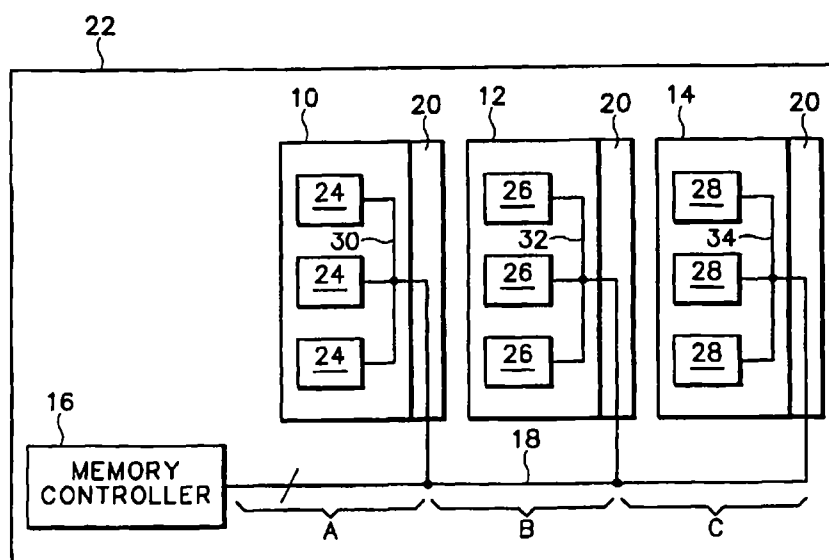
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

[Continued on next page]

(54) Title: MEMORY MODULE HAVING BUFFER FOR ISOLATING STACKED MEMORY DEVICES



(57) Abstract: The present invention utilizes a buffer to isolate a stack of memory devices, thereby taking advantage of the increased memory density available from stacked memory devices while reducing capacitive loading. A memory module in accordance with the present invention may include a stack of memory devices and a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus. In a memory system in accordance with the present invention, multiple buffered stacks of memory devices are preferably coupled in a point-to-point arrangement, thereby further reducing capacitive loading.

WO 02/025454 A3



ACTION

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(88) Date of publication of the international search report:

22 August 2002