ABSTRACT

Three Dimensional IC Package Module

In the present invention a high performance package is described where semiconductor chips are stacked together in a pancake like fashion with inter chip communications facilitated by chip to chip vias formed through the material of each chip. The chip to chip vias are created by etching and filling a hole from the back of a chip through the silicon substrate stopping at the first level of metalization and invoking the wiring of the chip to complete the path to the top side. The chip in the stack are aligned so that chip to chip vias form columns. Signal and power can travel the full length of a column from the bottom chip to the chip on top, or the wiring within the chips can interrupt the signal flow and form interstitial connections. Interstitial connections can also be used to enhance the wireability between chips in the stack. To accommodate cooling the chips in the stack are made in varying sizes and are ordered in size from the largest at the bottom of the stack to the smallest at the top of the stack. This provides a stair case like structure to allow heat sinks to be attached to each step formed by a chip and the smaller chip above. An interface substrate sits at the bottom of the stack and provides for communication external to the stack by connecting the columns of chip to chip vias to an array of pins to mate with a connector. The short distances that signals must travel lends this three dimensional stacked chip package to high performance for off chip communications.

Figure 1a

This Sheet Has Been Replaced

