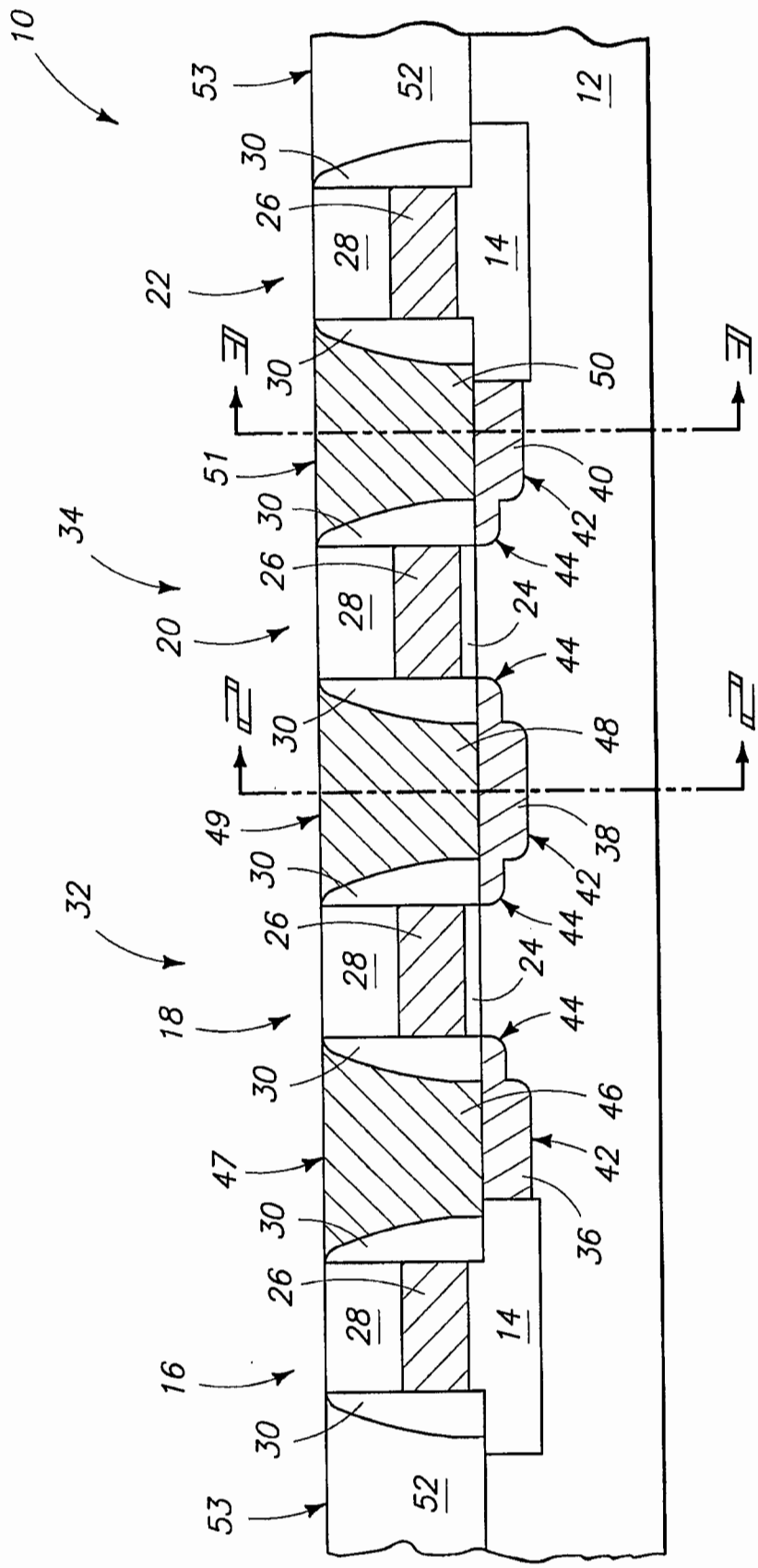

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FIG II

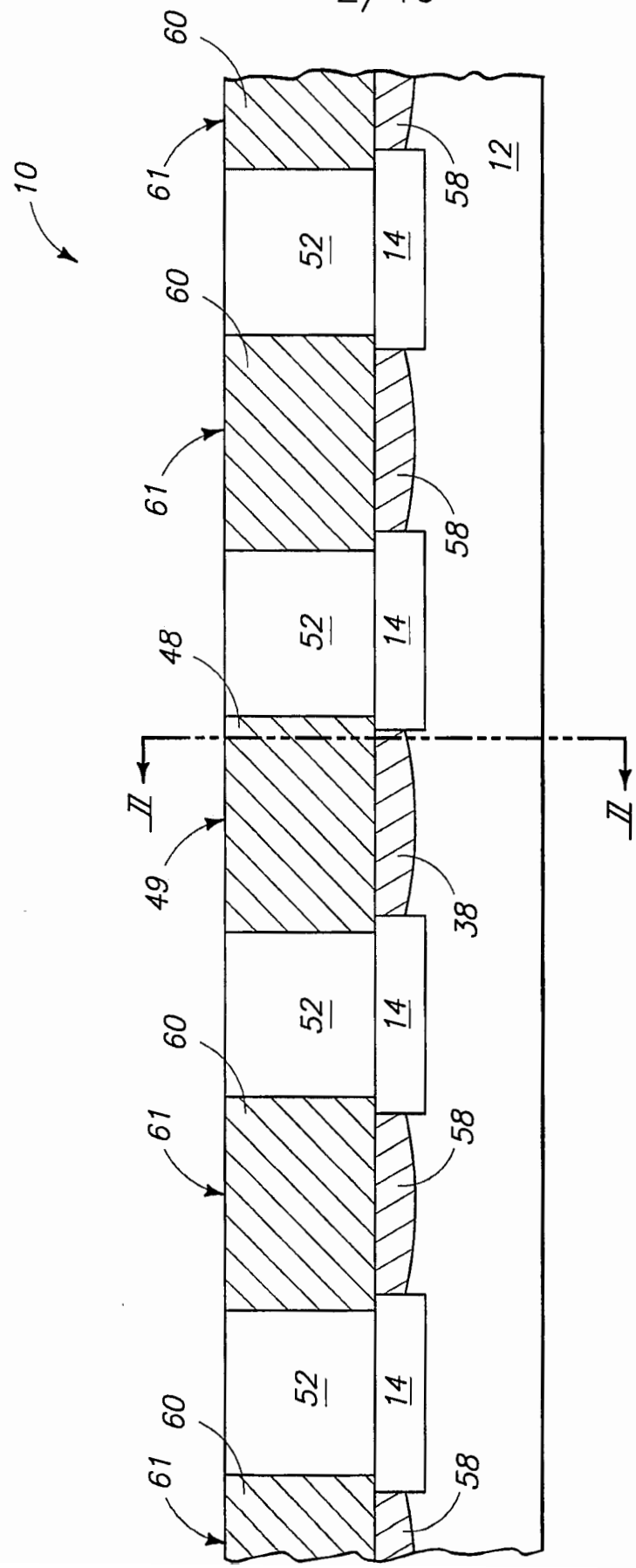

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FIG. 2

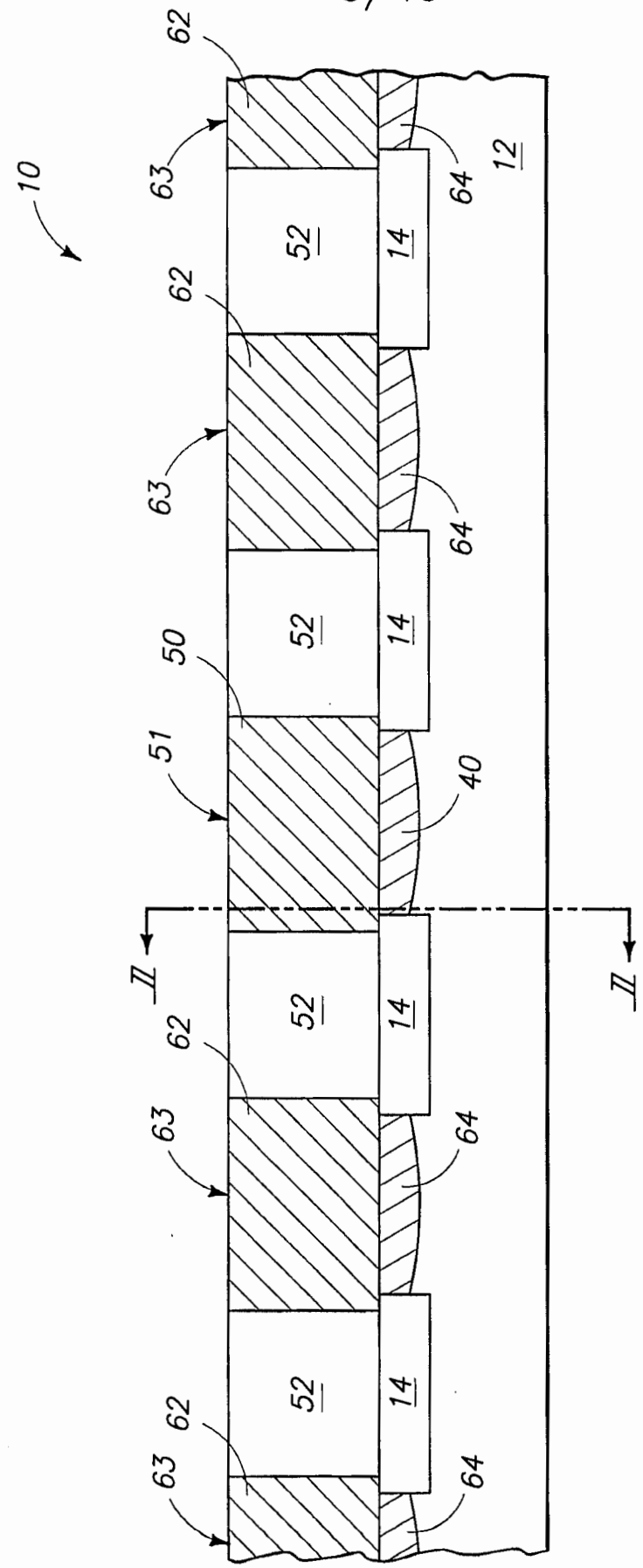
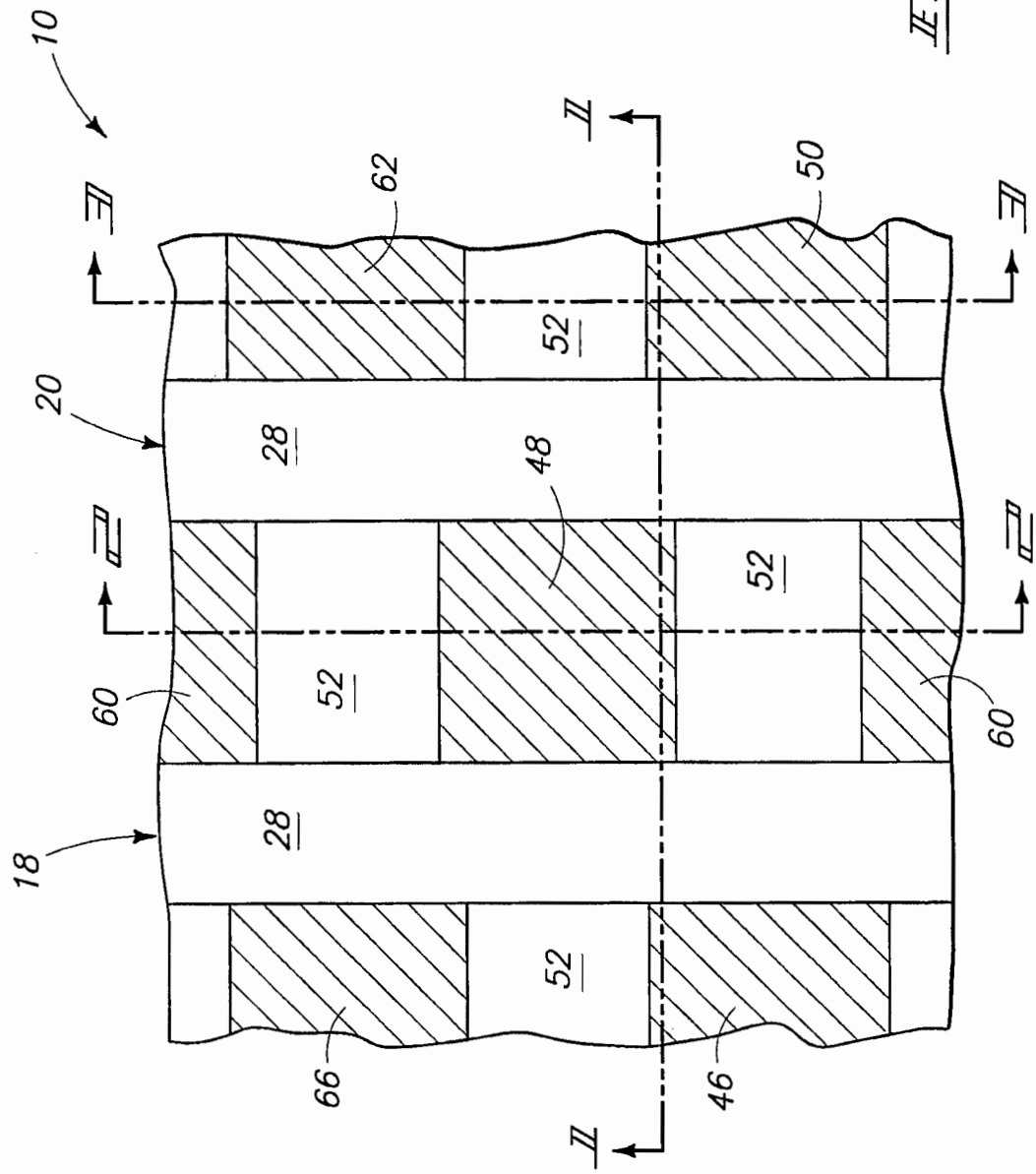

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FIG. 3

Fig 3E



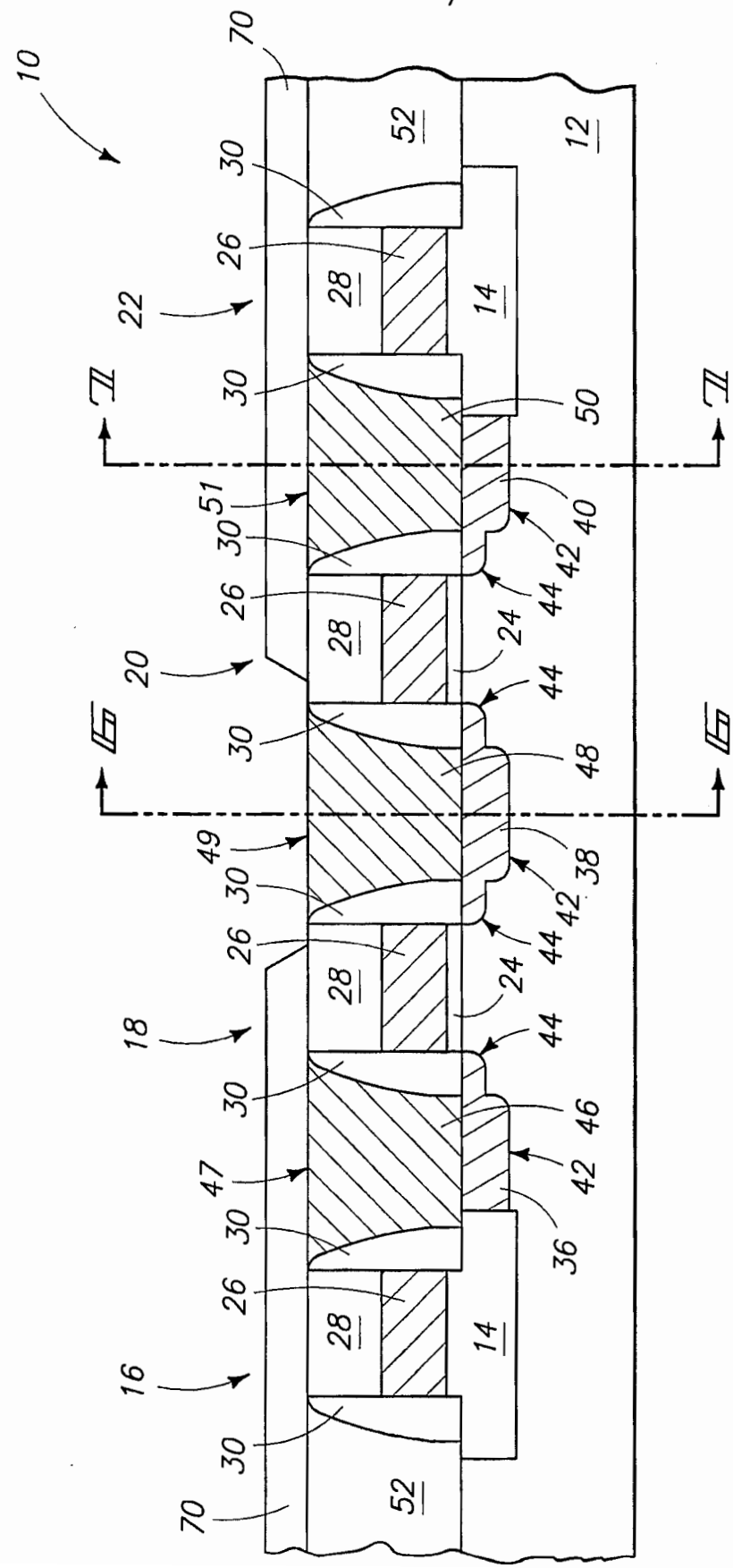

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FIG. 5

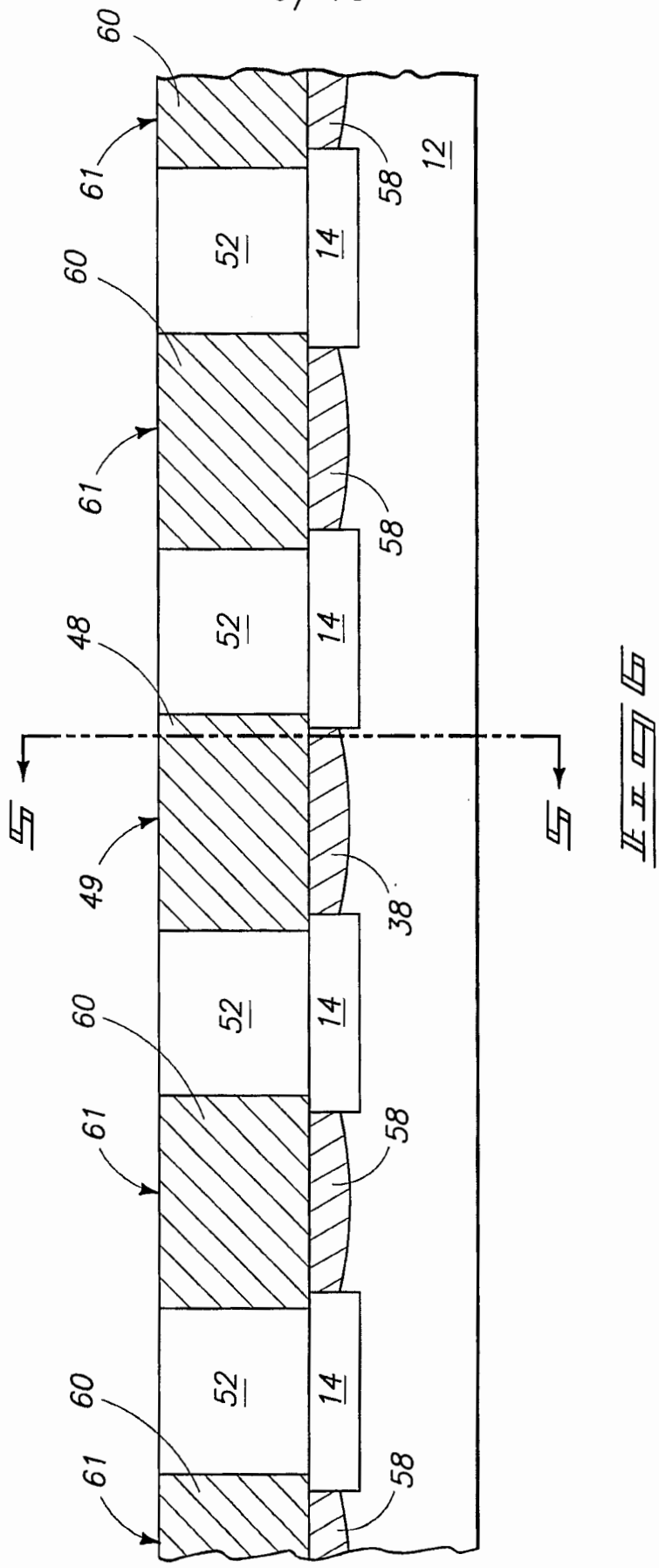

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FIG 5

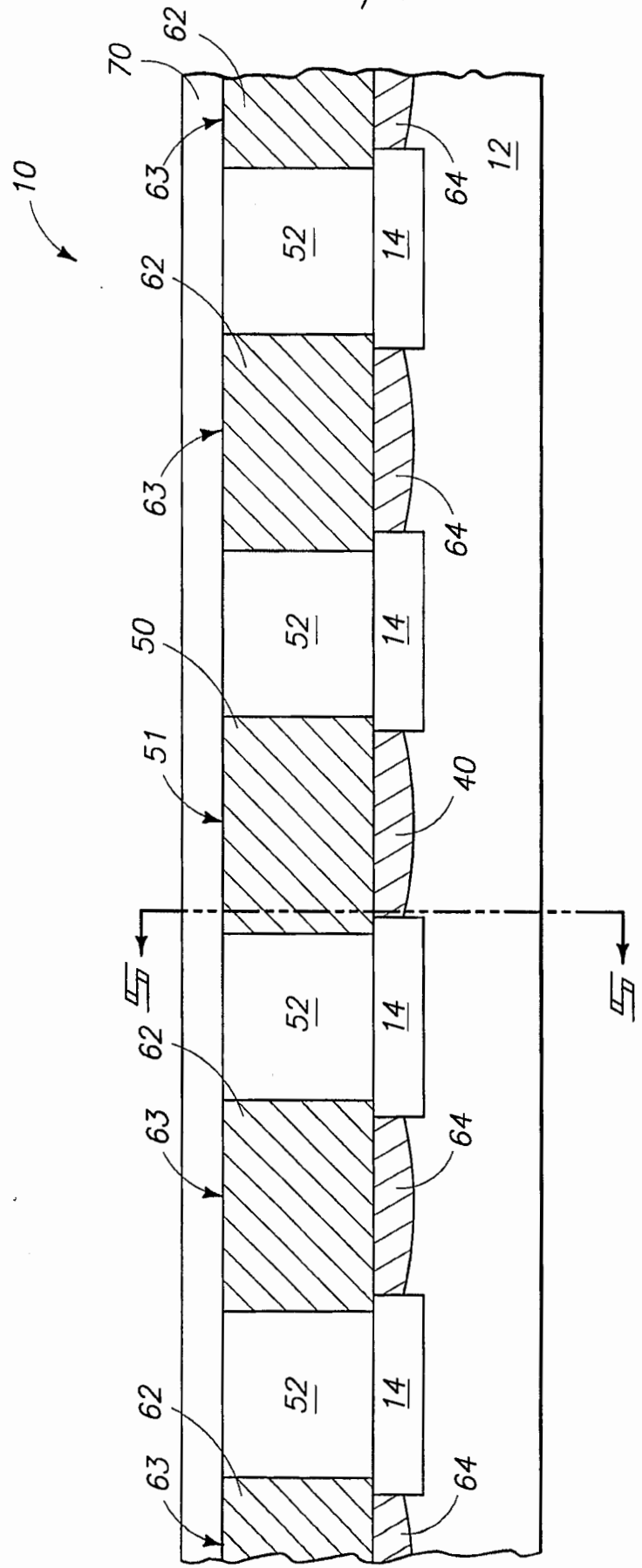


FIG. 7

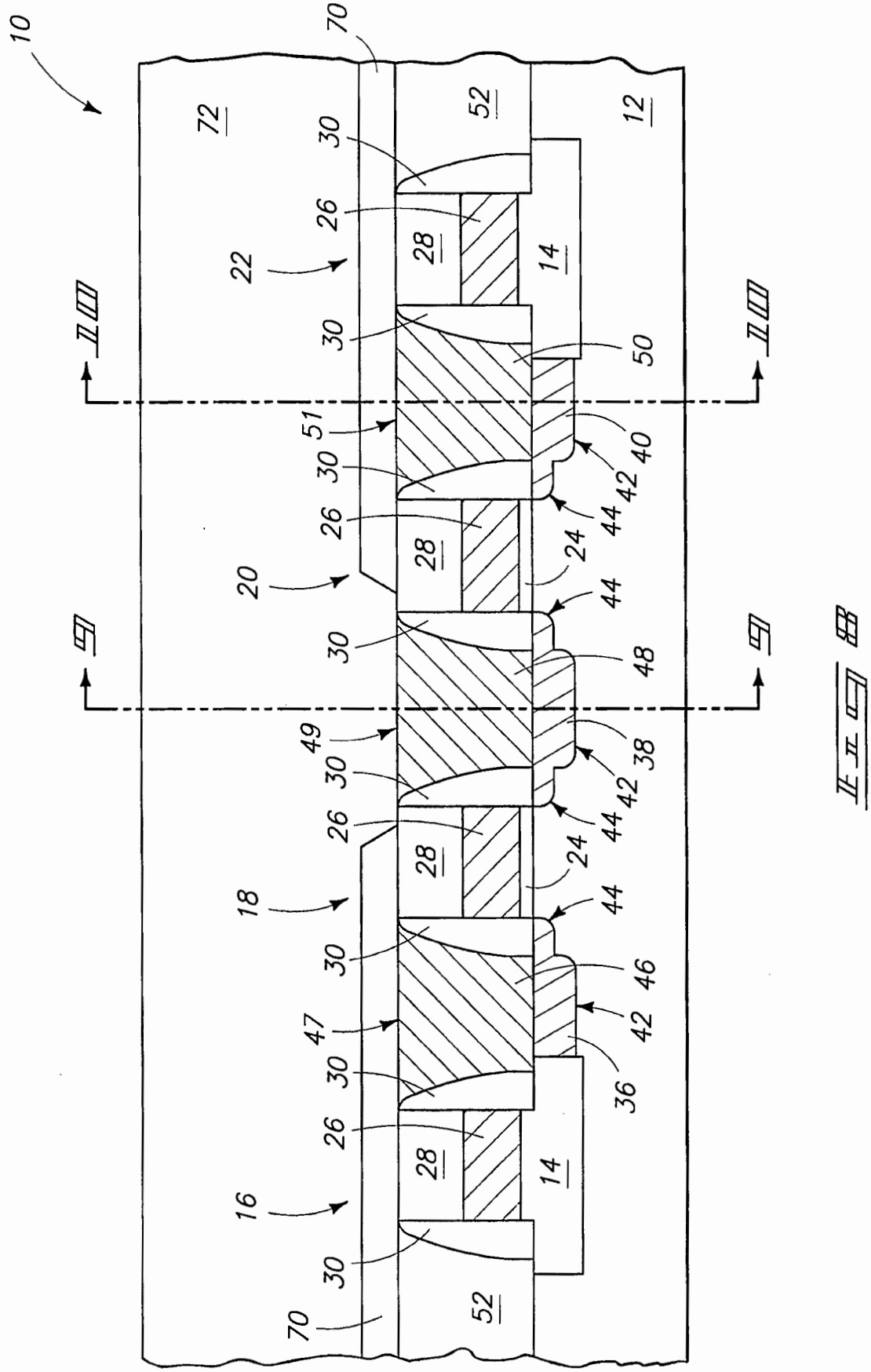

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FIG. 8B

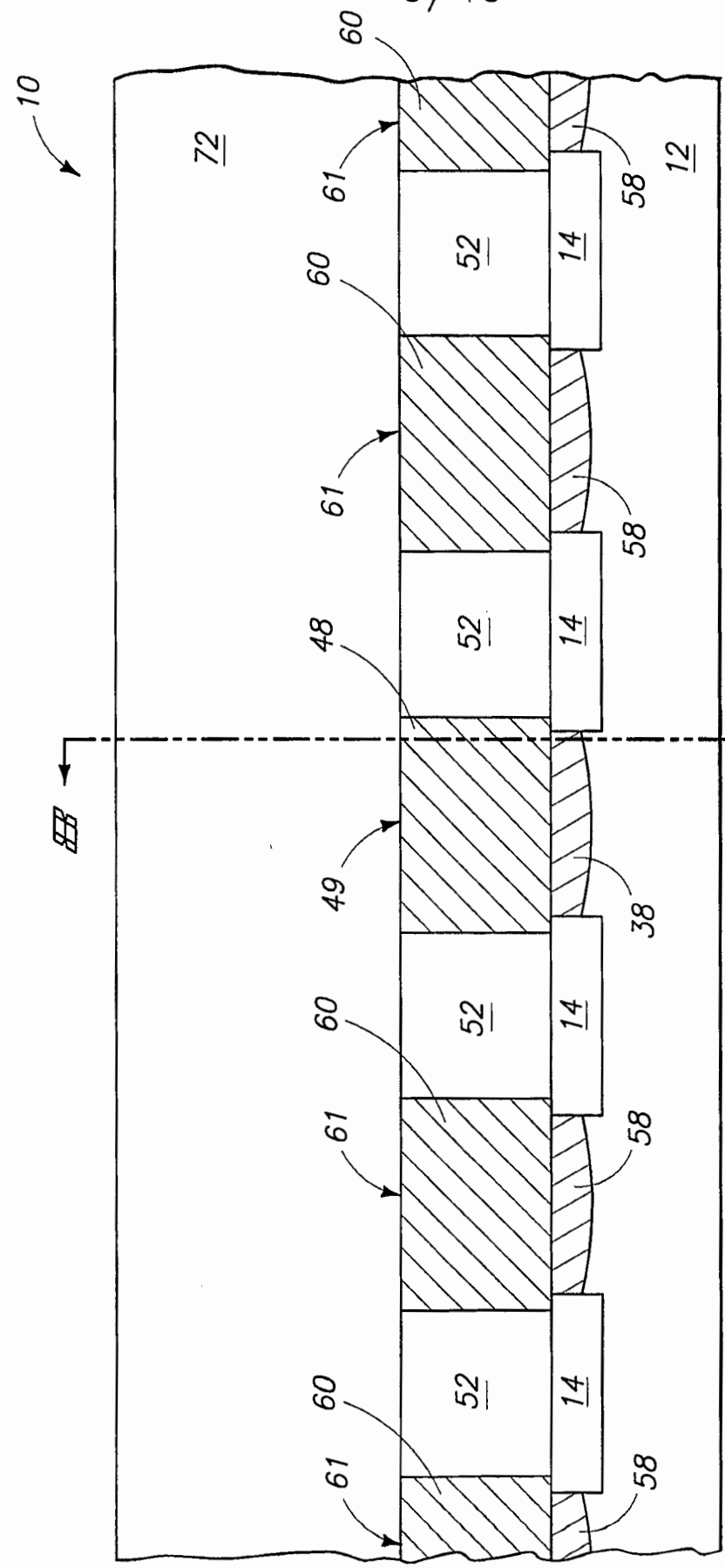


FIG 5

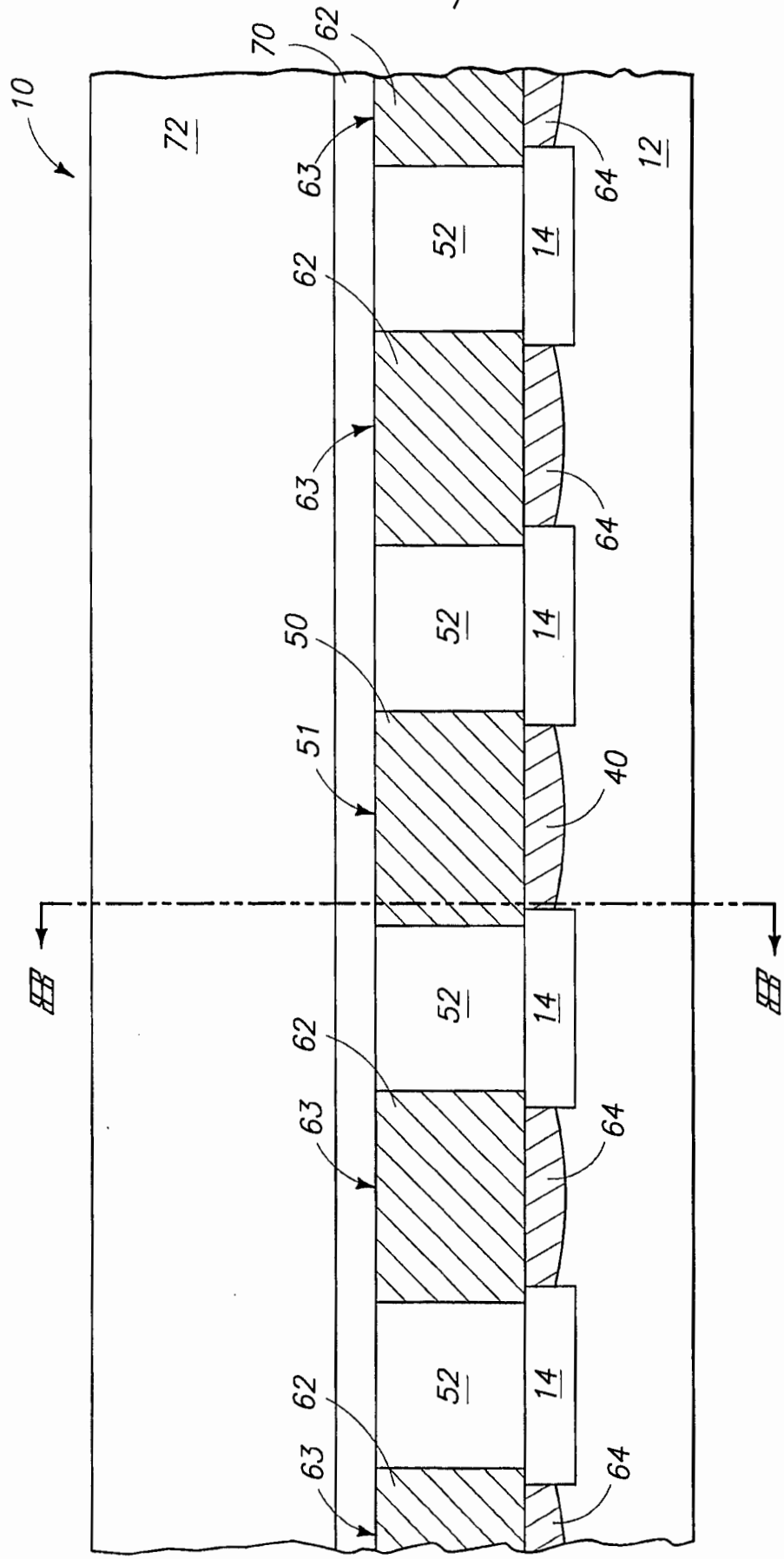
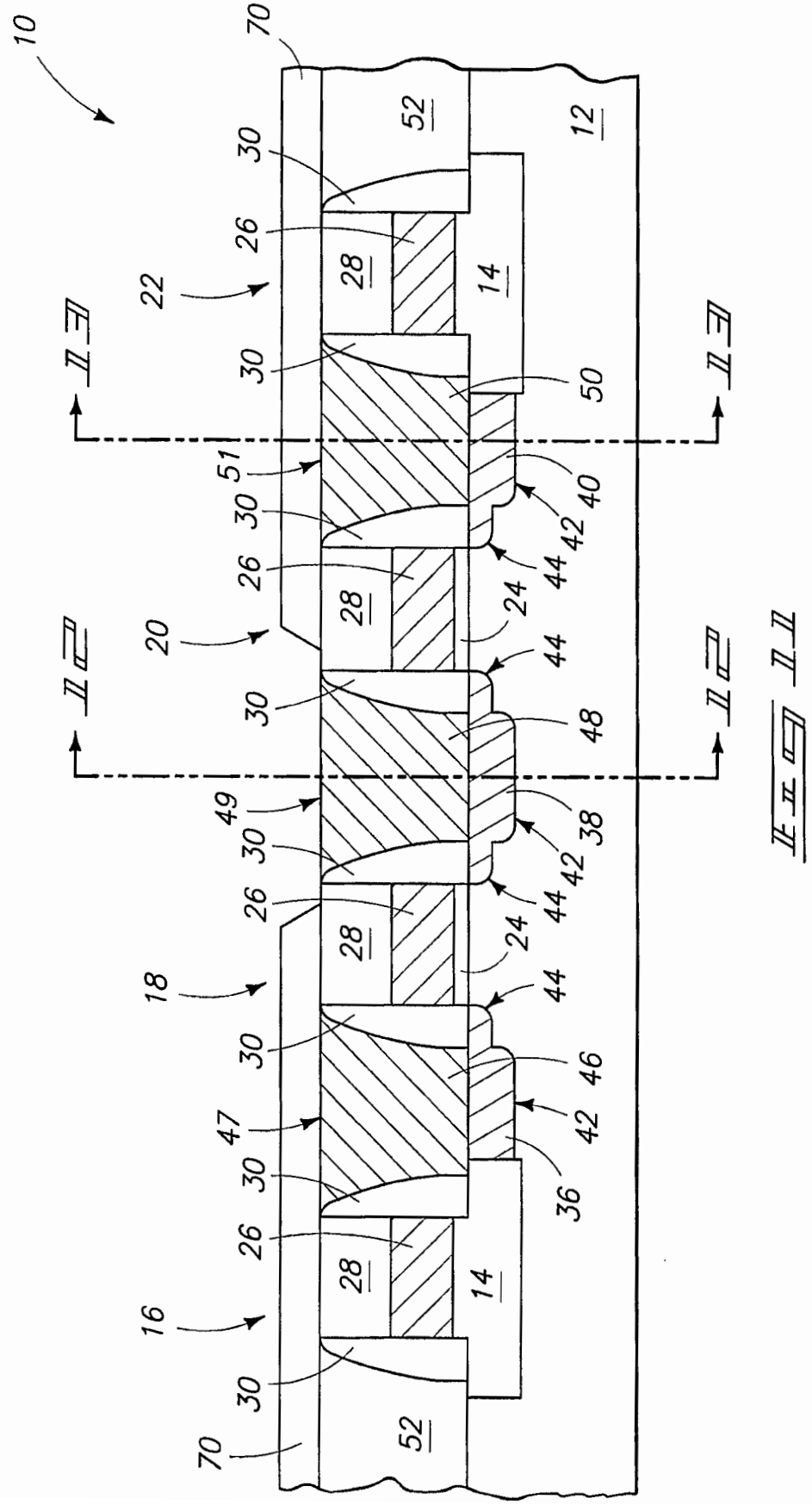

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FIG 11


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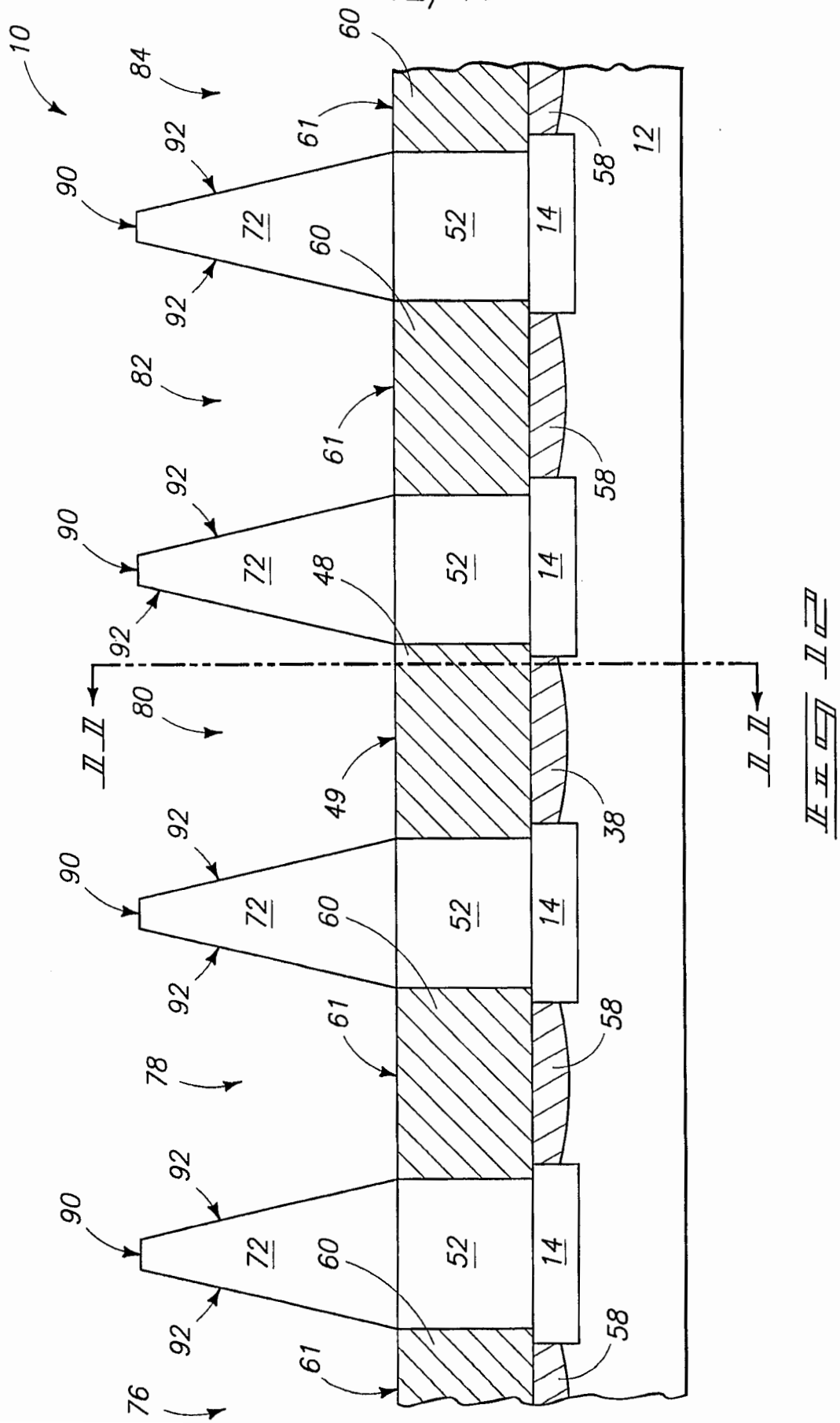


FIG. II

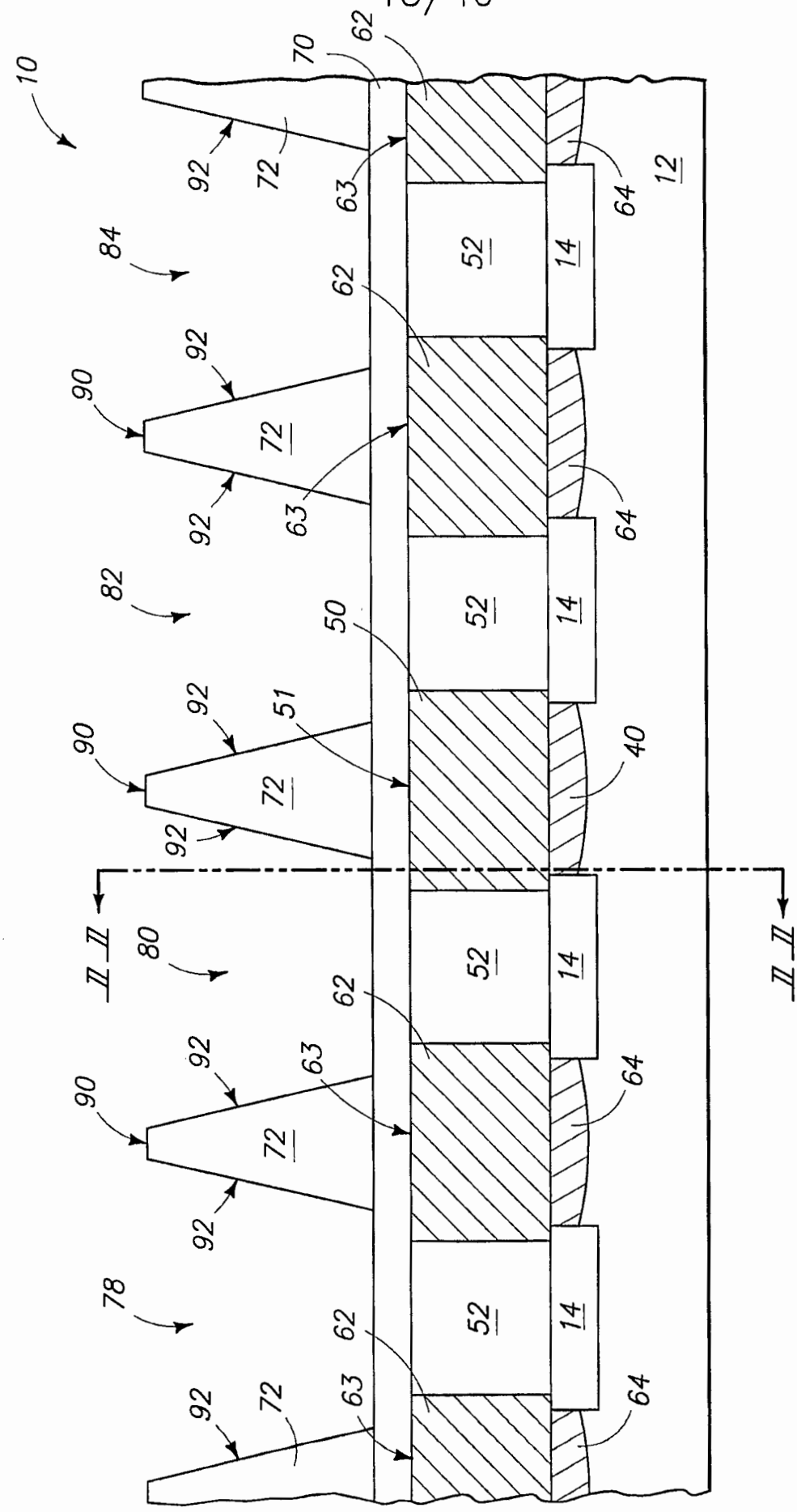


FIG. II

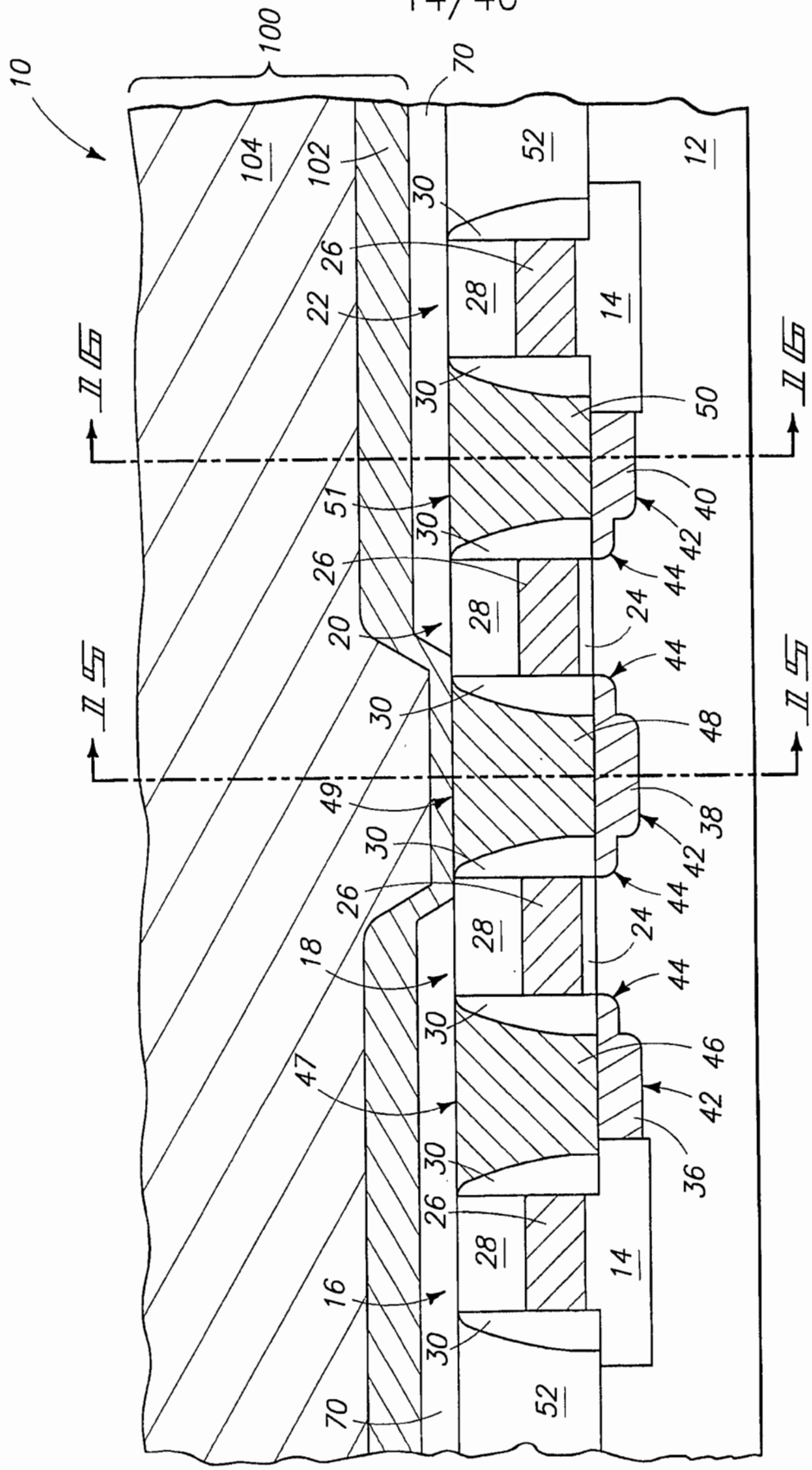

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FIG II

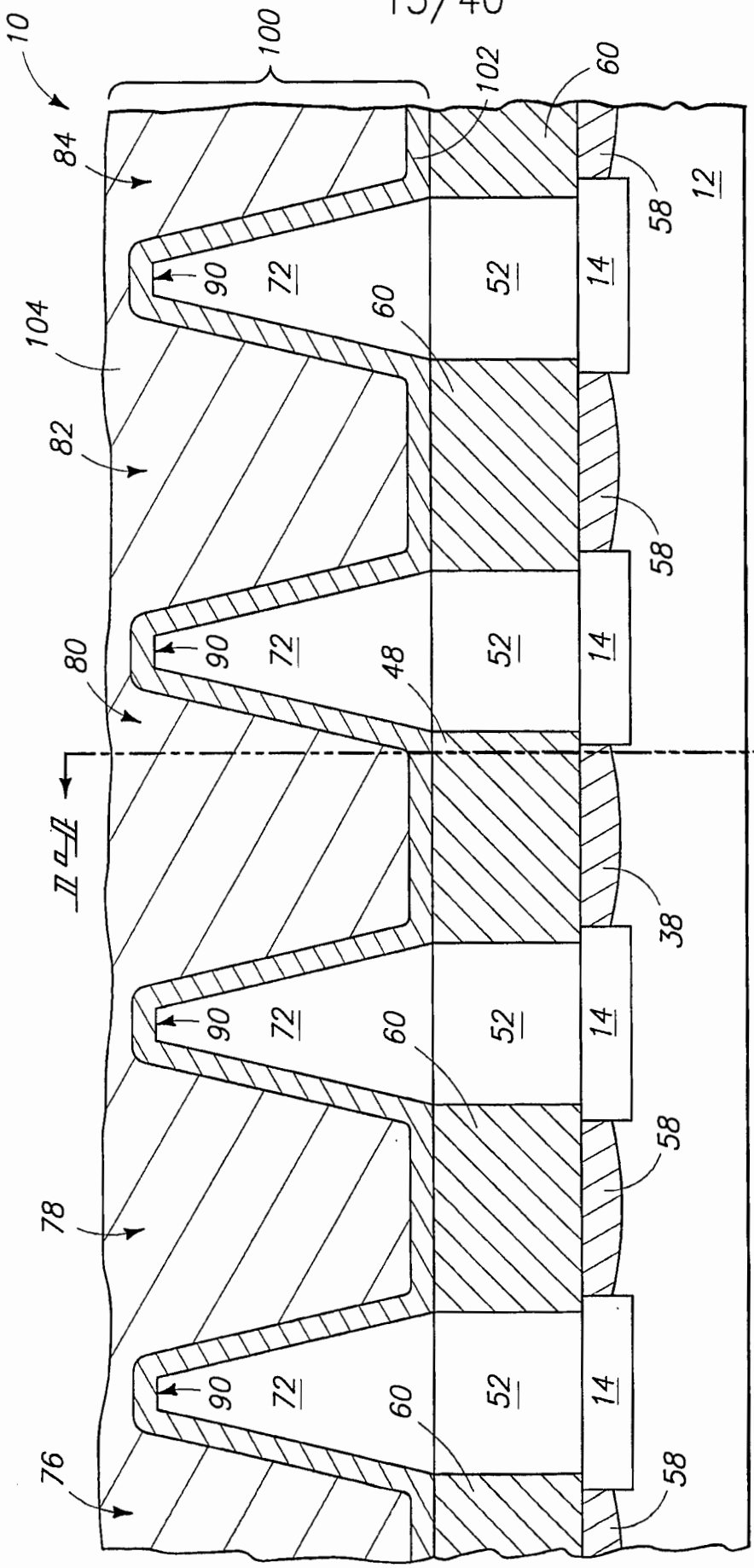


FIG 5

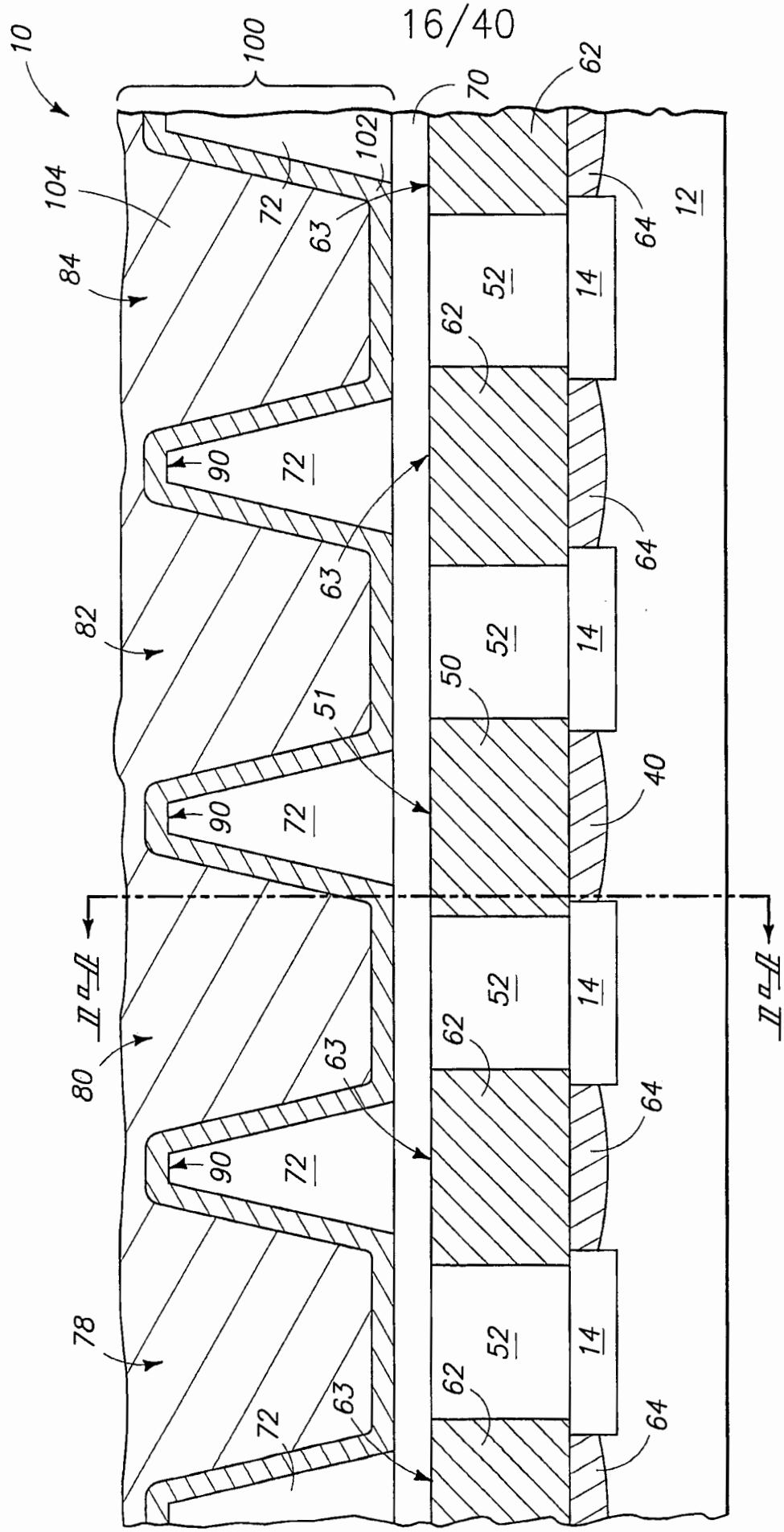

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FIG. 1B

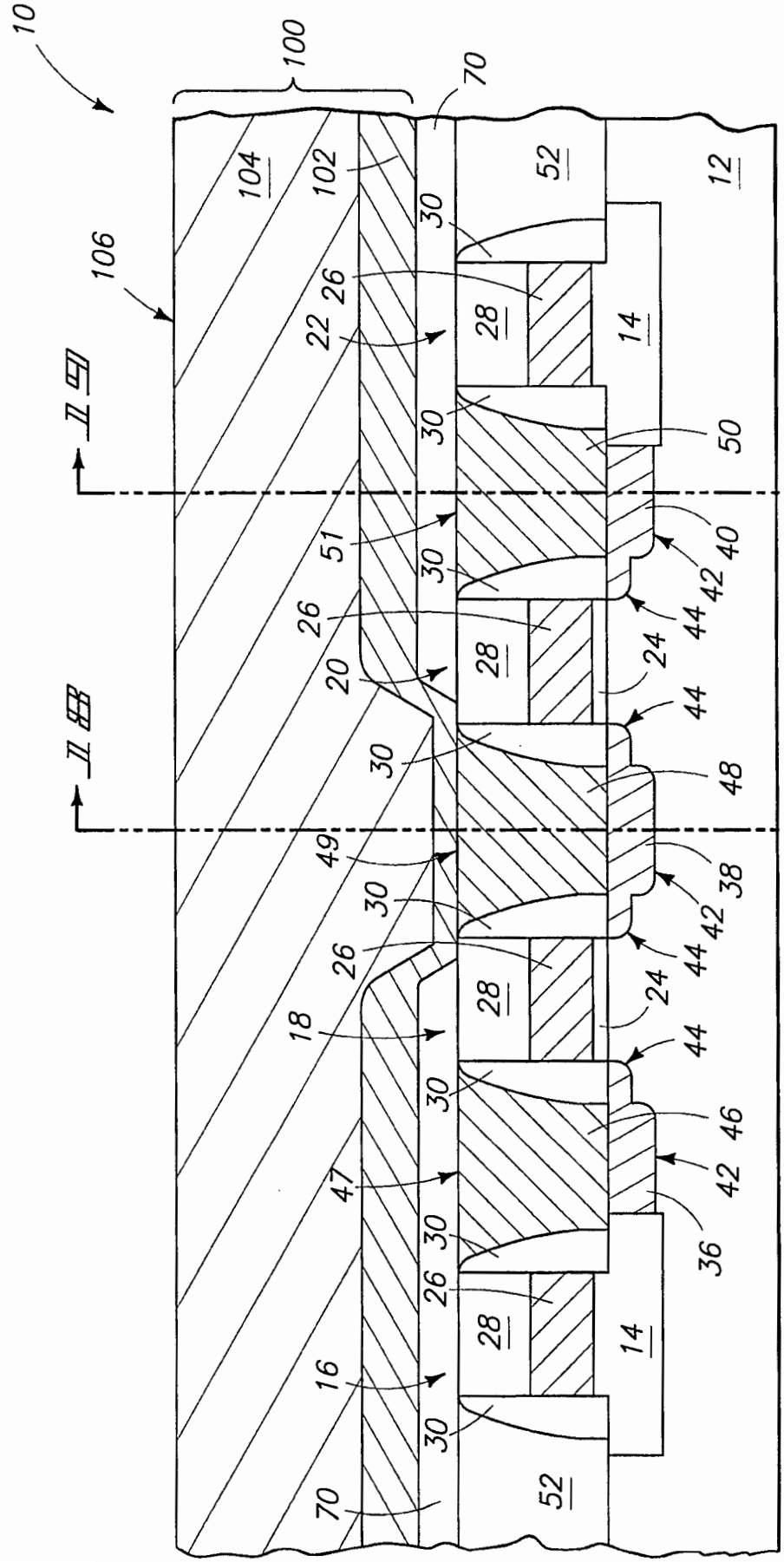

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FIG. 17

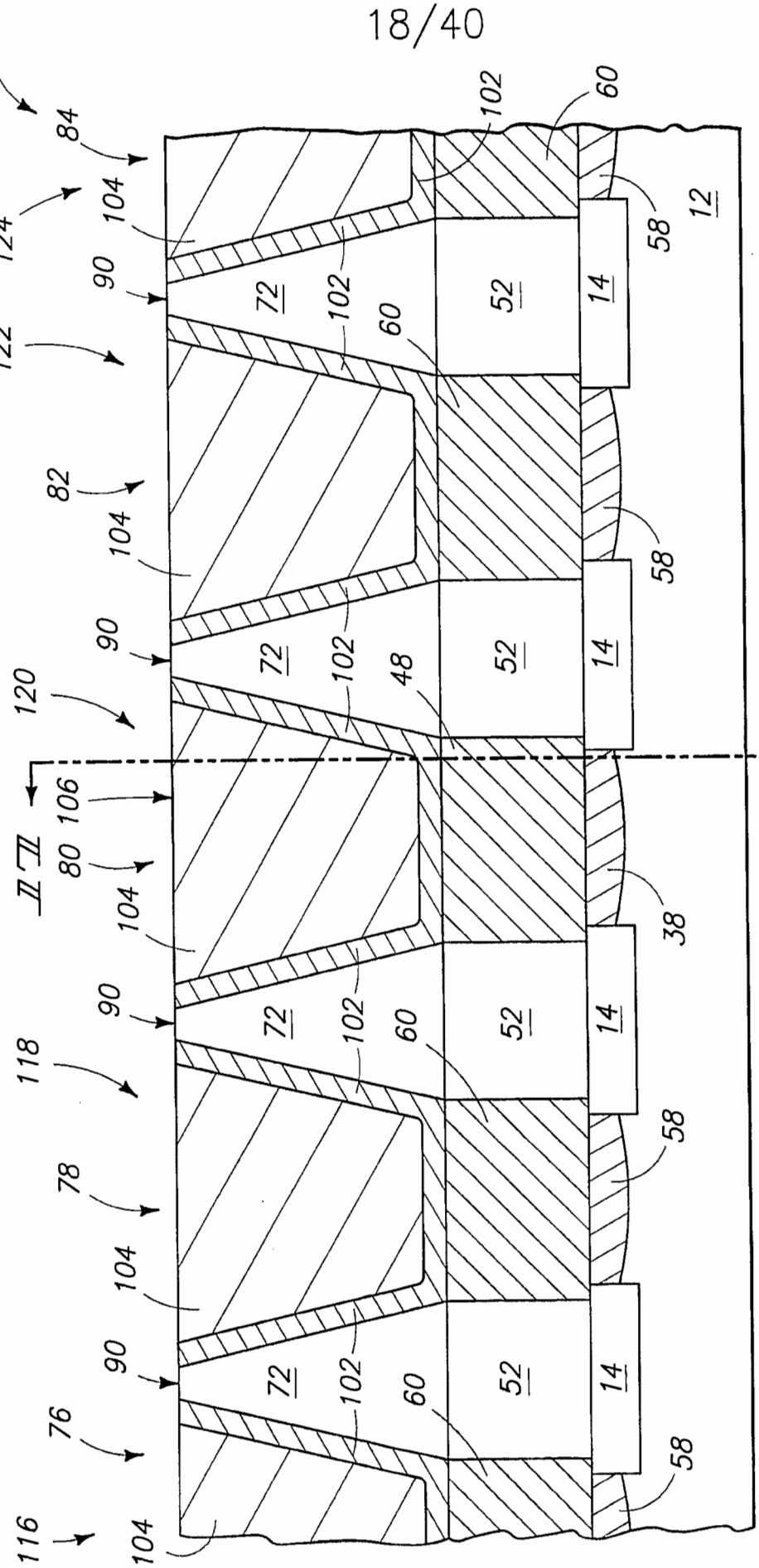

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FIG. 11

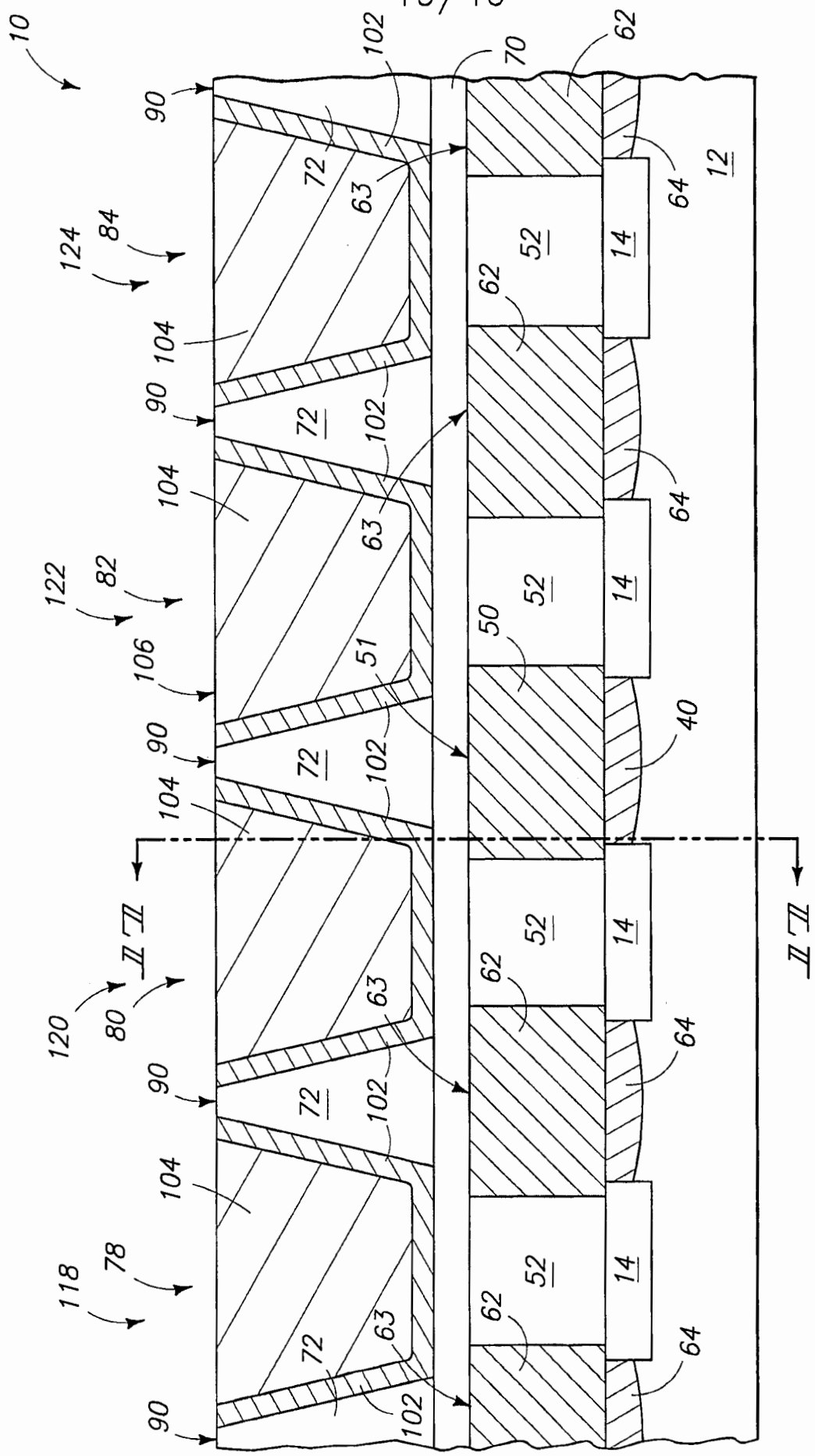

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FIG 5A

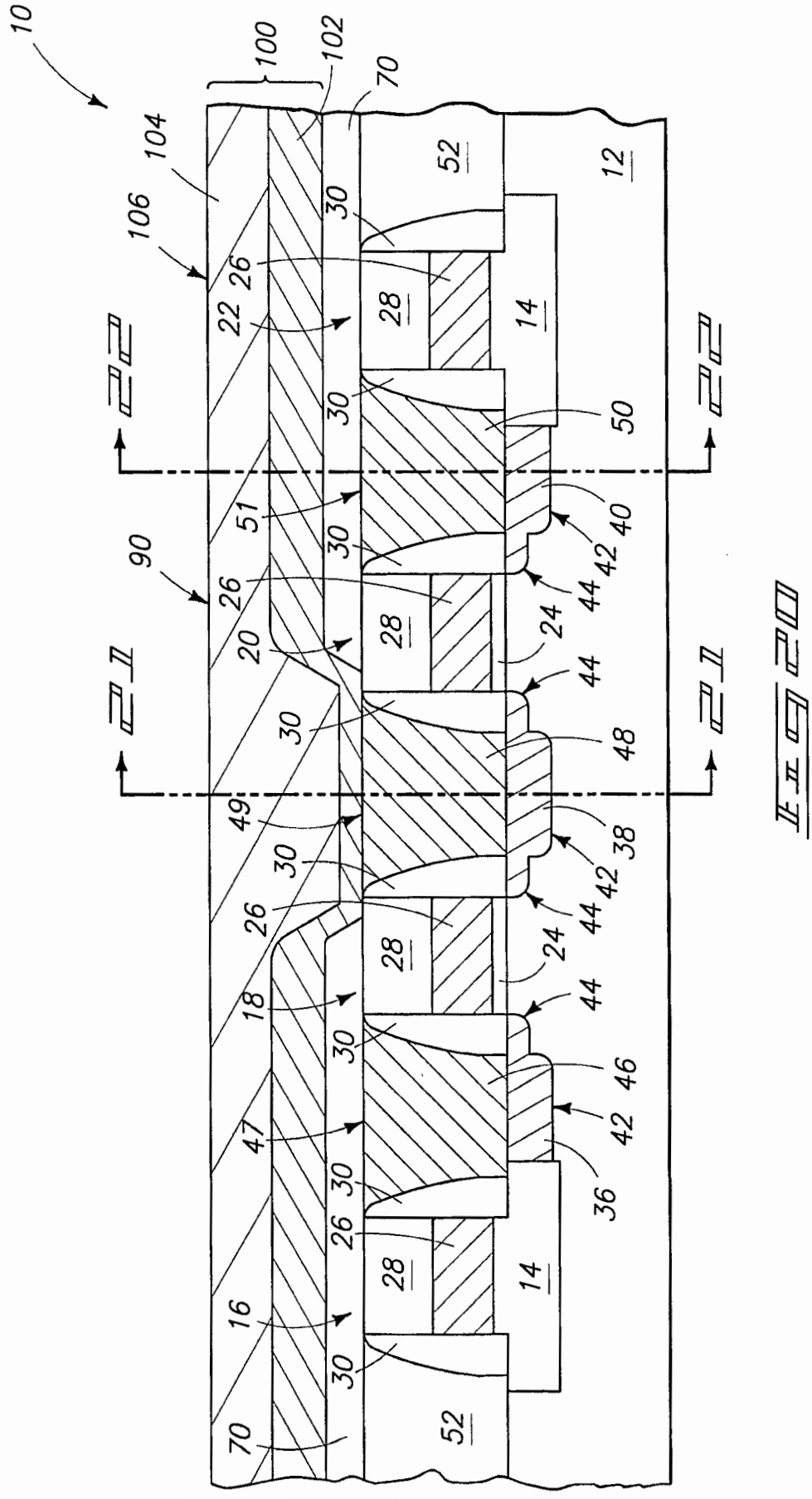

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FIG 2B

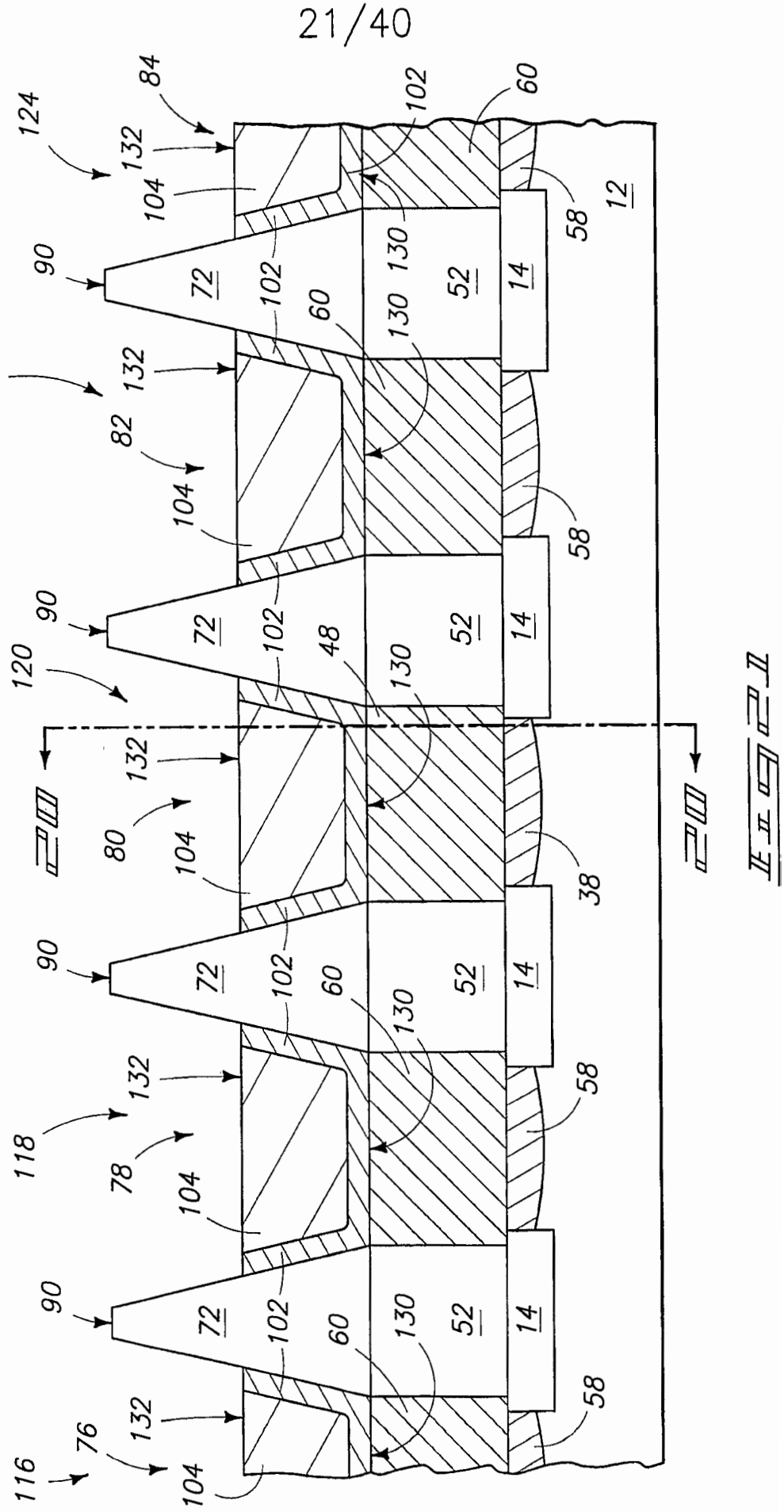

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FIG 5H

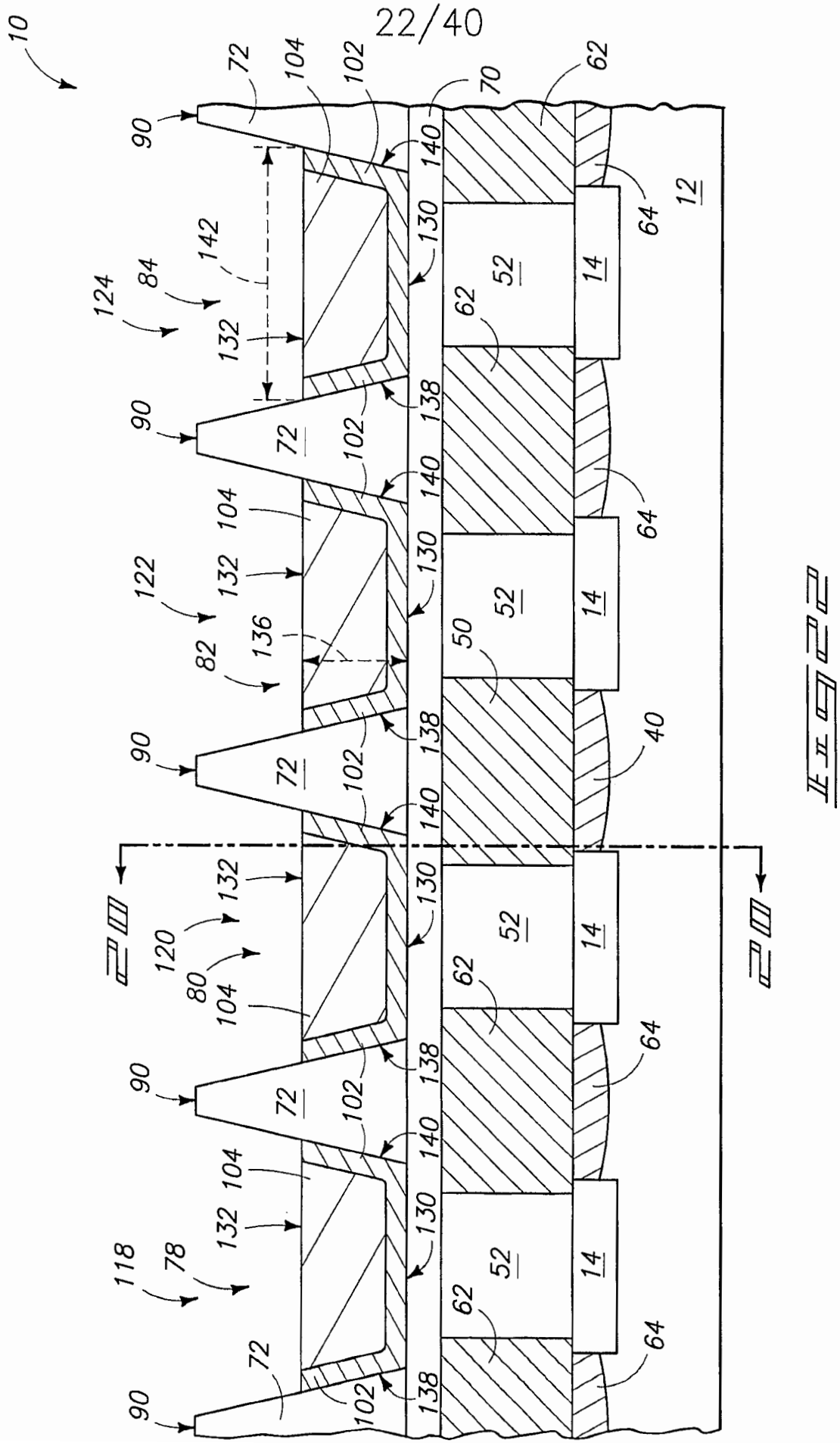

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FIG 22

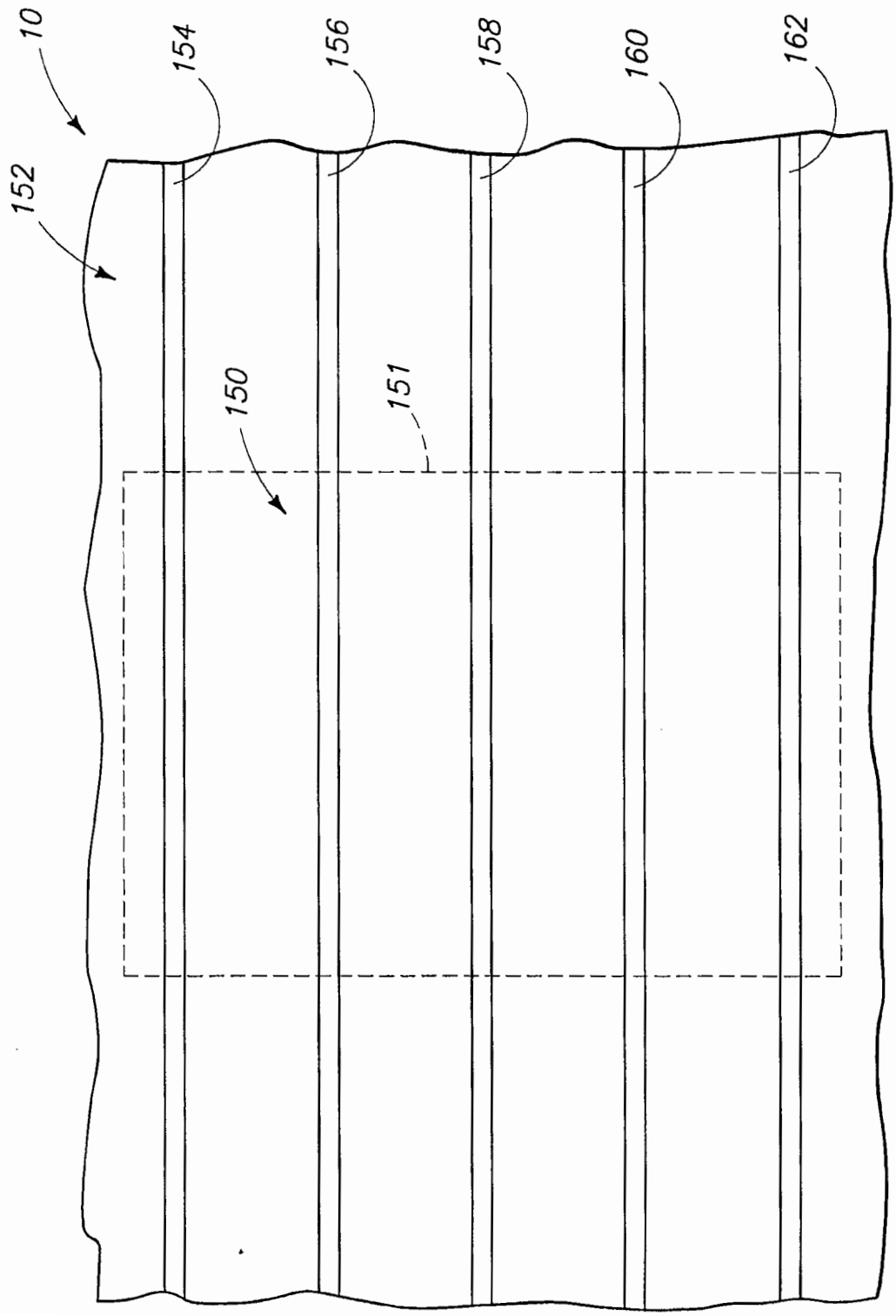


FIG 23

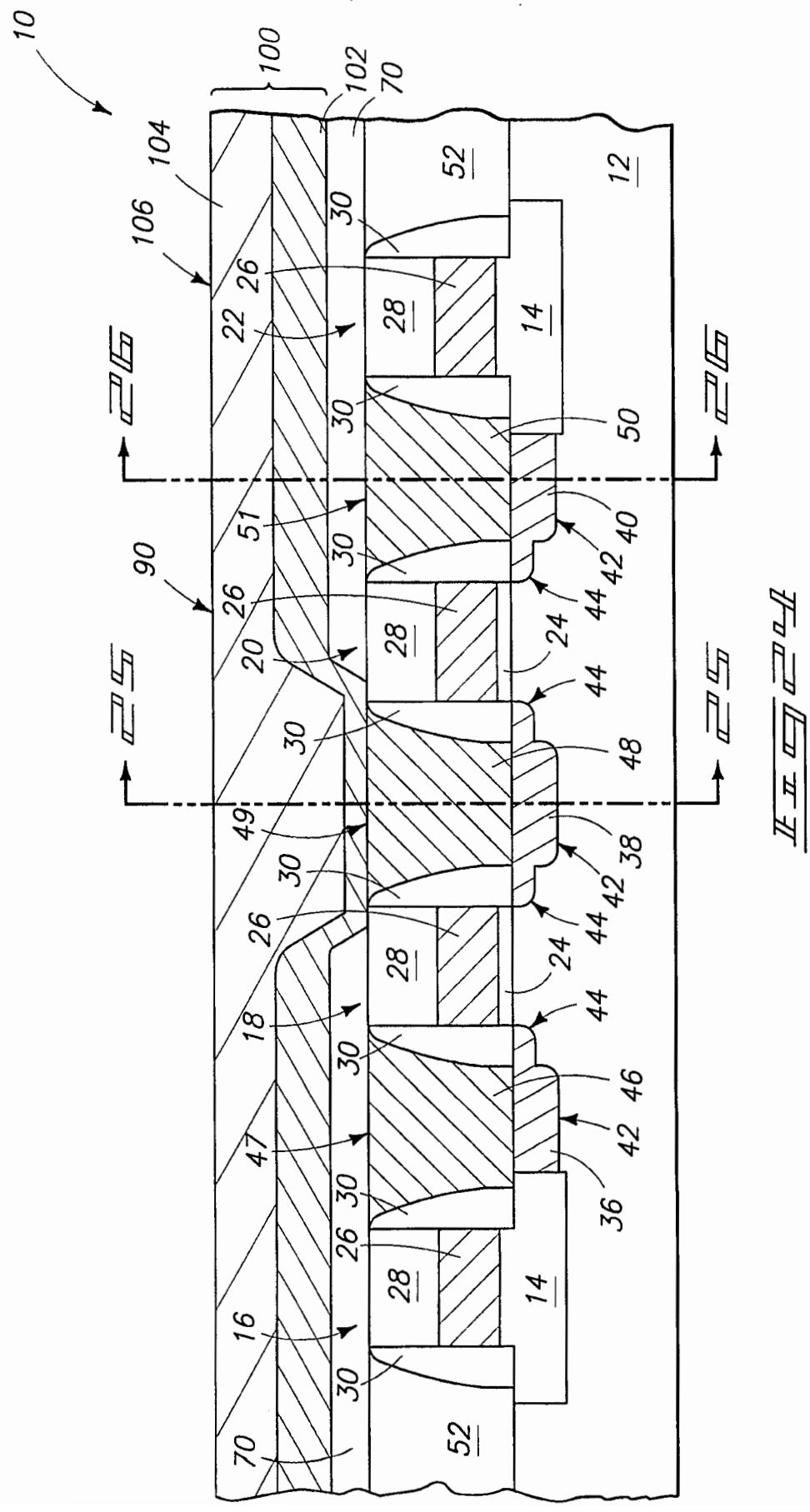

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FIG 2B-2S

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FIG 25

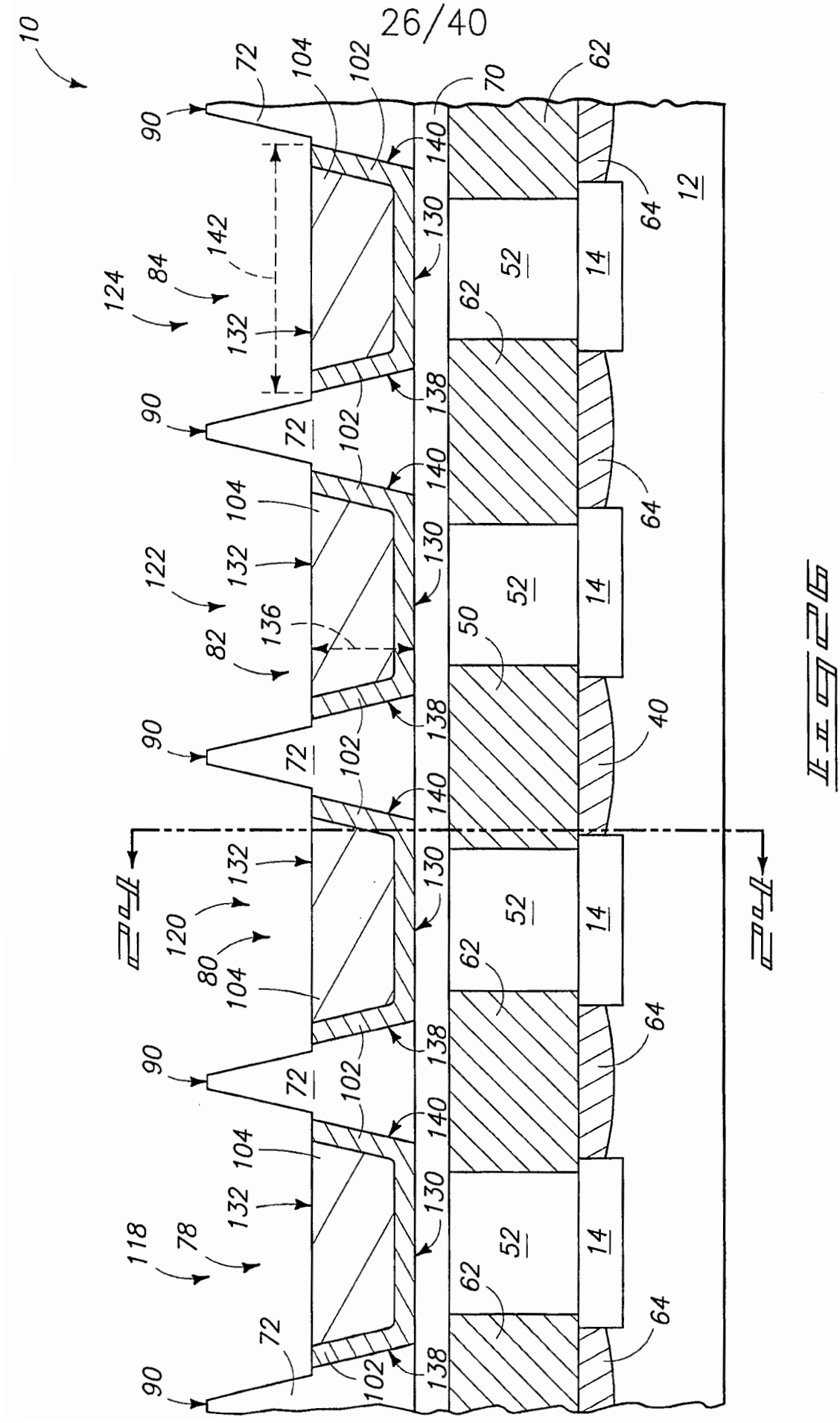

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FIG 2E

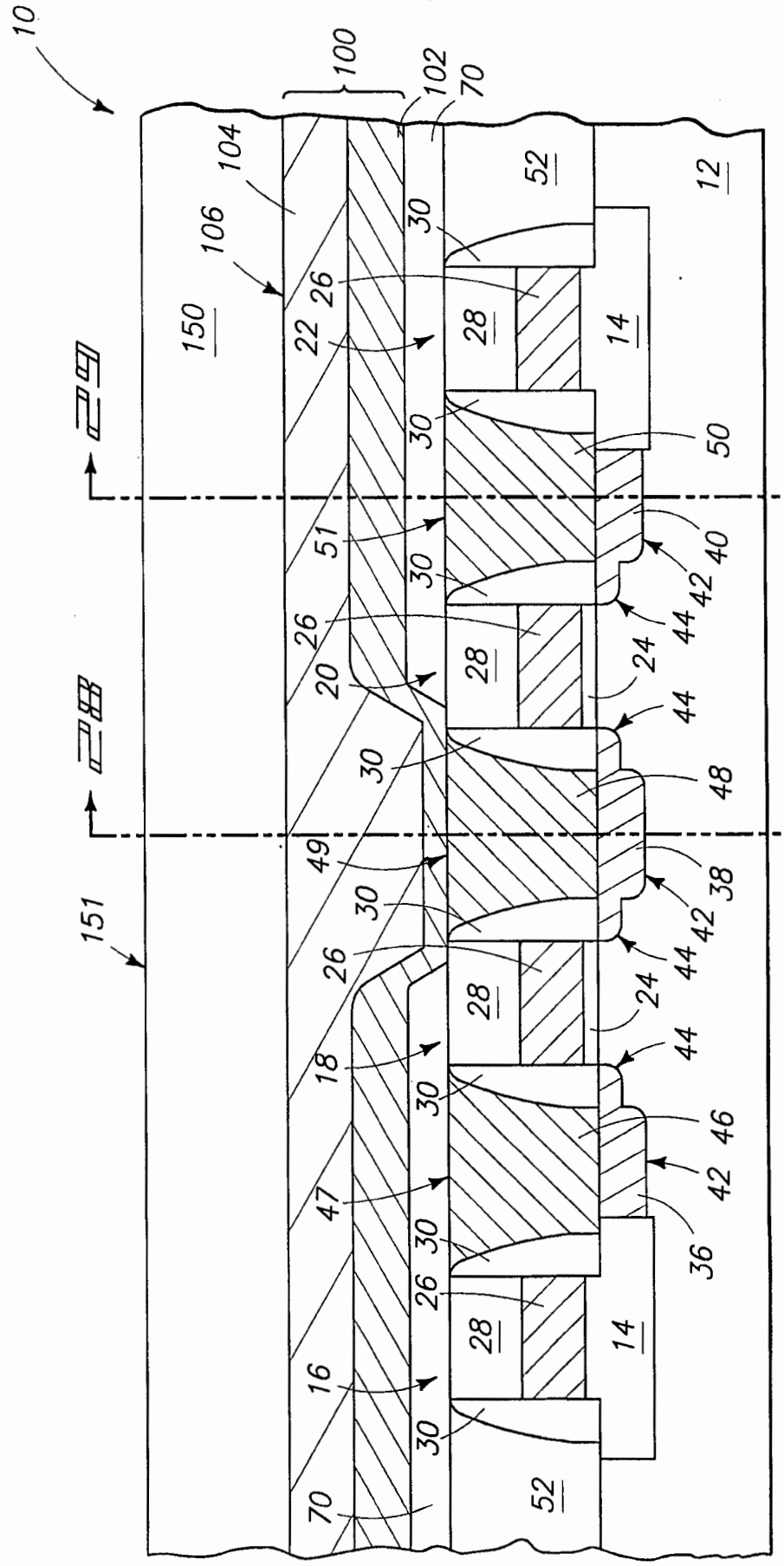

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FIG 27

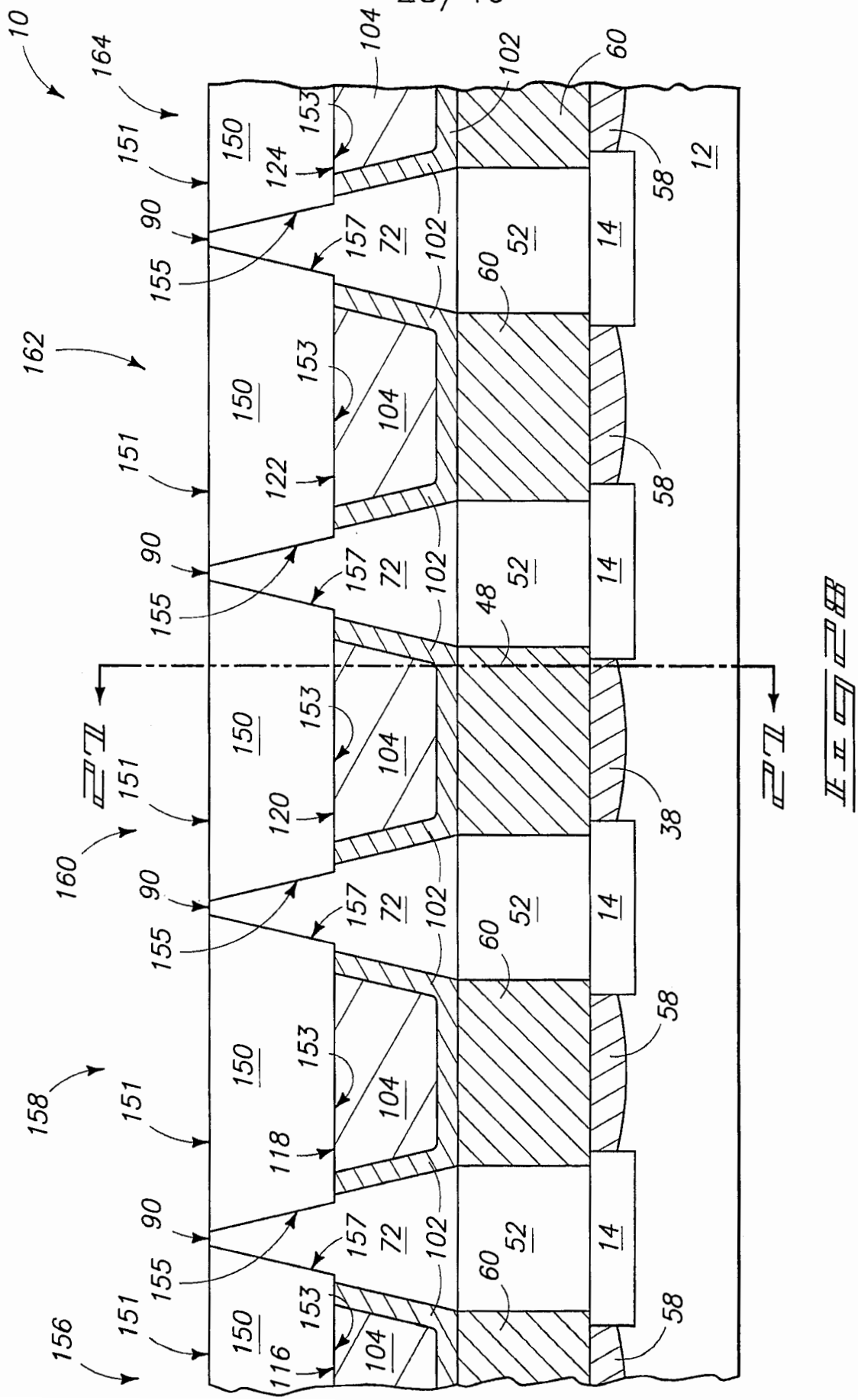

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FIG 28

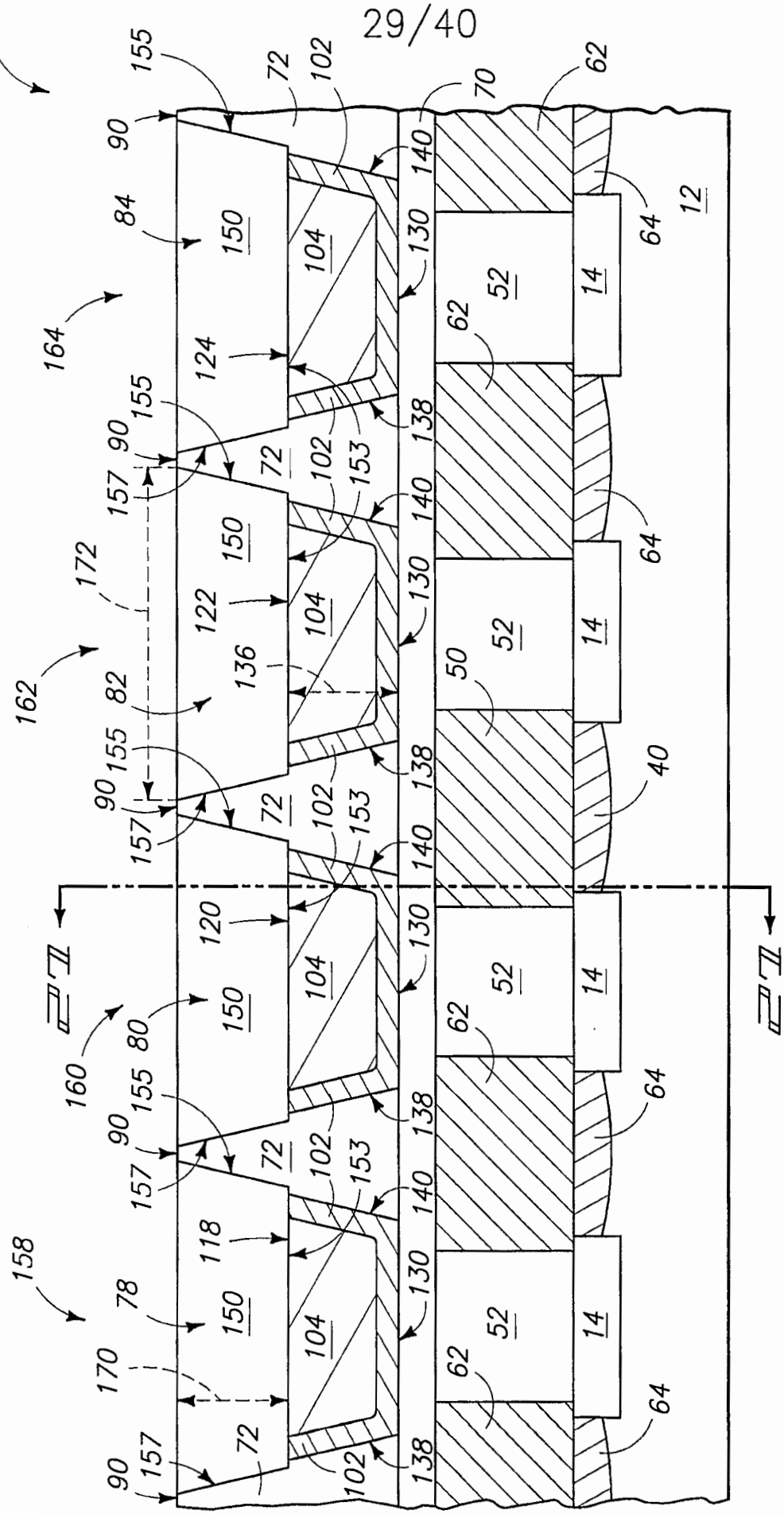
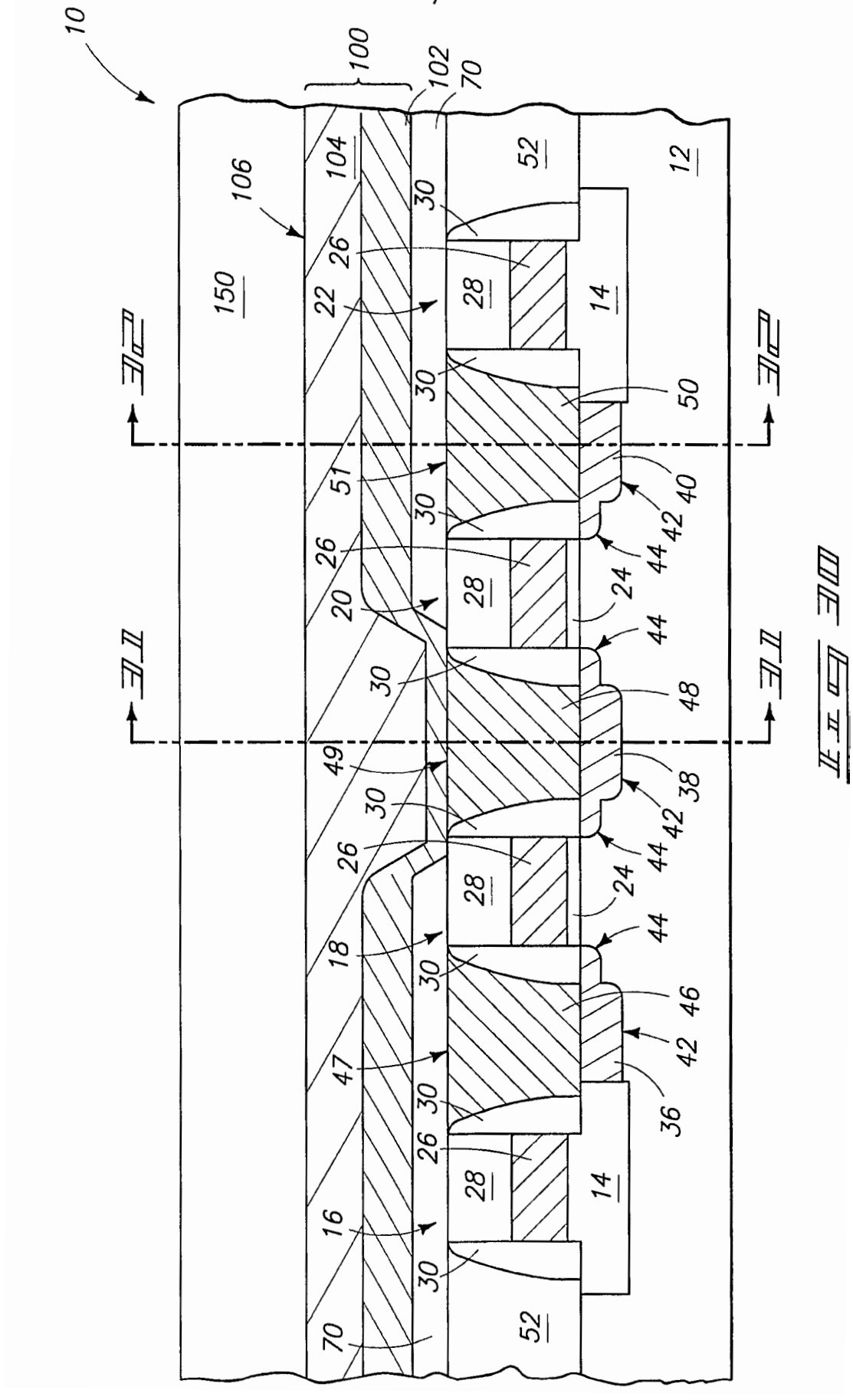

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FIG 59


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FIG. 30

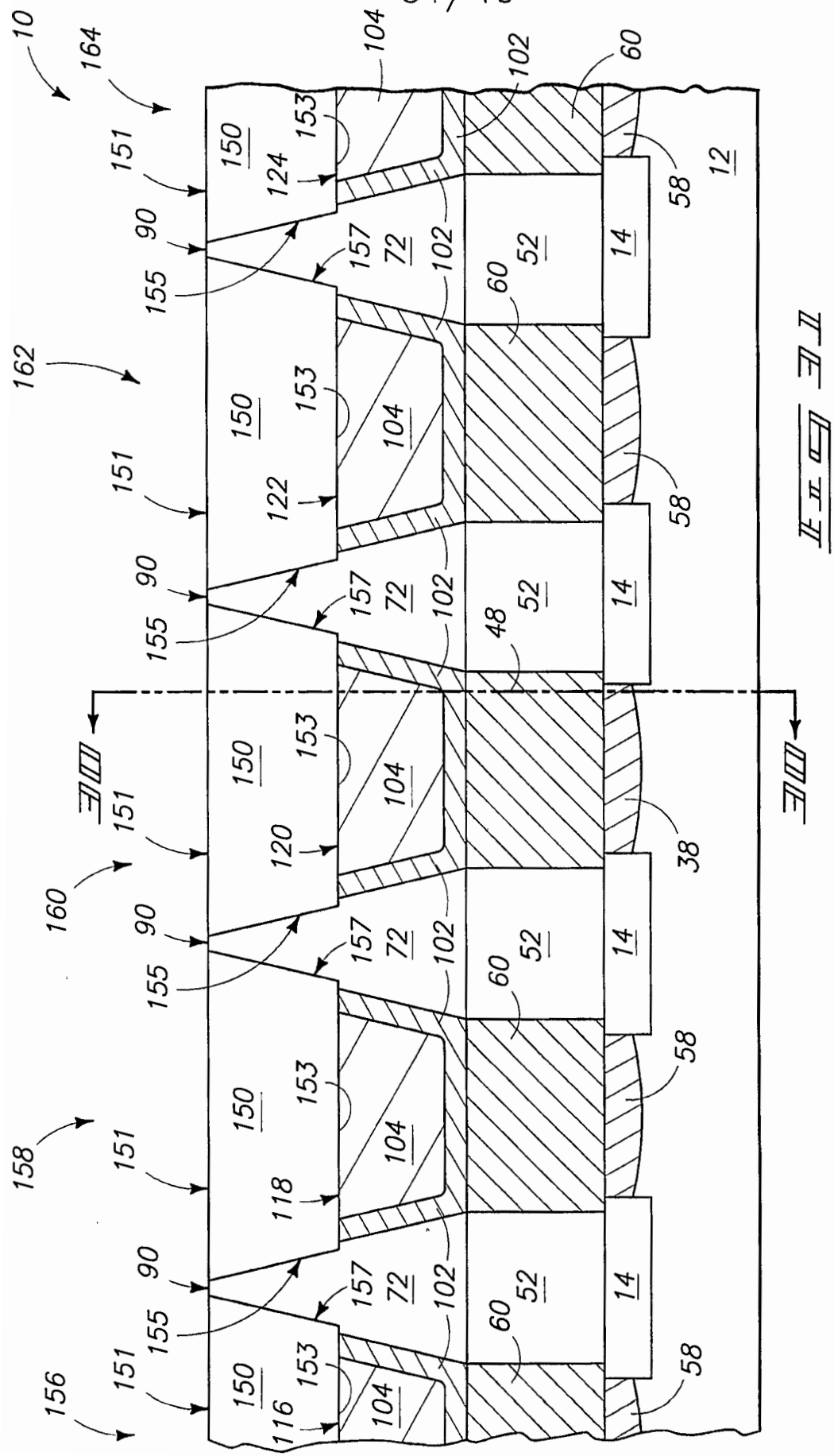
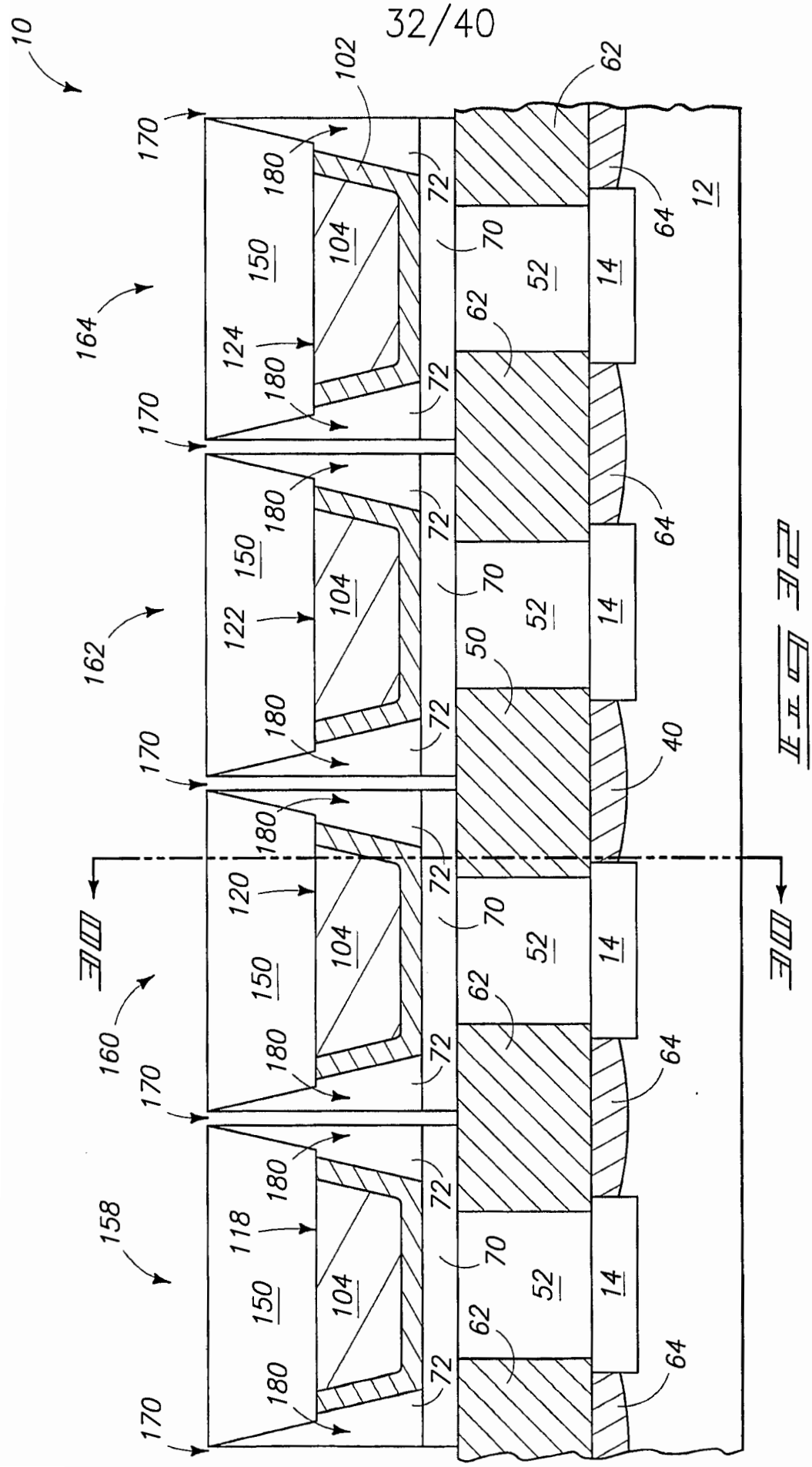
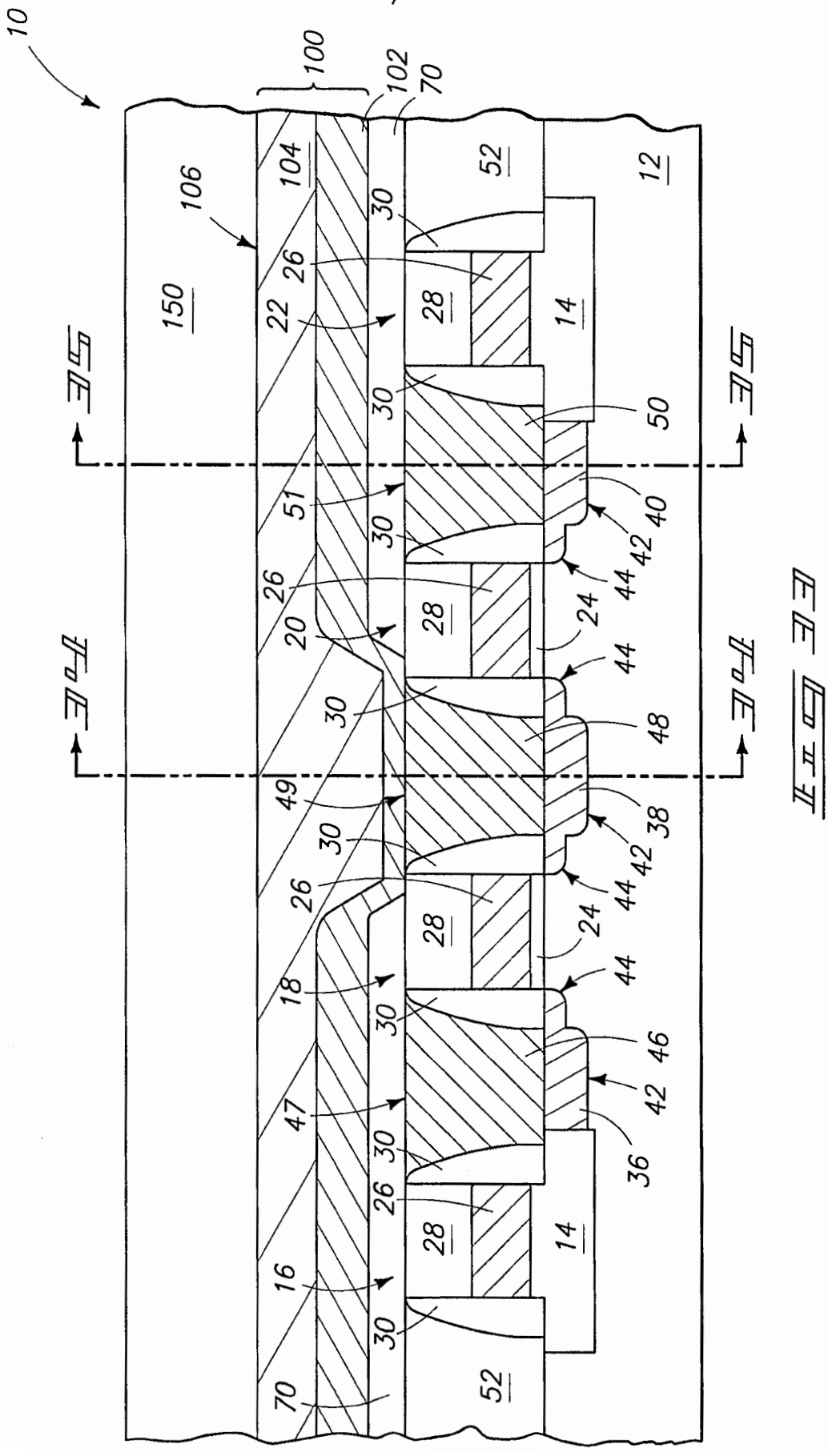

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FIG. 11


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FIG 3A
FIG 3B
FIG 3C

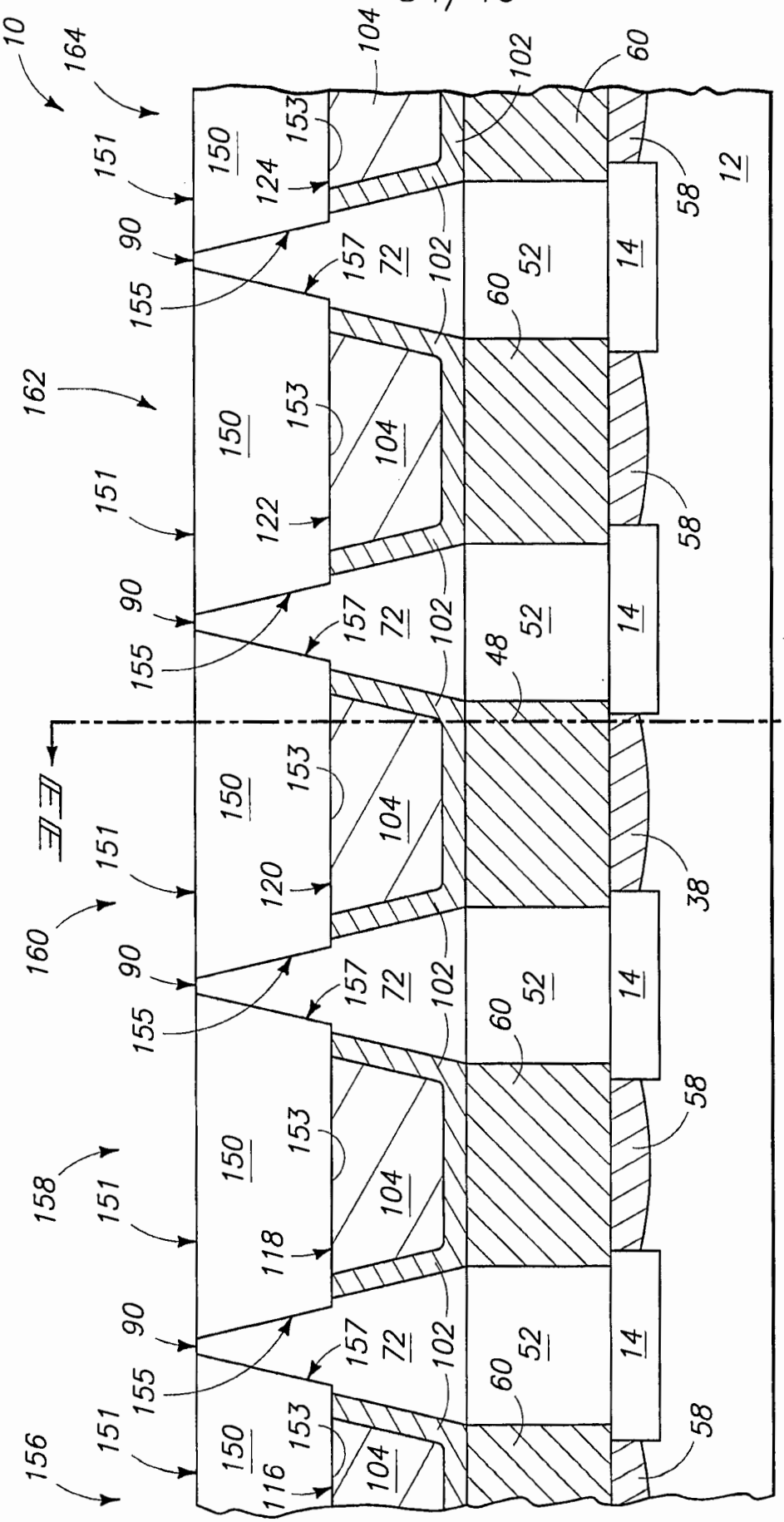

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FIG 11

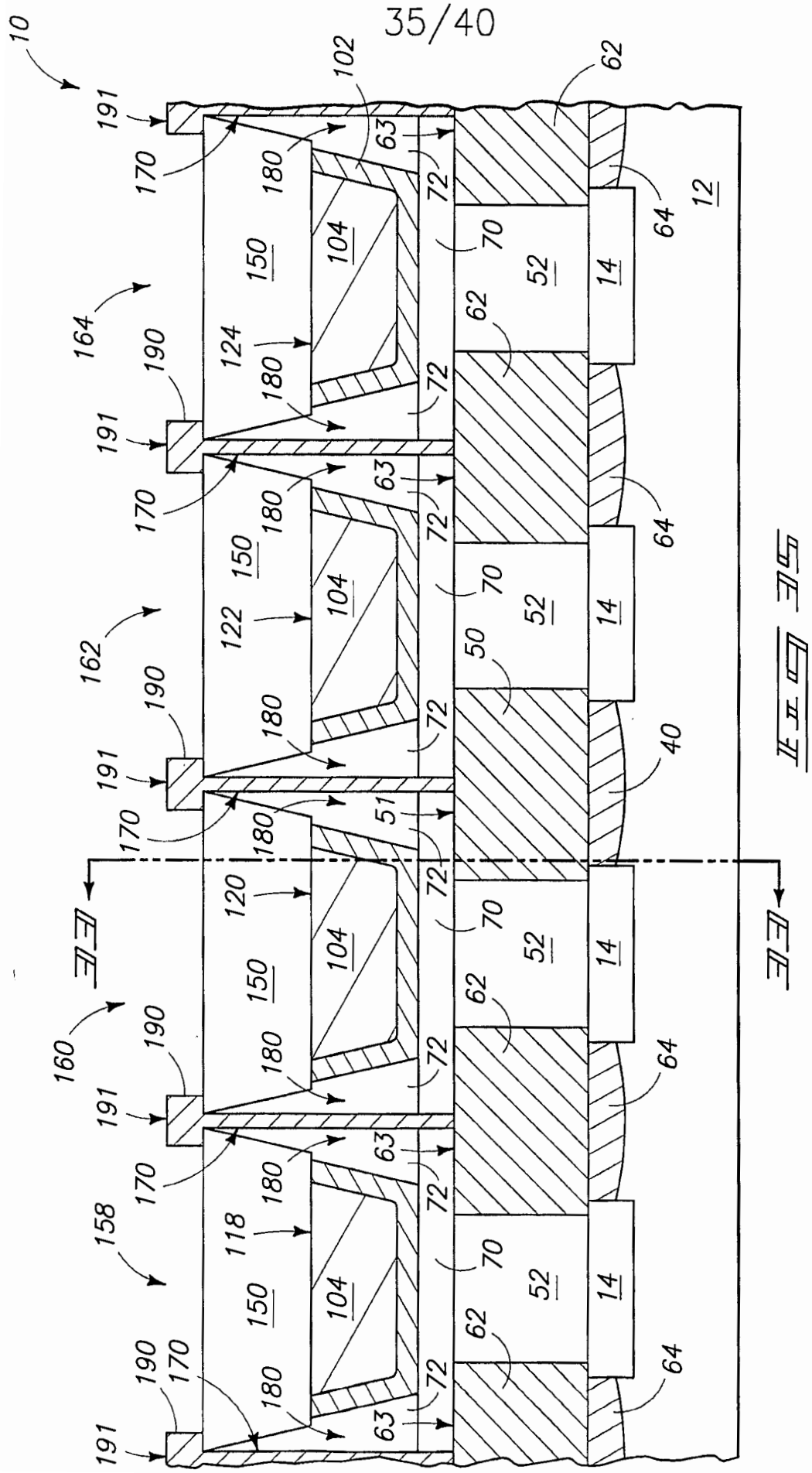

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FIG. 35

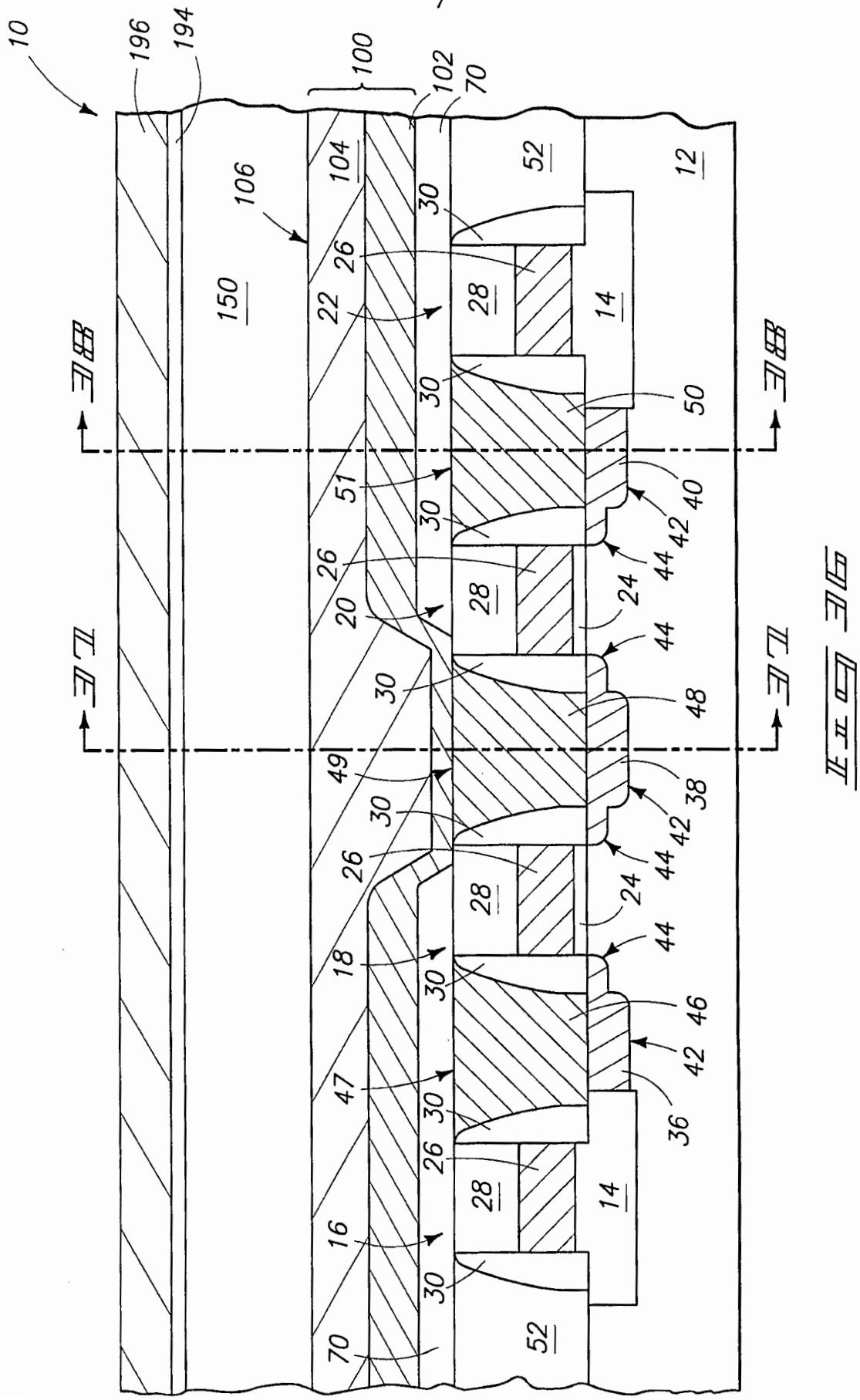

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FIG 36

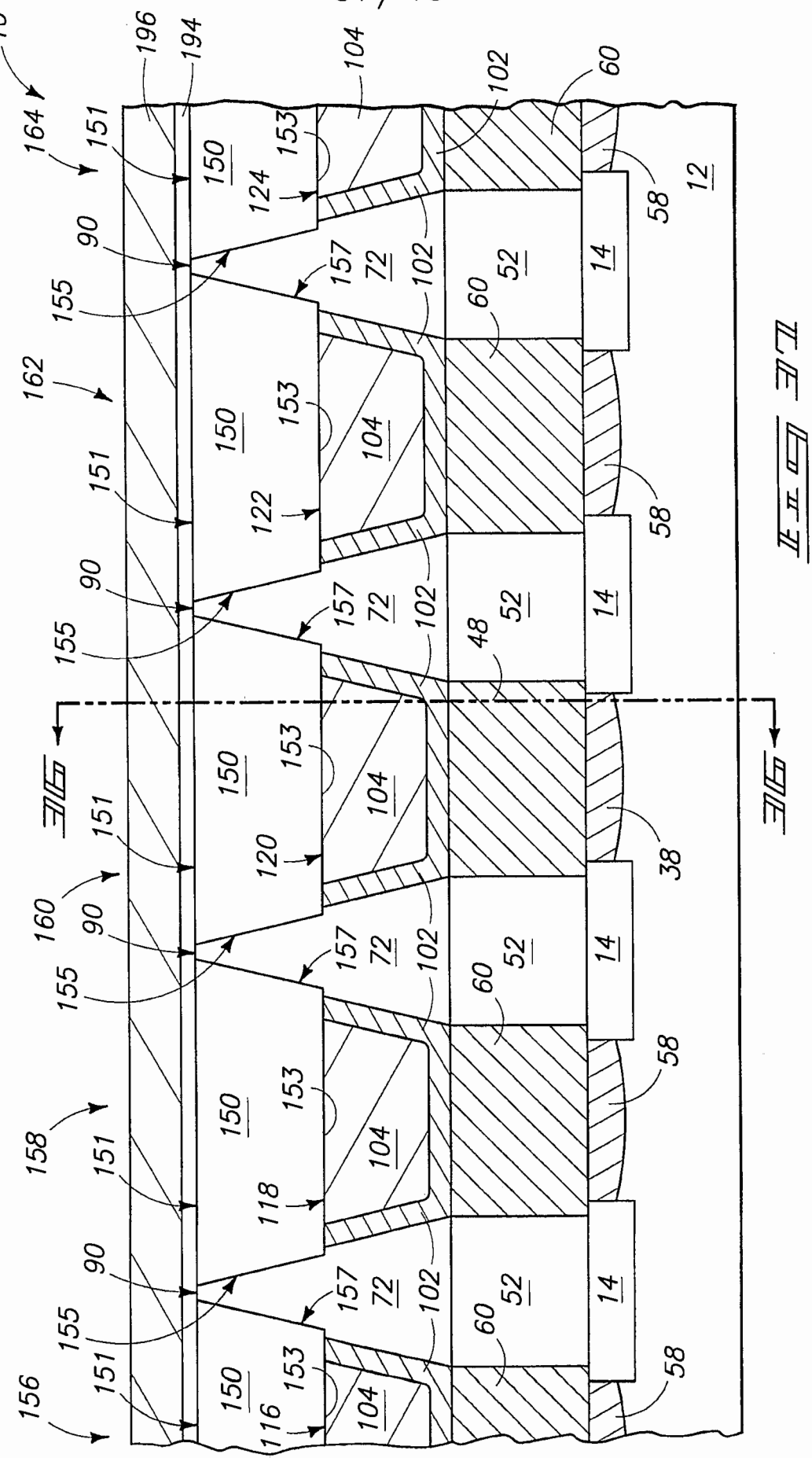

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FIG 37

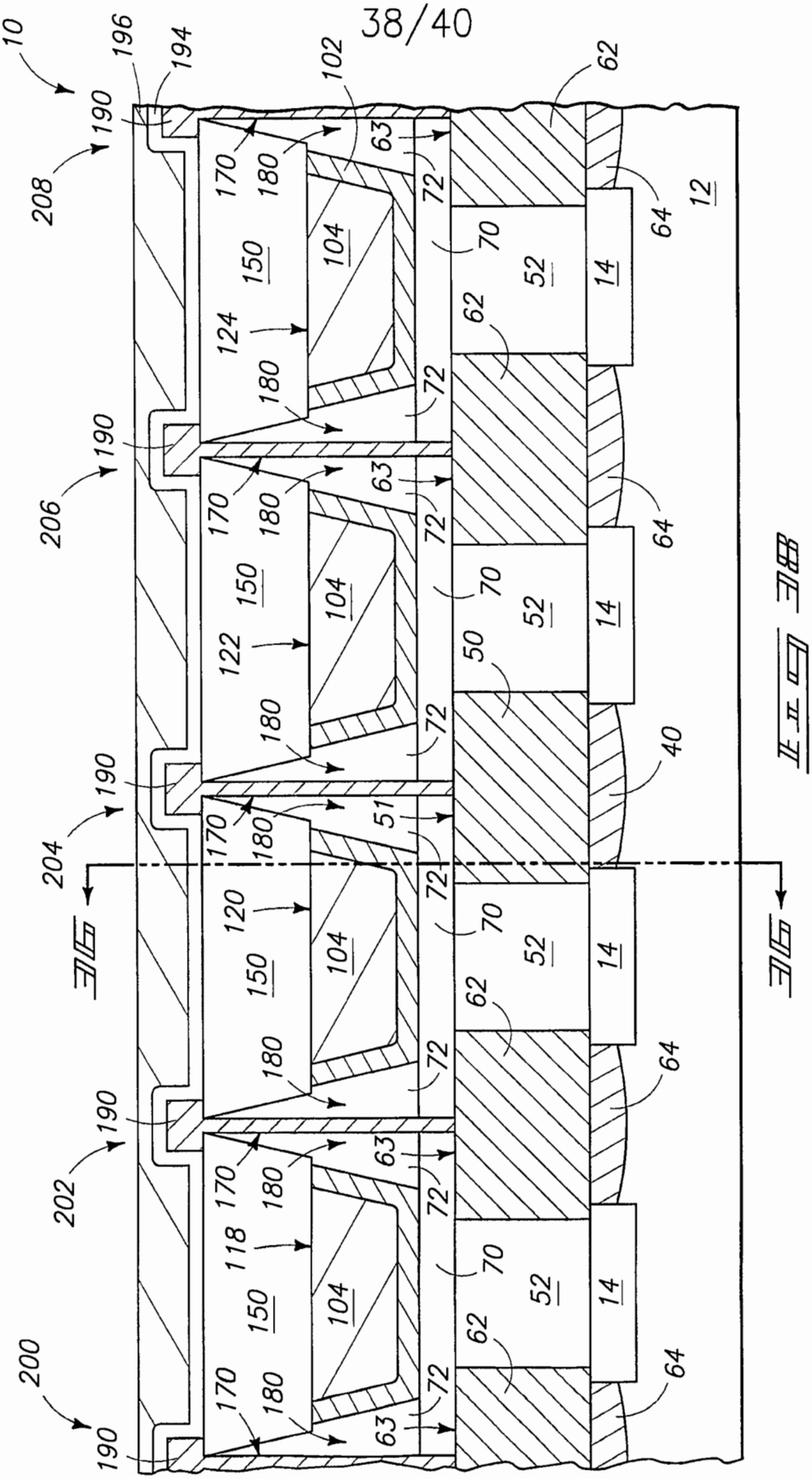

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FIG 38

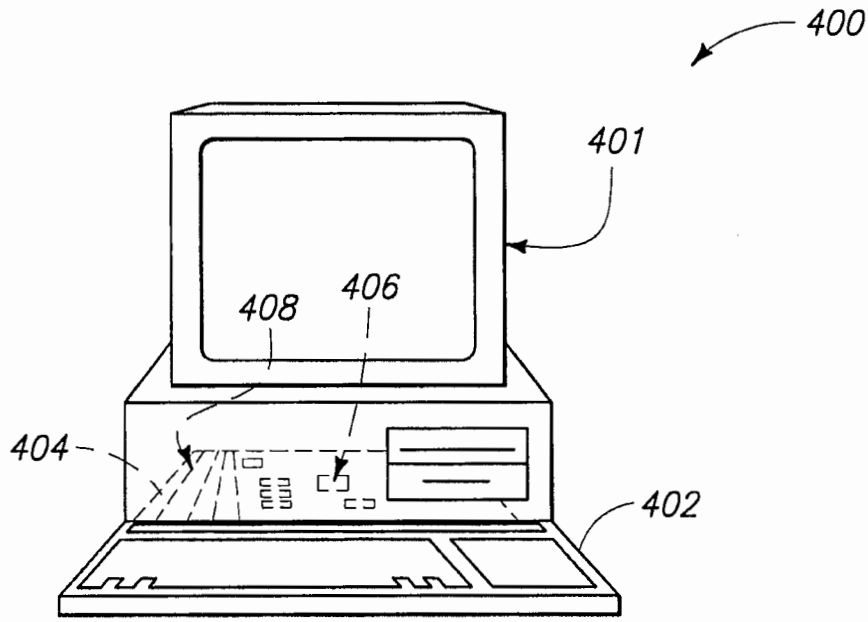


Fig 39

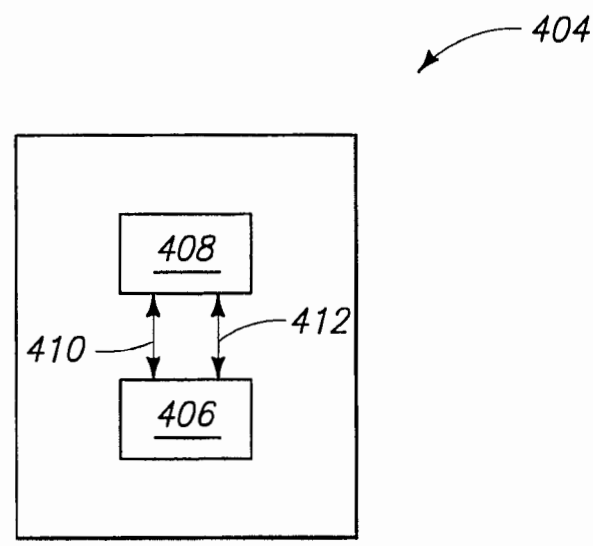


Fig 40

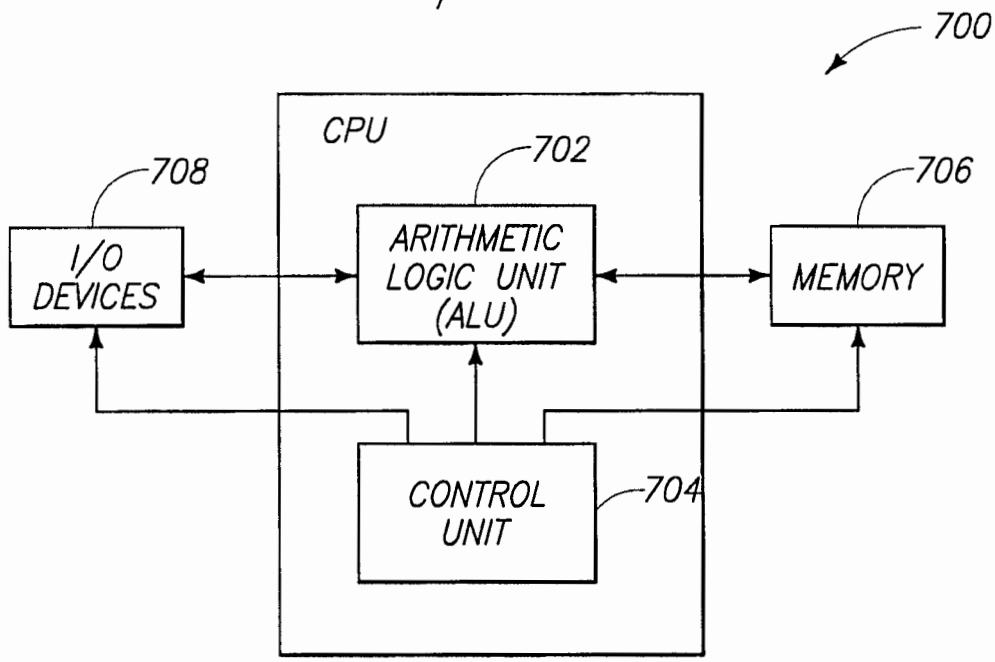

700
CPU
702
708
706
I/O DEVICES
ARITHMETIC LOGIC UNIT (ALU)
MEMORY
CONTROL UNIT
704

Fig. 1

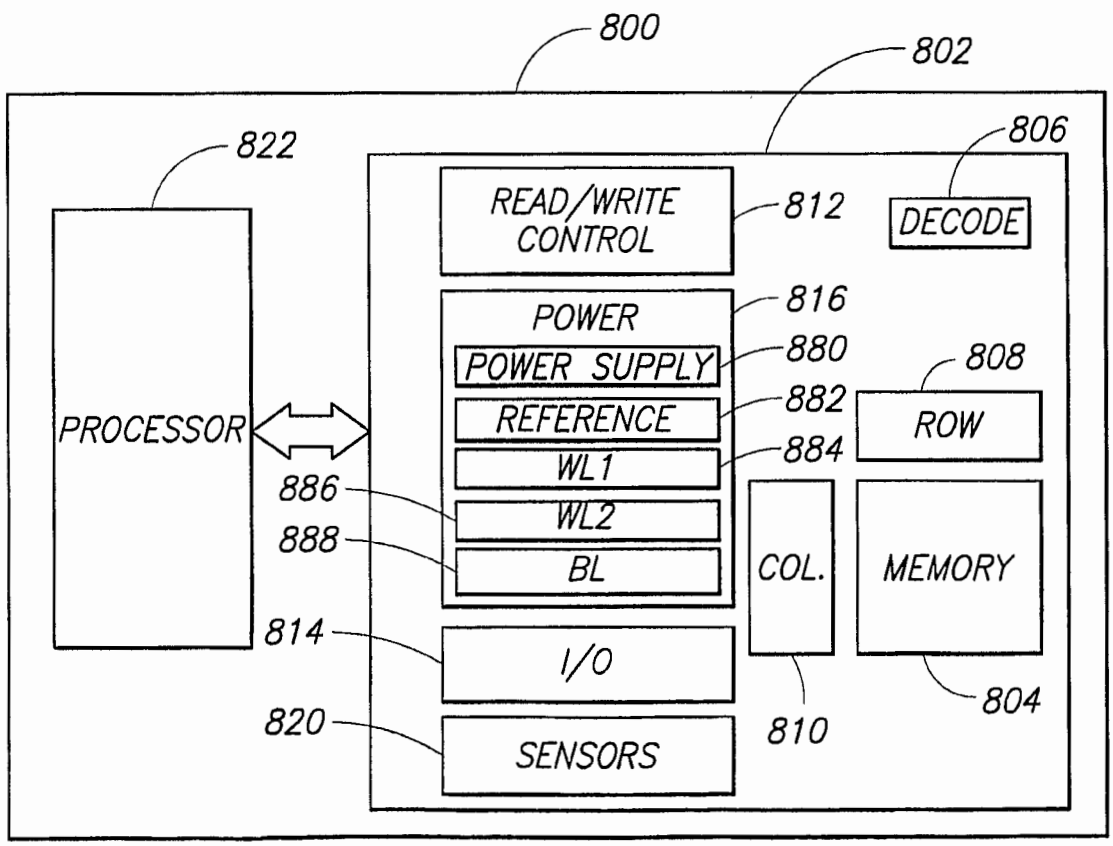

800
802
822
806
READ/WRITE CONTROL
812
DECODE
816
POWER
POWER SUPPLY
880
808
REFERENCE
882
ROW
PROCESSOR
884
WL1
886
WL2
888
BL
COL.
MEMORY
814
I/O
804
820
SENSORS
810

Fig. 2